



Detailed Course Description - Course Plan Development and Updating Procedures/ Department	QFXX/0408-3.0E
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Faculty	Science & Information Technology	Department	Computer Science
Course number	112334	Course title	Computer Architecture
Number of credit hours	3	Pre-requisite/co-requisite	Computer organization and design

Brief course description

Computer architecture is concerned with computer design , organization , operating systems, networks, and many other materials. This course introduces the following topics: **Register transfer and microoperations, ALU circuit, Bus system, Simple computer architecture, Control unit, Instruction cycle, Addressing architectures, Parallel processing, CISC and RISC computers, Modes of transfer.**

Course goals and learning outcomes	
Goal 1	Learning about the basic hardware components and simple computer architecture.
Learning outcomes	1.1 Construct registers and counters 1.2 Use register transfer language to specify microoperations. 1.3 Understand different microoperations and design an ALU circuit.
Goal 2	Understanding simple computer organization.
Learning outcomes	2.1 Define the computer instruction code. 2.2 Explain the basic computer organization. 2.3 Construct the control unit and control signals.
Goal 3	Recognizing addressing architectures.
Learning outcomes	3.1 Understand instruction formats and addressing modes. 3.2 Design the bus system. 3.3
Goal 4	Providing knowledge of parallel processing and pipelining.
Learning outcomes	4.1 Understand the Instruction cycle and parallel processing. 4.2 Understand the execution of different instructions and modes of transfer. 4.3
Textbook	1.- William Stallings, "Computer Organization and architecture", 10th ed, Prentice- hall , 2016 . 2.-
Supplementary	1.- David Harris and Sarah Harris, "Digital design and computer architecture",

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references	<p>2nd ed., Morgan Kaufmann, 2012.</p> <p>2.- John L. and David A., ‘Computer Architecture ’, 5th ed, Morgan Kaufmann, 2011 .</p> <p>3.- Linda Null and Julia Lobur, ‘Essentials of Computer Organization and Architecture’, 3rd ed, Jones & Bartlett Learning, 2010.</p>
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Course timeline				
Week	Number of hours	Course topics	Pages (textbook)	Notes
01	1	Register transfer and microoperations.	335-375	
	1	Registers.		
	1	Counters.		
02	1	Control word.	447- 454	
	1	Memory transfer .		
	1	ALU circuit.		
03	1	Arithmetic circuit.		
	1	Logic circuit.		
	1	Shift circuit.		
04	1	Bus system.	458-464	
	1	CPU, register organization.		
	1	Register stack.		
05	1	Memory stack.	464-471	
	1	A simple computer architecture.		
	1	Instruction code.		
06	1	Stored program organization.		
	1	Direct and indirect addresses.		
	1	First Exam .		
07	1	Computer registers.	471- 477	
	1	Common bus system.		
	1	Computer instructions.		
08	1	Control unit.	477- 499	
	1	Control signals .		
	1	Instruction cycle.		
09	1	Register reference instructions.		
	1	Memory reference instructions.		
	1	I/O Fundamentals.		
10	1	I/O instructions.	499-511	
	1	Complete computer description.		
	1	Addressing architectures .		
11	1	Addressing modes and Instruction formats..	543-549	
	1	Parallel processing.		
	1	Pipelining.		
12	1	Instruction pipeline.	550-554	



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	1 1	CISC and RISC CPUs. Second Exam .		
13	1 1 1	Modes of transfer . Computer I / O. I / O bus and interface unit.	597-627	
14	1 1 1	programmed I / O. Interrupt I / O. DMA.		
15	1 1 1	General problems and applications. Review of previous chapters.		
16	1 1 1	Final Exam .		

Theoretical course evaluation methods and weight	Participation = 10% First exam 20% Second exam 20% Final exam 50%	Practical (clinical) course evaluation methods	Semester students' work = 50% (Reports, research, quizzes, etc.) Final exam = 50%
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Approved by head of department		Date of approval	
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Extra information (to be updated every semester by corresponding faculty member)

Name of teacher	Dr. Maher Nabulsi	Office Number	9332
Phone number (extension)	346	Email	nabulsi@zug.edu.jo
Office hours			