جامعة الزيتونة الأردنية
**Al-Zaytoonah University of Jordan**
كلية العلوم وتكنولوجيا المعلومات
**Faculty of Science and Information Technology**

" عراقة وجودة"
"Tradition and Quality"

| Detailed Course Description - Course Plan Development and Updating Procedures/ Software Engineering Department | QF01/0408-3.0E |
|---|---|

| Faculty | Science and IT | Department | Software Engineering |
|---|---|---|---|
| **Course number** | 0114231 | Course title | Digital Logic Design |
| Number of credit hours | 3 | Pre-requisite/co-requisite | 0114211 |

### Brief course description

This course emphasis on the following topics: the number systems and conversions., Digital systems, Unsigned and signed binary numbers, Binary codes,  Boolean Algebra and logic gates, The map method, Combinational circuits, MSI  circuits, Sequential circuits, Registers and counters.

| | **Course goals and learning outcomes** |
|---|---|
| **Goal 1** | Recognizing basic hardware components and digital systems of computer. |
| Learning outcomes | 1.1 Understand the number systems and conversions. |
| **Goal 2** | Knowing Binary codes and Learning about unsigned and signed binary numbers. |
| Learning outcomes | 2.1 Represent unsigned and signed numbers in binary system. <br> 2.2 Construct different binary codes. |
| **Goal 3** | Learning about Boolean Algebra and logic gates and knowing the map method. |
| Learning outcomes | 3.1 Use Boolean algebra to describe digital circuits . <br> 3.2 Use the map method for simplification Boolean functions. <br> 3.3 Understand NAND  &  NOR  implementations. <br> 3.4 Use the don't care conditions in the map method . |
| **Goal 4** | Providing knowledge of combinational and sequential circuits. |
| Learning outcomes | 4.1 Define the combinational and sequential circuits. <br> 4.2 Design the combinational circuits ( adder, subtractor,..) <br> 4.3 Design MSI circuits ( decoder, encoder, MUX, …) |
| **Textbook** | 1. Morris.M.Mano, Michael Ciletti,**" digital design",** 5th ed.,  Prentice-hall , 2013 . |
| **Supplementary references** | 1. David Harris and Sarah Harris, "**Digital design and computer architecture** ", 2nd ed, Morgan Kaufmann, 2012. <br> 2. David L. Prowse, "**Computer Structure and Logic** ",Pearson Education, 2011. <br> 3. John L. and David A**.,** "**Computer Organization and Design",** 4th ed, Morgan Kaufmann , 2011. <br>  4. Charles , Larry Kinny, "**Fundamentals of Logic Design** ",6th ed. , Thomson,  2009. |

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| Course timeline | | | | |
|---|---|---|---|---|
| **Week** | **Number of hours** | **Course topics** | **Pages (textbook)** | **Notes** |
| **01** | 1<br>1<br>1 | **Digital systems.**<br>• Number systems.<br>• Conversions between systems. | 1-16 | |
| **02** | 1<br>1<br>1 | • Complements .<br>• Unsigned numbers.<br>• Signed numbers . | | |
| **03** | 1<br>1<br>1 | **Binary codes.**<br>• Codes for decimal digits<br>• Parity code and error detection.<br>• ASCII code . | 16- 33 | |
| **04** | 1<br>1<br>1 | **Boolean Algebra and logic gates.**<br>• Theorems and properties. | 33-64 | |
| **05** | 1<br>1<br>1 | • Boolean functions.<br>• Canonical and Standard forms , non-standard .<br>• Logic operations and gates. | | |
| **06** | 1<br>1<br>1 | • Buffer, inverter , AND, OR .<br>• NAND, NOR , E – OR , E -NOR .<br>**First Exam .** | | |
| **07** | 1<br>1<br>1 | **The map method.**<br>• Two , three and four- variable functions .<br>• Product of sums simplification. | 64-110 | |
| **08** | 1<br>1<br>1 | • NAND & NOR implementations.<br>• Don't care conditions .<br>**Combinational circuits.** | 111-126 | |
| **09** | 1<br>1<br>1 | • Design procedure. Half adder, full adder.<br>• Half sub-tractor, full sub-tractor.<br>• Analysis procedure . | | |
| **10** | 1<br>1<br>1 | • Code conversion.<br>• Parity generator and parity checker.<br>**MSI circuits.** | 126- 166 | |
| **11** | 1<br>1 | • Parallel adder- subtractor circuit.<br>• Decoder , encoder. | | |

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|  |  | 1 | • MUX , De-MUX . |  |  |
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| **12** |  | 1 | **Second Exam** | 167- 175 |  |
|  |  | 1 | **Sequential circuits.** |  |  |
|  |  | 1 | • Analysis of clocked sequential circuits . |  |  |
| **13** |  | 1 | • Flip-flops :  SR , D |  |  |
|  |  | 1 | • JK , and  T |  |  |
|  |  | 1 | • Excitation tables. |  |  |
| **14** |  | 1 | **Registers and counters.** | 175 - 217 |  |
|  |  | 1 | • Design of registers. |  |  |
|  |  | 1 | • Design of counters. |  |  |
| **15** |  | 1 | • General problems and applications. |  |  |
|  |  | 1 | • Review of previous chapters. |  |  |
|  |  | 1 |  |  |  |
| **16** |  | 1 | **Final Exam .** |  |  |
|  |  | 1 |  |  |  |
|  |  | 1 |  |  |  |

| **Theoretical course evaluation methods and weight** | Participation = 10% First exam 20% Second exam 20% Final exam 50% | **Practical (clinical) course evaluation methods** | Semester students' work = 50% (Reports, research, quizzes, etc.) Final exam = 50% |
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| **Approved by head of department** |  | **Date of approval** |  |
|---|---|---|---|
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Extra information (to be updated every semester by corresponding faculty member)

| **Name of teacher** | Dr. Dara Aqel | Office Number |  |
|---|---|---|---|
| Phone number (extension) |  | Email | ___d.aqel____@zug.edu.jo |
| Office hours |  |  |  |