Detailed Course Description - Course Plan Development and Updating Procedures/ Computer Science Department	QF01/0408-3.0E

Faculty	Science and IT	Department	Computer Science
Course number	0112231	Course title	Logic Design
Number of credit hours	3	Pre-requisite/co-requisite	0112114 Discrete Structure

Brief course description

	Course goals and learning outcomes
Goal 1	Recognizing basic hardware components and digital systems of computer.
Learning outcomes	1.1 Understand the number systems and conversions.
Goal 2	Knowing Binary codes and Learning about unsigned and signed binary numbers.
Learning outcomes	2.1 Represent unsigned and signed numbers in binary system. 2.2 Construct different binary codes.
Goal 3	Learning about Boolean Algebra and logic gates and knowing the map method.
Learning outcomes	3.1 Use Boolean algebra to describe digital circuits . 3.2 Use the map method for simplification Boolean functions. 3.3 Understand NAND & NOR implementations. 3.4 Use the don't care conditions in the map method .
Goal 4	Providing knowledge of combinational and sequential circuits.
Learning outcomes	4.1 Define the combinational and sequential circuits. 4.2 Design the combinational circuits (adder, subtractor,..) 4.3 Design MSI circuits (decoder, encoder, MUX, …)
Textbook	1. Morris.M.Mano, Michael Ciletti," **digital design",** 5th ed., Prentice-hall , 2013 .
Supplementary references	1. David Harris and Sarah Harris, "**Digital design and computer architecture ",** 2nd ed, Morgan Kaufmann, 2012. 2. David L. Prowse, "**Computer Structure and Logic** ",Pearson Education, 2011. 3. John L. and David A**.,** "**Computer Organization and Design",** 4th ed, Morgan Kaufmann , 2011. 4. Charles , Larry Kinny, **"Fundamentals of Logic Design ",**6th ed. , Thomson, 2009.

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Course timeline				
Week	**Number of hours**	**Course topics**	**Pages (textbook)**	**Notes**
01	**1** **1** **1**	**Digital systems.** Number systems. Conversions between systems.	1-16	
02	**1** **1** **1**	Complements . Unsigned numbers. Signed numbers .		
03	**1** **1** **1**	**Binary codes.** Codes for decimal digits. Parity code and error detection.	16- 33	
04	**1** **1** **1**	ASCII code . **Boolean Algebra and logic gates.** Theorems and properties .	33-64	
05	**1** **1** **1**	Boolean functions. Canonical and Standard forms , non-standard . Logic operations and gates.		
06	**1** **1** **1**	Buffer, inverter , AND, OR . NAND, NOR , E – OR , E -NOR . **First Exam .**		
07	**1** **1** **1**	**The map method.** Two , three and four- variable functions . Product of sums simplification.	64-110	
08	**1** **1** **1**	NAND & NOR implementations. Don't care conditions . **Combinational circuits.**	111-126	
09	**1** **1** **1**	Design procedure. Half adder, full adder. Half sub-tractor, full sub-tractor. Analysis procedure .		
10	**1** **1** **1**	Code conversion. Parity generator and parity checker. **MSI circuits.**	126- 166	
11	**1** **1** **1**	Parallel adder- subtractor circuit. Decoder , encoder. MUX , De-MUX .		

12	**1 1 1**	**Second Exam** **Sequential circuits.** Analysis of clocked sequential circuits .	167- 175	
13	**1 1 1**	Flip-flops : SR , D JK , and T Excitation tables.		
14	**1 1 1**	**Registers and counters.** Design of registers. Design of counters.	175 - 217	
15	**1 1 1**	General problems and applications. Review of previous chapters.		
16	**1 1 1**	**Final Exam .**		

Theoretical course evaluation methods and weight	Participation = 10% First exam 20% Second exam 20% Final exam 50%	**Practical (clinical) course evaluation methods**	Semester students' work = 50% (Reports, research, quizzes, etc.) Final exam = 50%

Approved by head of department		**Date of approval**	

Extra information (to be updated every semester by corresponding faculty member)

Name of teacher		Office Number	
Phone number (extension)		Email	_____@zug.edu.jo
Office hours			