QF01/0408-4.0E	Course Plan for Bachelor program - Study Plan Development and Updating Procedures/ Computer Science Department

Study plan No.	**2021/2022**		**University Specialization**		**Computer Science**		
Course No.	**0112 341**		**Course name**		**Computer Architecture**		
Credit Hours	**3 hours**		**Prerequisite Co-requisite**		**Operating Systems**		
Course type	☐ **MANDATORY UNIVERSITY REQUIREMENT**	☐ **UNIVERSITY ELECTIVE REQUIREMENTS**	**FACULTY MANDATORY REQUIREMENT**	☑ **Support course family requirements**	☐ **Mandatory requirements**	☐ **Elective requirements**	
Teaching style	☐ **Full online learning**		☑ **Blended learning**		**Traditional learning**		
Teaching model	☐ **2 Synchronous: 1asynchronous**		☑ **2 face to face : 1synchronous**		**3 Traditional**		

Faculty member and study divisions' information (to be filled in each semester by the subject instructor)

Name	Academic rank	Office No.	Phone No.	E-mail	
Dr. Maher Nabelsi	**Associate professor**	**9332**	**-**	**nabulsi@zuj.edu.jo**	
Division number	**Time**	**Place**	**Number of students**	**Teaching style**	**Approved model**
				Blended	**2:1**

Brief description

Computer architecture is concerned with computer design, organization, operating systems, networks, and many other materials. This course introduces the following topics: **Register transfer and micro-operations, ALU circuit, Bus system, Simple computer architecture, Control unit, Instruction cycle, Addressing architectures, Parallel processing, CISC and RISC computers, Modes of transfer.**

Learning resources

Course book information (Title, author, date of issue, publisher ... etc)	William Stallings, "**Computer Organization and architecture"**, 10th ed, Prentice- hall , 2016 .			
Supportive learning resources (Books, databases, periodicals, software, applications, others)	1. David Harris and Sarah Harris, "**Digital design and computer architecture",** 2nd ed., Morgan Kaufmann, 2012. 2. John L. and David A., '**Computer Architecture** " , 5th ed, Morgan Kaufmann, 2011 . 3. Linda Null and Julia Lobur, "**Essentials of Computer Organization and Architecture**", 3rd ed, Jones & Bartlett Learning, 2010.			
Supporting websites	https://elearning.zuj.edu.jo			
The physical environment for teaching	☑ Class room	☐ labs	☐ Virtual educational platform	☐ Others
Necessary equipment and software	----------			

QF01/0408-4.0E	Course Plan for Bachelor program - Study Plan Development and Updating Procedures/ Computer Science Department

Supporting people with special needs	----------
For technical support	----------

Course learning outcomes (S= *Skills, C= Competences K= Knowledge,)*

No.	Course learning outcomes	The associated program learning output code
	Knowledge	
K1	Learning about the basic hardware components and simple computer architecture.	**MK3**
K2	Understanding simple computer organization.	**MK3**
K3	Recognizing addressing architectures.	**MK3**
K4	Providing knowledge about parallel processing and pipelining.	**MK3**
	Skills	
S1	Construct registers and counters. Use register transfer language to specify micro-operations. Understand different micro-operations and design an ALU circuit.	**MS5**
S2	Define the computer instruction code. Explain the basic computer organization. Construct the control unit and control signals.	**MS5**
S3	Understand instruction formats and addressing modes. Design the bus system.	**MS5**
S4	Understand the Instruction cycle and parallel processing. Understand the execution of different instructions and modes of transfer.	**MS5**
	Competences	
C1	The ability to understand the simple computer architecture.	**MC4**
C2	The ability to understand simple computer organization.	**MC4**
C3	The ability to use different addressing architectures.	**MC4**
C4	The ability to Recognize parallel processing and pipelining.	**MC4**

Mechanisms for direct evaluation of learning outcomes

Type of assessment / learning style	Fully electronic learning	Blended learning	Traditional Learning (Theory Learning)	Traditional Learning (Practical Learning)
First exam	0	**0**	%20	0
Second / midterm exam	%30	**%30**	%20	30%
Participation / practical applications	0	**0**	10	30%
Asynchronous interactive activities	%30	**%20**	0	0
final exam	%40	**%50**	%50	40%

Note: Asynchronous interactive activities are activities, tasks, projects, assignments, research, studies, projects, and work within student groups ... etc, which the student carries out on his own, through the virtual platform without a direct encounter with the subject teacher.

Schedule of simultaneous / face-to-face encounters and their topics

QF01/0408-4.0E	Course Plan for Bachelor program - Study Plan Development and Updating Procedures/ Computer Science Department

Week	Subject	learning style*	Reference **
1	**Register transfer and microoperations.** Registers. Counters.	Lectures	335-375
2	Control word. Memory transfer . **ALU circuit.**	Lectures	447- 454
3	Arithmetic circuit. Logic circuit. Shift circuit.	Lectures	
4	**Bus system.** CPU, register organization. Register stack.	Lectures	458-464
5	Memory stack. **A simple computer architecture.** Instruction code.	Lectures	464-471
6	Stored program organization. Direct and indirect addresses.	Lectures	
7	Computer registers. Common bus system. Computer instructions. **Midterm Exam.**	Lectures	471- 477
8	**Control unit.** Control signals. **Instruction cycle.**	Lectures	477- 499
9	Register reference instructions. Memory reference instructions. I/O Fundamentals.	Lectures	
10	I/O instructions. Complete computer description. **Addressing architectures.**	Lectures	499-511
11	Addressing modes and Instruction formats.. **Parallel processing.** Pipelining.	Lectures	543-549
12	Instruction pipeline. **CISC and RISC CPUs.**	Lectures	550-554
13	**Modes of transfer**. Computer I / O. I / O bus and interface unit.	Lectures	597-627
14	programmed I / O. Interrupt I / O. DMA.	Lectures	
15	General problems and applications. Review of previous chapters.	Lectures	

16	Final Exam

*** Learning styles: Lecture, flipped learning, learning through projects, learning through problem solving, participatory learning ... etc.**
**** Reference: Pages in a book, database, recorded lecture, content on the e-learning platform, video, website ... etc.**

Schedule of asynchronous interactive activities (in the case of e-learning and blended learning)

Week	Task / activity	Reference	Expected results
1	Differentiate between combinational and sequential circuits.	https://elearning.zuj.edu.jo	Understanding
2	Construct registers.	https://elearning.zuj.edu.jo	Understanding and developing
3	Construct counters.	https://elearning.zuj.edu.jo	Understanding and developing
4	Use register transfer language to specify micro-operations.	https://elearning.zuj.edu.jo	Understanding
5	Construct bus system.	https://elearning.zuj.edu.jo	Understanding and developing
6	Construct arithmetic circuit.	https://elearning.zuj.edu.jo	Understanding and developing
7	Construct logic circuit.	https://elearning.zuj.edu.jo	Understanding and developing
8	Construct shift circuit.	https://elearning.zuj.edu.jo	Understanding and developing
9	Design an ALU circuit.	https://elearning.zuj.edu.jo	Understanding
10	Use instruction formats.	https://elearning.zuj.edu.jo	Understanding
11	Use addressing modes.	https://elearning.zuj.edu.jo	Understanding
12	Construct the control unit and control signals.	https://elearning.zuj.edu.jo	Understanding and developing
13	Describe the steps of Instruction cycle.	https://elearning.zuj.edu.jo	Understanding
14	Specify the advantages of parallel processing and pipelining.	https://elearning.zuj.edu.jo	Understanding
15			
16			