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Interlayer Dielectrics

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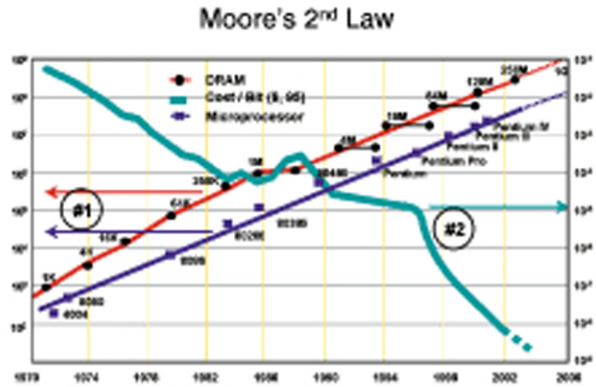

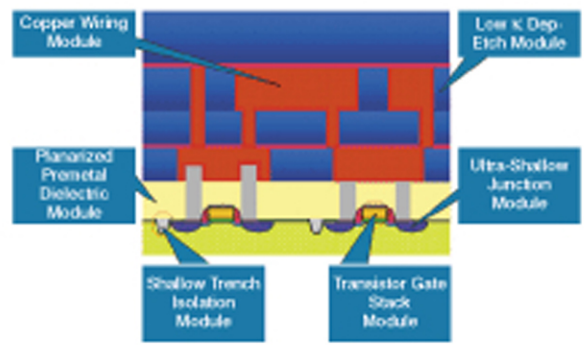

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Interlayer Dielectrics for Semiconductor Technologies

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Preface

Electrically insulating materials form the dielectric films used in capacitors, the gate dielectrics in the metal–oxide–semiconductor field-effect transistors (MOSFETs), and the isolation between the electrical conductors used as contacts and interconnections (both on-chip and in packaging). Interlayer dielectric (ILD) materials play the role of isolating electrically conducting and semiconducting features and films. They also perform as masks against impurities, such as in selective-area diffusion, ion implantation, and impurities from the processing environment. More recently, they have also served as a stop layer for the chemical mechanical polishing of a metal on top of the ILD. Classically, silicon dioxide, deposited by chemical vapor deposition techniques, has been the preferred ILD material, both undoped and doped with phosphorus, boron, arsenic, and/or germanium. However, with the continued shrinking of the channel length of the MOSFET, the interconnect dimensions are also shrinking to accommodate an increasing number of devices. This has led to a serious interconnect-related circuit delay and to compromising the performance advantages of decreasing channel length. This delay, generally known as RC delay, is associated with the increasing interconnect resistance (R) and increasing ILD capacitance (C). Use of Cu as a replacement for Al has lowered R by about 40%. There is considerable effort expended, now, in lowering C by replacing SiO_2 (dielectric constant $\kappa = 4.0$) with lower-κ ILD materials.* This book, for the first time, puts together the science and technology of the ILD materials and associated processes in one volume, written by authors with experience in the field. It is, thus, an edited volume with 13 chapters written to cover the science, properties, and applications of different ILD materials, including silicon-based dielectrics, low-κ materials, such as polymers, porous materials, C and/or F doped silicon oxides, high dielectric constant materials, and those useful for wave guide applications in optical communications on the chip and the package. The book provides up-to-date knowledge with appropriate references for further reading and research. It is noted that the knowledge (both from materials and process points of view) about the SiO_2-based dielectrics is thought to be more or less complete. However, the continued shrinkage in the dielectric film dimensions and the use of newer materials (e.g. Cu), which contact dielectrics, have led into much more stringent requirements and thus into newer domains of research and applicability determinations of SiO_2 as ILD and as gate oxide. As far as newer low-κ ILD materials are concerned, we know very little. Admittedly, the field of ILD materials, both low-κ and high-κ, is young and this book provides a up-to-date starting point. In Chapter 1, the subject of ILD is

*Both the symbols 'k' and 'κ' are used in literature for dielectric constant. Throughout the book, except chapters 7, 8, 10, and 11, symbol 'κ' is used.

introduced with reference to the present and future semiconductor integrated circuit technologies and the challenges that lie ahead in the development of ILD materials and processes.

In Chapter 2, the properties of ILD materials are discussed in four groupings: electrical, mechanical, chemical and electrochemical, and thermal and thermodynamic. The chapter focuses on the properties of the ILD materials in particular emphasizing the impact of processing, actual use, and interactions with other materials that the ILD is in contact with. Many known and relevant properties are presented, for easy reference, in tabular format.

Chapter 3 focuses on ILD materials characterization techniques necessary in evaluating and thus in the development of low dielectric constant materials. Development of characterization techniques, with some emphasis on thermo-mechanical properties is discussed. Recently developed techniques used for porous dielectrics are included. Finally, an attempt is made to correlate molecular structure and materials properties, specifically using three classes of dielectrics, namely polymers, silsesquioxanes, and porous materials.

Chapter 4 examines the key interfaces and interactions between dielectrics and metals, dielectrics and semiconductors, and between different dielectrics for advanced semiconductor technologies, such as porous and dense dielectrics, organic, and silicon-based materials. The different methods for detecting interactions are compared. Modeling is presented as a method to predict interface reliability and the impact of material changes and interface modifications. The impact of dielectric interface properties on performance and reliability issues such as chemical mechanical polishing (CMP) compatibility, packaging reliability, as well as transistor performance, *RC* delay, and electromigration (EM) resistance, is also addressed.

Chapter 5 focuses on silicon-based deposited dielectric oxides, nitrides, and oxynitrides, and includes doped oxides. Deposition, resultant properties, and applications such as ILD are discussed.

Chapter 6 examines the status of polymer-ILD related work, with special emphasis on the role of the structure and its stability, preparation methods, interactions with surrounding materials, and adhesion. The discussion includes a brief presentation of polymer-chemistry related variations in the monomers and their polymerized (ILD films) products.

Chapter 7 covers CVD deposited amorphous carbon fluorides, a new group of low-κ materials. They contain C, F, H, and O and are shown to yield κ as low as 2.3. This chapter discusses the fundamentals, deposition, and properties of C-F films and issues related to integration of C-F films as an ILD in the advanced Si ICs.

Trapped air or inert gases can lower the κ very effectively. Chapters 8 and 9 explore a range of low-κ porous materials focusing on nanoporous silica xerogels as a benchmark. Preparation, defect-porosity characterization, properties, adhesion, processing, and interaction with metals have been critically examined and discussed. Tables and figures provide relevant data.

Chapter 10 diverts from the general thrust of the low-κ dielectrics. There is a serious need of high-κ dielectrics for applications such as capacitor and gate dielectrics and as isolation layers in packages. The dielectric constants of such materials range from 10 to >1000. The key to their applicability lies in keeping leakage currents very low. This chapter examines such materials and their deposition with emphasis on atomic layer deposition (ALD).

The possibility of using photonic interconnects on-chip is being examined as a replacement for slower electronic (metallic) interconnects. An integral part of this photonic interconnect scheme is a guided wave system for the photon's propagation. The bit rate capacity or bandwidth of a passive waveguide is independent of its length for chip-level interconnects. Chapter 11 focuses on these guided wave systems. Applications of such systems are examined for a variety of cases, for example, on-chip, off-chip, and three-dimensional stacked chips. Materials characteristics, of both low- and high-κ materials are defined and examined.

Chapter 12 discusses the reliability of ILD materials used as insulating layers in a multilevel interconnection scheme. It focuses on considering all types of failure and the causes that affect the usefulness and the intended life of the ILD, thus of the device/circuit and on identifying and eliminating these causes. Standard modes of evaluation and prediction of the useful life are reviewed.

Chapter 13 examines the requirements for the continuation of CMOS scaling, both for high-performance logic and memory devices, and the implications for future process and material technology requirements, with emphasis on dielectrics.

Wherever the fast-moving semiconductor technologies take us, it is becoming obvious that new materials are needed for all types of applications. Manipulating the materials and their properties at atomic dimensions has become a must and a challenge at the same time. This book attempts to present the case of ILD materials with these thoughts in mind.

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Contents

Interlayer Dielectrics for Semiconductor Technologies
Murarka, Eizenberg and Sinha (Eds.)
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Chapter 1
Introduction: interlayer dielectrics in microelectronic devices

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The last few decades are frequently described as the solid-state electronics revolution era, the most significant technological revolution since the industrial revolution of the nineteenth century. Solid-state electronics has now totally engulfed our life, and its applications continue to grow at an unprecedented rate.

The most significant characteristic of the development and evolution of the solid-state electronics industry lies in the continuous miniaturization of the device dimensions in the circuit (expressed in The International Technology Roadmap for Semiconductors, 2001 [1]), leading to more components and more functions per area, as described by Moore's law (Fig. 1.1). This shrink and the efforts of the industry to abide by Moore's law are driven by two factors: the improved performance due to increased speed and more functions per unit area, and the lower cost per bit. Thus, the solid-state electronics of the 1960s evolved into microelectronics when typical lateral device dimensions reached the micrometer range. Now we are rapidly approaching the era of nanoelectronics as lateral dimensions are set to decrease below 100 nm (0.1 μm).

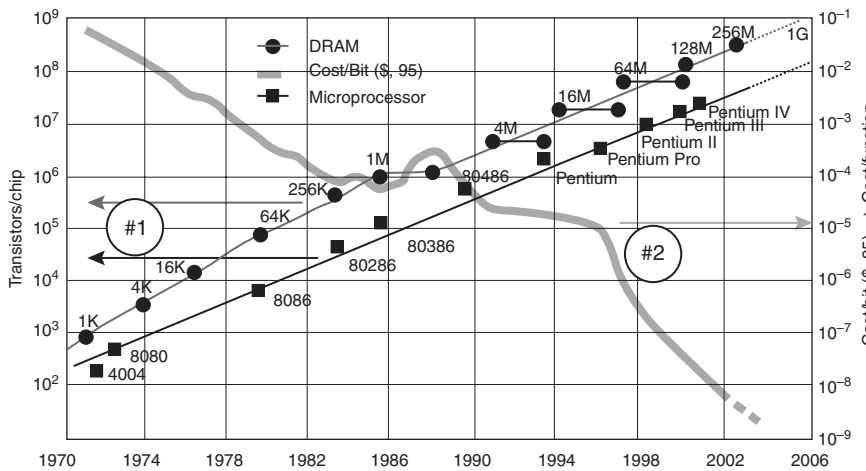

Fig. 1.1 Moore's law (Source: *Forbes* March 25, 1995 and *Applied Materials*, 1999).

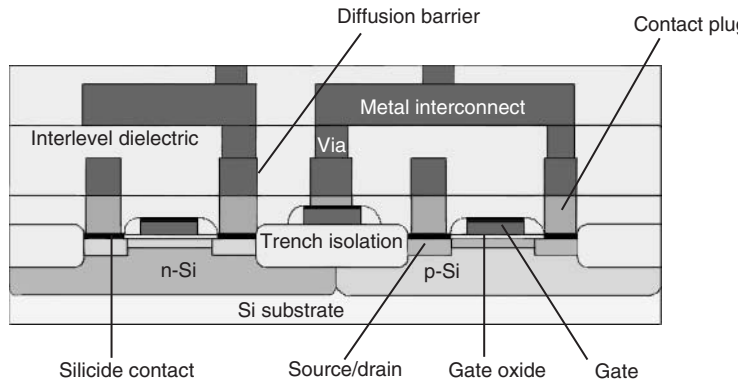

Fig. 1.2 Schematic drawing of a CMOS device.

Materials have played and will play increasingly a crucial role in this microelectronics revolution and evolution. The ability to produce devices with high performance, high reliability, and affordable price depends on the materials chosen and on our ability to process them in such a way that they will function in the desired manner during the device fabrication and in the actual use with a predicted reliability.

The core of a microelectronic device is the semiconducting material. Most of current microelectronic devices are based on silicon (Si), while some, especially the optoelectronic devices, utilize mainly III–V semiconductors such as GaAs, InP, and GaN. This book focuses on developments and trends in ultra-large-scale integrated (ULSI) microelectric devices, and therefore, by default, the semiconductor is Si (at this stage). The transistors and other active parts of the semiconductor are connected by horizontal and vertical conducting segments, mostly metallic (doped poly-Si is also used), that serve as the gate metallization, contacts, and metal interconnects that may consist of an adhesion promoter/diffusion barrier under and over the main current carrier metal, as illustrated in Fig. 1.2. Advanced microprocessors may consist of close to 10 levels of metallization, see Fig. 1.3.

The third-component of a device consists of the dielectric layers. These layers can be divided into three groups according to their function: (i) the active dielectric layers; (ii) the layers needed mainly during device processing; and (iii) the insulating layers.

The first group consists of dielectric films that play an active role in device operation, mainly for the storage of charge. These are the gate oxide and the capacitor dielectric in memory devices.

The second group consists of dielectric films that are needed during device processing. Examples are: (a) anti-reflection coatings (ARC) such as silicon nitride or carbide based layers used for the lithography step; (b) etch stop layers such as silicon nitride or carbide needed during the etching process and more recently during chemical mechanical planarization (CMP); and (c) masks against impurities, for example, metal ion getters, or layers introduced to enable

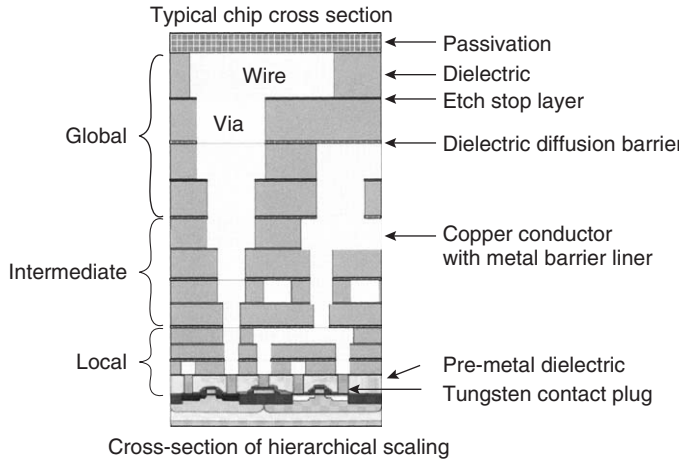

Fig. 1.3 Schematic drawing of a microprocessor with a hierarchical wiring approach for multilevel interconnects. (Copied from Ref. [1].)

selective area diffusion or ion implantation. Most of the layers described above do not have any specific role in device functioning after the completion of its processing. On the contrary, in many cases they affect, interfere, and even degrade the performance. This is the case, as an example, when the etch or CMP stop layer causes an increase in the effective dielectric constant of an interlevel dielectric layer (to be described below) that is desired to have the lowest possible dielectric constant, namely, to serve as a low-κ material.

The third group of dielectric films utilized in microelectronic devices consists of insulating layers. The isolation between two adjacent transistors is done by trench isolation (see Fig. 1.2), and when isolation of the device from the ambient is needed, a dielectric material is used as a passivation cap. The isolation between metal lines in the same level is carried out by an intermetal dielectric, and that between two metal levels is performed by an interlevel dielectric. Both types are usually called interlayer dielectrics (ILDs).

The continued evolution of the microelectronics industry requires the introduction of new materials in order to accommodate the continued miniaturization (shrink in dimensions) with projected improvement in the performance. The latter is expected to continue even if at some point in time the shrink will stop due to economical reasons (might become too complicated and therefore too expensive) or due to physical limitations in device operation (e.g. reaching dimensions where quantum mechanical effects dominate, completely changing the nature of charge transport). The introduction of new materials necessarily requires simultaneous development of processes and studies that examine the compatibility of such materials in the surroundings of the device and the circuit. Simultaneously, other large number of new issues have emerged, all in response to interconnect (the metal and the dielectric) materials, structures, close proximity of

the vertical and horizontal interconnects, power dissipation, and the anisotropy of the dielectric constant. Note that we are heading into smaller and smaller volumes of material, which must be effective and reliable, defect-free with zero or very low stress, and with no or minimal chemical/metallurgical activity (since smallest amounts of matter will coexist in these structures). Such small volume or width or thickness requirements may lead to properties beyond present and naturally accepted values.

New materials have recently been introduced in microelectronic devices in the semiconducting and metallic parts of the device. As new semiconductors, $Si_{1-x}Ge_x$ alloys, either grown epitaxially on the Si substrate or deposited as polycrystalline material, have now been introduced (yet in a limited extent) in order to enhance the charge carrier mobility. Also a dramatic change in the metallic materials is currently taking place. Cu is replacing the currently used Al(Si,Cu) alloys as the interconnect metal in order to increase the circuit speed, to enable operation at higher power levels, and to improve device reliability. Cu has lower electrical resistivity and better electromigration resistance than Al and its alloys. The replacement of the interconnect metal requires also a change in the use of the adhesion promoter/diffusion barrier, and thus TaN_x currently replaces TiN in this function. With further shrink, newer and thinner adhesion promoter/diffusion barrier materials are being sought to replace the current materials in this class. A less dramatic, but not less important, materials change is occurring in the silicides used for contacts, local interconnects, and gate metallization formed with a metal silicide on polysilicon. $TiSi_2$ is phasing out, being replaced by $CoSi_2$, with the possibility of the introduction of NiSi or PtSi for some applications (which in the future might even be replaced by metal gates). All these materials changes practically skipped the dielectric part of the device. Silicon dioxide, in all respects, has been the ideal dielectric for use in Si-based devices and circuits. However, today its limitation, for use as an ILD, is mainly due to its high dielectric constant of about 4.

Now we are on the verge of a period when new materials will be introduced into the third component of the device materials: the dielectrics. The importance of this sector is increasing significantly, and in many aspects it has a critical role in limiting device performance. As device dimensions shrink, the switching speed of its basic element, the MOSFET (metal oxide silicon field effect transistor), is expected to increase, since the carriers transit time (for a given applied voltage) across the length of the channel is decreasing with the shrink of this dimension. However, the effective speed of the device is controlled not only by this intrinsic gate delay, but also by the speed of signal propagation to and from the device through the metal interconnects, the basic charge carriers. These are capacitatively coupled to the insulating dielectrics engulfing them, the ILDs, leading to a so called interconnect *RC* delay time. A simple model of the interconnects equivalent circuit is given in Fig. 1.4, where *P* represents the line pitch, *W* the line width, *S* the line spacing, *T* the line thickness, and the ILD line thickness above and below is equal.

The *RC* delay [2, 3] is given by:

$$RC = 2\rho\,\kappa\,\epsilon_0\,(4L^2/P^2 + L^2/T^2), \tag{1.1}$$

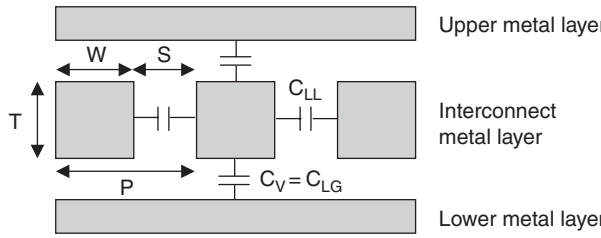

Fig. 1.4 Schematic diagram of a typical interconnect element. Subscripts LG and LL refer to the line-to-ground and line-to-line contributions. (Adapted from Ref. [2] © 1995 IEEE.)

where ρ is the metal resistivity, ϵ_0 the vacuum permittivity, κ the relative dielectric constant of the ILD, and L the line length. The decrease in features size results in a sharp increase in the RC delay time, which for devices smaller than 0.25 μm controls the overall on-chip cycle time [2, 3]. Therefore, in order to increase device speed, the lower resistivity Cu is replacing Al (as discussed above), and the current ILD, SiO_2 (with $\kappa = 4$), will be replaced by other dielectrics with a lower dielectric constant (so-called low-κ materials). An additional reason for the search for the low-k dielectrics is the fact that power dissipation in a circuit is given by:

$$P = \left(\frac{1}{2}\right) f_{\mathrm{d}} C V^2 f, \tag{1.2}$$

where C is the total on-capacitance, V the supply voltage, f the operational frequency, and f_{d} the fraction of gates that switch during a clock period. Reducing κ, thus C, will reduce the power dissipation, will make circuits faster, hence also more portable. The search for suitable low-κ dielectrics is currently the most important and urgent step. There are large number of choices being pursued by the researchers and the microelectronic industry. Thus, the subject of these new and experimental low-κ materials is covered in a significant portion of this book, Chapters 5–9.

The other need to introduce new dielectric materials is that of replacing SiO_2 as the dielectric material in gate and memory capacitors by materials with a higher dielectric constant, so-called high-κ dielectrics. The lateral shrink in device dimensions also requires scaling down the gate oxide thickness to a value which is approaching 1 nm. In such a thin layer of SiO_2, leakage current will increase dramatically due to quantum mechanical tunneling. The problem can be avoided by using a thicker dielectric with a higher κ, still maintaining a capacitance equivalent to a 1 nm SiO_2 film. The drive to replace SiO_2 by a high-κ dielectric for the memory capacitor dielectric is due to the need to reduce memory cell size (especially in embedded memory microprocessors). The extremely small size of the capacitor results in a very small charge, too low to be reliable, especially for portable appliances based on a reduced operating/charging voltage. Replacing SiO_2, with $\kappa = 4$, by a material with a very high κ value (in the range of 100 and even >1000) is important to enable the above discussed shrink of the memory cell size. These two implementations of high-κ dielectrics are discussed in Chapter 10 of our book.

The important role of dielectric materials is expected to increase beyond the scope discussed so far. First, the trend of increases in complexity and performance of devices can continue in spite of the fact that we are approaching the limits of miniaturization of lateral dimensions, by overcoming the difficulties and building three dimensional devices. Also Si transistors will be fabricated on top of an insulator (SOI), and the challenge lies both in the ability to overgrow high-quality Si as well as to control the properties of the underlying insulator. In parallel, efforts are taking place to improve performance by integrating the packaging on the chip. This trend may require adding insulators specific for the packaging process into the device processing sequence, with all possible interactions and limitations. And finally, in order to enhance device speed, optical interconnects may replace some of the current metal interconnects. Dielectric layers will be used in a role new to current Si devices: as optically active layers, waveguides, etc. The possible implementation of high-κ dielectrics for packaging and waveguide applications is discussed in Chapter 11.

This book intends to examine the science of dielectric materials relevant for microelectronic devices, as well as to review the current and future materials for the various applications. Special attention is given to the importance of the various interfaces between the dielectrics and the adjacent metallic, dielectric or semiconducting materials (Chapter 4). We must characterize as well as control these interfaces in order to prevent negative interactions and interferences during processing or operation. Characterization of the dielectrics, covering a very wide range of properties, is a real challenge that is discussed in depth in Chapter 3, but is also embedded in many other chapters. A special chapter is dedicated to the important issues of reliability (Chapter 12).

Although the book has focused mainly on our current knowledge of the properties, processing, and applications of dielectric deposited films in Si-based microelectronic devices, it also examines the future trends in this fascinating field of electrically insulating films made of inorganic, organic, mixed inorganic–organic, and porous materials. The book endeavors in raising some fundamental issues about the properties and use of such interlayer dielectric materials. Presently, finding functional ILD materials with κ less than 2 seems very difficult, and physics and chemistry of such materials in near-atomic-size applications are being examined to find the needed solution. A brief discussion of these scientific issues and hopes and some of our predictions (short term as well as long term) are summarized in Chapter 13.

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Interlayer Dielectrics for Semiconductor Technologies
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Chapter 2
Dielectric properties

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Abstract

This chapter reviews the properties of the dielectric materials with special reference to those used or to be used as the interlayer dielectrics (ILDs) and forming the insulating layers between the interconnect-lines in one plane or in a multilevel scheme of interconnections in an integrated circuit. All the properties, electrical, mechanical, chemical and electrochemical, and thermal and thermodynamic, have been examined both from fundamental and practical application points of view. The impact of process, actual use, and the interactions with other surrounding materials with which the dielectric is in contact with, is examined. Both organic and inorganic dielectrics are considered. Available data on the various properties are listed in various tables for comparison and quick reference purposes.

2.1 Introduction

A dielectric material is defined as a non-conductor of electricity. In other words, it is an effective electrical insulator with very high resistance associated with a large band gap, for example, 8–9 eV for SiO_2 compared to 1.12 for Si. Such materials are, therefore, used as interlayer dielectrics (ILDs) between two levels of the metal interconnections that interconnect the devices among themselves or to the outside world. There are large number of materials, including oxides, ceramics, nitrides, and polymers, that are electrical insulators and candidates for ILD applications. This chapter examines the properties that are essential in determining this application. The chapter also briefly explores the necessary ILD evaluation techniques and the ranges of applicability. It is noted that additional parameters, such as deposition, patterning, planarization, post-metallization processes, etc. will eventually determine these and final applicability on actual integrated circuits.

ILD properties can be grouped into four categories: electrical, mechanical, chemical and electrochemical, and thermal and thermodynamic. Table 2.1 lists all the properties and behaviors that need to be examined and fall in these four categories [1–6]. The process, actual use, and proximity to other materials may alter and thus determine these properties and ensuing behavior and

reliability of ILD materials. This chapter thus not only focuses on ILD properties but also an emphasis is placed on knowing the impact of process, actual use, and interactions with other materials ILD is in contact with, on the properties of the ILD.

2.2 Electrical properties

The electrical stability of the dielectric, whether used as an ILD or as the passivation layer, throughout the processing of the device and during its actual use is of prime importance.

The ILD electrical properties of concern are listed in Table 2.1. These all relate to electrical conduction through the dielectric and polarization that lead to interaction with electrons, as a result of applied field on the conductor in contact with the dielectric. We define the need (that of a good ILD material) in terms of high electrical bulk and surface resistivity, extremely low leakage and thus very high electric field strength (commonly known as dielectric strength), low charge trapping, dielectric constant and its anisotropy, low dissipation, and high reliability. Note that many of these desired behaviors are associated with high band gap and that both alternating and direct current (ac and dc) effects are important and must be examined. Table 2.2 lists the best approximations of the defining properties of new ILD materials with dielectric constants lower than 3 [1–6]. These requirements are modified as we move from post-metallization

Table 2.1 Requirements for low dielectric constant ILD materials

Electrical	Mechanical	Chemical	Thermal
Kappa anisotropy	Film thickness/unif.	High chemical resistance	High thermal stability, T_g
Low dissipation	Adhesion	High etch selectivity	Low thermal expansion
Low leakage	Low stress	Low moisture absorption	Low thermal shrinkage
Low charge trapping	High tensile modulus	Low solubility of H_2O	High thermal conductivity
High electric field strength	High hardness	Low gas permeability	
High reliability	Low shrinkage	High purity	
	Low weight loss	No metal corrosion	
	High crack resistance (high facture toughness)	High storage life	
		Environment Safety and Health (ESH) compatible	

Table 2.2 Defining ILD characteristics

Characteristic	Desired value
	ELECTRICAL
Dielectric constant at 1 MHz	1.5–3
Dissipation factor	< 0.005
Anisotropy	Undesirable
Breakdown strength	≥ 1 MV/cm
Bulk resistivity	$\geq 10^{15}\,\Omega$ cm
Surface resistivity	$\geq 10^{15}\,\Omega$ cm
	MECHANICAL
Final stress	$\leq \pm 100$ MPa
Tensile modulus	> 1 GPa
Tensile strength	> 0.2 GPa
Elongation-at-break	$> 5\%$
Crack resistance	Very high
Adhesion to itself and to metal and diffusion barrier/adhesion promoter	Pass tape peel test after thermal cycling to ~ 400°C
	CHEMICAL
Interaction with acids, bases, and solvents used in processings	Preferably none
CMP	Compatible
Etch	Dry (RIE) high rate, selectivity over metal, oxygen plasma resistance
Moisture absorption	≤ 1 wt%
Out gassing	Low ≤ 500°C
Shelf-life	≥ 6 months, room temperature, 40% relative humidity
Gap-fill capability	Excellent, no voids
Permeable to	Inert gases and hydrogen
Purity	Very high, free of mobile ions, particles $\leq$ ppb level
Metal content thickness uniformity, 3σ	
Within wafer	$< 10\%$
Wafer to wafer	$< 5\%$
Compatible/non-corrosive	With metal and diffusion barrier/adhesion promoter, environmentally safe
	THERMAL
Glass transition temperature onset, slow ramp	≥ 400°C
CTE	< 50 ppm, isotropic
Thermal conductivity	High
Thermal stability	
TGA, 1% weight loss in inert gas at	> 425°C
Out gassing temperature	> 500°C
Shrinkage	$< 2.5\%$

temperatures of ~400–450°C to temperatures as low as 200–250°C and whether we shall use reactive ion etching or dual-damascene chemical mechanical planarization for defining metal interconnections. One must also add a concern, especially related to plasma processes (such as plasma enhanced chemical vapor deposition and dry etching). The dielectric related processes should not cause any damage in the gate dielectric or at the gate dielectric–silicon interface.

2.2.1 Resistivity

The resistivity determines the voltage-induced current through the material. Dielectrics in the integrated circuits are subjected to very high electric fields up to 10^7 (higher in cases of high voltage devices/circuits) volt/cm. Thus very high resistivity ($> 10^{14}\,\Omega\,\text{cm}$ at 25°C) materials are preferred. Higher ILD resistivities are important to prevent charge carriers moving from one of the metallic interconnect/dielectric interfaces to such other interfaces thus causing high unacceptable leakages. Mechanisms of the charge carrier movements (that may be non-ohmic) through the ILD are discussed under the next subheading of leakage.

Tables, throughout the text, compare various properties of different dielectric materials, many of which are either used or considered for application as ILD. Most of these materials have very high resistivities, specially the polymers, and thus satisfy the initial selection process. It is noted that besides the bulk resistivity, the surface resistivity also plays an important role in determining the dielectric applicability. There are no specific criteria listed for the surface resistivity values. Surfaces are defected and provide fast charge carrier diffusion-paths along themselves leading to significantly lower resistivity compared to bulk. Surfaces become interfaces when a new film is deposited on top and thus become a source of a large number of defects associated with imperfect growth (associated with lattice mismatch, already present impurities and defects, deposition rates, temperature of deposition, involved nucleation and growth mechanisms, etc.). As dielectric films become thinner and thinner, surface to volume ratio increases leading to possibly an important role of the surface and interface electrical conduction mechanisms. For example, a semiconductor–insulator interface (e.g. Si/SiO_2) is known to cause various effects (fixed charge, surface states, interface states, etc.) that affect the metal–oxide–semiconductor (MOS) capacitator properties. Similarly, the interfaces between metal and insulator and between two metallic layers and metal surfaces themselves lead to an increase in the total resistance of the metal [7]. Grain boundaries, which can be considered as interfaces between two crystalline grains, are known to increase the resistance.

Besides surfaces, bulk resistivity is also influenced by: (a) impurities, especially those which can easily ionize under applied bias, for example, water and H_3O^+, H^+, OH^-, Na^+, Cl^- etc.; (b) defects of all types: point, line, area, and volume, some of which result because of lower than bulk density of the film; and (c) a smaller effect associated with the stress that influences the band gap of materials. Also many inorganic dielectrics suffer from non-stoichiometry leading to the generation of higher than expected concentration of vacancies and/or interstitials

(note that such a nomenclature of point defects is strictly true only for crystalline materials, but is arbitrarily used even for non-crystalline solids). Ionic dielectrics (e.g. TiO_2, Al_2O_3) generally have lower electrical resistance than covalently bonded materials, for example, polymers. This is associated with the participation of ions in the current carrying process. Covalently bonded polymers like Teflon and polyethylene have higher electrical resistivities. However, there are polymers which suffer from: (a) continuous charge transfers and exchanges that accompany the associated isomerisms; and (b) the presence of moities like –OH, –F and –Cl that ionize under electrical bias. It is noted that some of the undesirable changes, leading to higher electrical current, are associated with the formation of the metal–polymer interface and the impact of applied field on such an interface. The phenomena are discussed in a later chapter on polymers.

2.2.2 Current leakage and dielectric strengths

Ideally, a dielectric should be a perfect insulator, that is, the resistivity should be infinite. In reality all dielectrics have a finite resistivity leading to a passage of current (I) through the dielectric when subjected to applied voltages. Conduction mechanisms responsible for the current flow through impurity-free dielectric include Poole–Frenkel emission [8] and Fowler–Nordheim tunneling [9]. In the former type, the current density J (current I per unit area) is given by

$$J = C_1 E \exp\left[-q\left(\phi_B - \sqrt{(qE/\pi\varepsilon_{ILD})}/kT\right)\right] \tag{2.1}$$

For Fowler–Nordheim tunneling, J is given by

$$J = C_2 E^2 \exp -\left(\frac{E_0}{E}\right) \tag{2.2}$$

where C_1, C_2, and E_0 are constants, q is the electronic charge, ϕ_B the barrier height, E the electric field, k is Boltzmann's constant, and T the temperature in Kelvin. Note that Frenkel–Poole type conduction is associated with field-enhanced excitation of trapped electrons into the conduction band and is observed only in heavily damaged insulators. Fowler–Nordheim conduction is associated with electrons tunneling from the metal Fermi level into the oxide conduction band, although more complicated tunneling mechanisms are possible. For example, a charge may tunnel from the semiconductor conduction or valence band into an oxide trap. Creation of such a trap could be associated with an oxide defect or an impurity in low concentrations. This charge may then tunnel into one of the insulator bands. It should be pointed out that the above mechanisms are not necessarily independent of each other. One may dominate over the other depending on measurement conditions like applied voltage and temperature. Experimentally, one can determine I–V or J–E curves as a function of temperature. Since Fowler–Nordheim tunneling is essentially independent of temperature while Frenkel–Poole emission is temperature dependent, they can easily be determined by taking measurements over a wide temperature regime.

There are several other conduction mechanisms that can contribute to current through the dielectrics. They are ionic hopping conduction [10], space-charge limited conduction [11], and Schottky effect [12].

The ionic current density is given [10] by

$$J_1 \approx A^1 a^2 \frac{E}{T} \exp\left(-Q_i/kT\right) \tag{2.3}$$

where a is the ionic jump distance A^1 is a constant, and Q_i is the activation energy. Such a mechanism normally dominates in ionic materials.

The space-charge limited conduction is described [11] by

$$J = \frac{8\,\mu k \varepsilon_0 V^2}{9d^3}, \tag{2.4}$$

where J is the current density, μ the carrier mobility, V is the applied voltage, ε_0 the free-space permittivity, and d the dielectric film's thickness. The space-charge limited current is the result of carrier injection in the dielectric when no compensating charge is existing. Equation (2.4) is modified to incorporate the effect of the shallow traps [12]

$$J = \frac{8\,\mu k \varepsilon_0 \Theta V^2}{9d^3}, \tag{2.5}$$

where Θ is the ratio of free and tapped charges. The deviation from Ohm's law is apparently due to the insulator's inability to transport charge as fast as they are generated. In fact, observations of V^n dependence with n as high as 16 has been reported [13–15].

The Schottky effect generates current [16] given by

$$J = A^* T^2 \exp\left[\left(\frac{qV}{4\pi\varepsilon_i d T^2}\right)^{1/2} - \frac{q\phi_B}{kT}\right], \tag{2.6}$$

where A^* is Rechardson constant, ϕ_B the barrier height of the metal on insulator (generally given as the difference between the work functions of the metal and insulator or semiconductor), ε_i the dielectric permittivity, and d the insulator's thickness. No one mechanism explains the complete I–V characteristics, but the conduction is generally associated with Poole–Frenkel effect. Table 2.3 defines various voltage and temperature dependencies associated with all these leakage mechanisms.

The leakage current capability, as discussed above, is generally defined in terms of the maximum voltage (or electric field which is voltage per unit thickness of the dielectric) that an ILD can sustain without leading to runaway currents (usually defined as a given current per unit area, e.g. 1×10^{-6} A/cm^2). At such runaway currents, the dielectric breaks down and discharges. This maximum field is called the dielectric strength given in units of volt/cm. For ordinary applications

Table 2.3 A comparison of leakage mechanisms in dielectrics

Mechanism	Voltage (V) and temperature (T) dependencies[a]
Poole–Frenkel	$V\exp(+2a\sqrt{V}/T - q\phi_B/kT)$
Fowler–Nordheim	$V^2\exp(-b/V)$
Ionic	$VT^{-1}\exp\left(-\frac{Q}{kT}\right)$
Space charge	V^2
Schottky	$T^2\exp(+a\sqrt{V}/T - q\phi_B/kT)$

[a] a is a constant with different values in different cases.

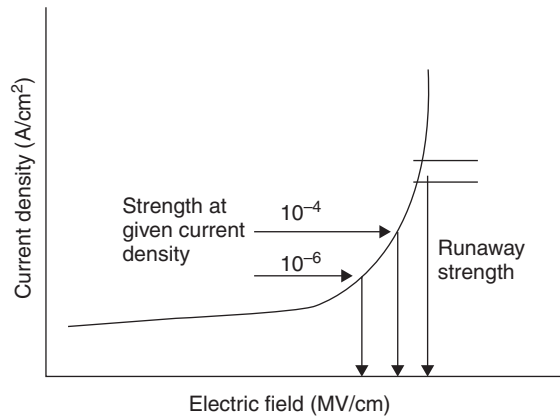

Fig. 2.1 Schematic representation of current density through a dielectric as a function of the applied field.

it is defined for runaway currents that are generally associated with: (a) electron avalanching by impact ionization; and/or (b) Joule-heating breakaway. In semiconductor ILD applications it is defined for a preset current. Figure 2.1 shows a schematic current vs field curve with dielectric strength defined for a runaway current or for a given current density. For ILD applications a dielectric strength of about 2–5 MV/cm is considered adequate.

Dielectric strength appears to be related to dielectric constant (see the following subheading below). The dielectric strength of the inorganic dielectrics is shown in Fig. 2.2 as a function of the dielectric constant [17]. Using this figure, one can obtain the field strength or dielectric constant of the dielectric of interest. Also note that a distribution in field strength is typically observed, with most dielectric failures at lower fields. These values reflect measurements in amorphous dielectric films. Note that SiO_2 has the lowest dielectric constant and the highest field strength; others are unsuitable for use with the ILD but can be useful in applications where higher capacitance per unit area is important. In addition, dielectric breakdown strength decreases with increasing dielectric constant, making materials like TiO_2 and PZT (lead

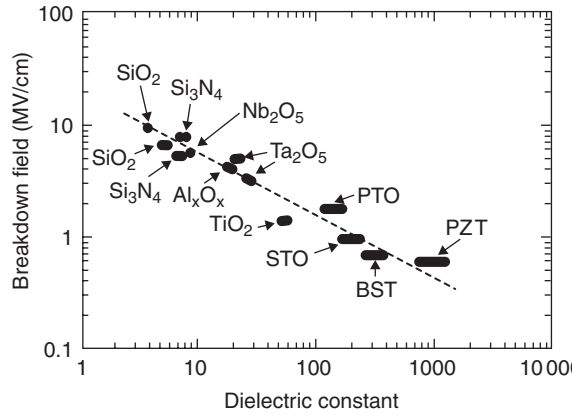

Fig. 2.2 A log–log plot of the dielectric breakdown field (for 10^{-6} A current) as a function of the dielectric constant of the dielectric (from Ref. [17]).

zirconium titanate) unsuitable for applications subjected to high fields (e.g. power ICs for metal–insulator–semiconductor (MIS) gate dielectrics and bypass capacitors).

Wu *et al.* [17] measured a change of more than 5 orders of magnitude of leakage current density in tantalum oxide films (deposited by a dc reactive sputtering technique) with a dielectric constant ranging from 20 to 45 and concluded that the leakage current under an external bias 'is controlled by the Poole–Frenkel *E*-field induced lowering effect regardless of the dielectric constant of the film.' They also concluded that 'the leakage current is also controlled by the Poole–Frenkel potential barrier, which is inversely proportional to the dielectric constant,' suggesting an intrinsic limit to the minimum leakage current one can achieve at a given field strength for high-dielectric-constant films. One would thus expect that the higher the dielectric constant of the film, the lower the breakdown field strength (defined at a fixed current density).

Table 2.4 lists the known or estimated breakdown fields (together with density and other electrical properties of interest) of several inorganic dielectrics. It is noted that there is a lot of discrepancy in the reported values of the breakdown field and resistivity. Values listed in Table 2.4 are best-guess estimations from published values [18–24]. Generally, and in absence of easier mode of breakdown, for example, trapped water or mobile ions, the organic dielectrics have higher breakdown voltages when compared to the inorganic materials.

Finally, it is noted that the dielectric breakdown field strength (defined as the runaway strength in Fig. 2.1) has a dielectric-thickness dependence and decreases with the thickness. The lowering of the field strength at higher thickness is associated with the defects and asperities and also with generally low thermal conductivities of the dielectric, the Joule heating effectively raising the temperature more in thicker dielectrics than in thinner ones. Higher the temperature, lower is the field strength, and the drop in the field strength at high temperatures could be very large.

Table 2.4 Densities, best-known band gaps, breakdown voltages (or field strengths), dielectric constants, and resistivities of inorganic dielectrics[a]

ILD materials	Density (g/cm^3)	Band gap (eV)	Breakdown voltage (MV/cm)	Dielectric constant[b] (at 1 MHz)	Resistivity[c] ($\mu\Omega$ cm)
BN	2.1	3, 4.6	–	7.1	1900 at 2000°C
Diamond	3.52	5.4	0.01–1.2	5.87, 5.66	–
MgO	3.58	7.3	–	9.65	2×10^{14} at 850°C
Al_2O_3	3.97	2.5–3.6	0.3–4.5	9.34,11.54	10^{22}
Al N	3.26	4.3	0.1–4	9	–
SiO_2[d]	2.32	~8	1–10	3.9	10^{21}–10^{22}
Si_3N_4[d]	3.2–3.4	3.9	5–8	7.5	~10^{20}
TiO_2	4.26	3–3.7	~2	86, 170	1.2×10^{10} at 800°C
Cr_2O_3	5.21	4.8	–	13.3, 11.9	1.3×10^{9} at 350°C
Y_2O_3	5.01	–	–	10	–
ZrO_2	5.75	2.0	–	12.5	1×10^{12} at 385°C
Nb_2O_5	4.47	2.4	~5	50	–
La_2O_3	6.51	5.4	–	21	–
CeO_2	6.86	–	–	7.0	6.5×10^{10} at 800°C
HfO_2	9.68	–	–	–	5×10^{15} at 400°C
Ta_2O_5	8.2	–	~5	24, 30, 65	–

[a]Collected from references cited in Ref. [18].
[b]More than one value indicates different phase or different measured direction.
[c]At or near room temperature unless specified.
[d]Amorphous films.

2.2.3 Polarization and charges in the dielectric

When an electric field is applied across a dielectric, polarization sets in the dielectric or in other words field induced dipoles are created. In addition, all dipoles (permanent dipoles already existing in the material plus field-induced ones) become aligned with applied field. The field induced charge distribution, in the space of the dielectric medium, is thus a result of various factors called: (a) electronic; (b) atomic or ionic; (c) orientation; and (d) space-charge polarizations. They cover all types of existing and field-induced charge distribution and alignments. If one defines a total polarizability as α it can be written as a sum of α_e, α_i, α_o, and α_s representing, respectively, the above factors. The electronic and ionic polarizations are associated with the applied field induced displacement of electrons in an ion, with respect to nucleus and of negative and positive ions in an ionic dielectric, respectively, so that effectively new dipoles are

created. For smaller ions and molecules, as in many polymers, the ionic polarization contribution is less dominating, leading to lower α. The orientation and space-charge polarizations are, on the other hand, associated with the field-induced alignment of existing dipoles in the material and with the existing mobile charges at the defect sites, for example, interfaces, grain boundaries, and dislocations. Classically, the total polarizability is given by the Clausius–Mosotti equation [25]:

$$\alpha = \frac{3}{4\pi N}\left(\frac{\kappa - 1}{\kappa - 2}\right) \tag{2.7}$$

where N is the number of molecules per unit volume and κ is the dielectric constant.

Dielectric constant, characteristic of the dielectric material across which an electric field is imposed, is defined as:

$$\kappa = \frac{\varepsilon}{\varepsilon_0} \tag{2.8}$$

where ε and ε_0 are the respective dielectric permittivities of the dielectric under consideration and of the vacuum. ε_0 has a value of 8.55×10^{-14} F/cm. Note that dielectric constant κ is also known as relative permittivity and has, therefore, a value of 1 for vacuum.

Equation (2.7) leads to a definition of the dielectric constant in terms of the polarizability:

$$\kappa = \frac{3}{1 - (4\pi N\alpha/3)} - 2 \tag{2.9}$$

Notice that the higher the N and/or α the higher is κ. The larger is the molar volume the lower is N and thus lower is κ. Thus, to obtain or design lower κ, materials with larger molar volume and lower polarization becomes necessary. As noted earlier, ILD made up of smaller atoms/ions (e.g. C, B, H) have comparatively lower α and thus have lower κ. For oxides, this tendency is clearly reflected in a plot of permittivity, ε, as a function of the mean atomic number per molecule, showing that permittivity increases with atomic number [26]. Among the organic functional groups, –F has the lowest and –OH has the highest molar polarizations although both have similar molar volume. Table 2.5 lists some of the organic functional groups with their molar polarizations and molar volumes [27]. It is also known that the polarizability increases in the order of single, double, and triple bonds, as one finds in many organic polymers.

Also note that the permittivity and thus the dielectric constant has a very small temperature dependence, with a temperature coefficient in the range of −200 to +200ppm/°C [26].

In most applications at or near room temperature ±100°C, the temperature-induced variation in the permittivity or the capacitance is negligible. Table 2.4 lists the dielectric properties of interest for the inorganic dielectrics. Many polymer types have been used or formulated for

Table 2.5 Molar polarization and molar volume of various functional groups [27]

Functional groups	Molar polarization φ	Molar volume V
–F	1.8	10.9
$-CH_3$	5.6	23.9
$-CH_2-$	4.7	15.9
	25.0	65.5
	15.0	23.0
	10.0	13.4
–O–	5.2	10.0
–OH	20.0	9.7

use in the microelectronic products and more recently for use as an ILD: polyurethanes, epoxies, phenoxies, silicones, polyimides, fluorocarbons, polyxylenes, polyesters, polyvinyls, polystyrenes, acrylics, diallylphthalates, polyamides, phenolics, and polysulfides. The out-of-plane dielectric constant, measured at 1 MHz ranges from a low of 1.9 to as high 6 or 7. Also a variety of amorphous C (with or without F), F and/or C containing SiO_2, xerogels and aerogels, porous materials with a dielectric constant in the range of as low as 1.01 to about 3.5 have been created and investigated for application as an ILD. Table 2.6 lists a few polymers along with their well-established dielectric properties. It is noted that although many ILD materials with desired κ values in the range of 1.5–3 have been formulated and produced, their applicability has not been possible due stringent requirement of the processability and reliability (see further discussion in the following subsections).

The magnitude of the charge that can be stored between two conductor plates separated by a dielectric is given as

$$Q = CV \tag{2.10}$$

where V is the applied voltage and C is the capacitance given by

$$C = \varepsilon\frac{A}{t} = \kappa\varepsilon_0\frac{A}{t}. \tag{2.11}$$

A and t are the area and the thickness of the dielectric between two conductor plates, respectively. Measurement of the dielectric capacitance provides direct means to obtain κ.

Higher dielectric constant means higher capacitance and thus higher charge stored between conductor plates, a necessarily required characteristic of the insulator in an MIS capacitor, for example, a gate capacitor in a MOSFET. However, higher capacitance and, thus higher

Table 2.6 Best-known properties of several low-κ materials[a]

Dielectric	κ	tan δ	T_g (approx.) (°C)
α-C:F	2.2–2.6	0.0002	400
BCB	2.6		300
Fluorinated polyimides	2.3–2.8		
Fluoromethylene cyanurates	2.3–2.7		
Fluoroacrylics	2.1–2.4		
Fluoroallyl siloxanes	2.3–2.4		
Polytetrafluoro ethylene	2.0		
Perfluorocyclobutane ethers	2.4		
Tetrafluorocyclophane	2.4		
Flare	2.6–2.8		>400
Polynorbornene	2.2		365
MSQ	2.6–2.7		>400
MSQ/HSQ hybrid	2.5–2.6		
Teflon AF, Cytop	2.24		<240
Polystyrene	2.6		<100
Styrene copolymers	2.6–2.8		
Sesquisiloxane	2.7		200
Poly (phenyl) oxide	2.6		150
Polyethylene	2.3		-80
Polypropylene	2.3–2.4		-10
Parylene-N	2.6–2.8		350
Parylene-F	2.2–2.3		450
PVC	3.3		
Polyisobutylene	2.2		
Teflon	1.9–2.1		300
SILK™	2.65		

[a]The list is not, by far, complete. See other materials mentioned in other chapters of this book. Also most of these polymers can not be considered for ILD applications because of the lack of high T_g and reasonable mechanical strength.

dielectric constant, is undesirable for an ILD because that causes a lowering of the circuit speed. Circuit speed is determined by a quantity RC where R is the resistance of the associated interconnecting wires and C is now the ILD capacitance (see Chapter 1). The nature of charges that are trapped in the dielectric and their impact as trapped and/or mobile oxide charge on both the C–V and I–V behaviors, have been discussed elsewhere by many authors (see, e.g. Refs [16, 28] and other similar texts). A typical C–V plot may look like any of the plots in Fig. 2.3. Figure 2.3(a) shows an ideal C–V behavior. Figure 2.3(b) indicates a stretching associated with the interface traps whose occupancy depends on the applied gate voltage and Fig. 2.3(d) shows a combined effect of the interface states and the flat band shift. Figure 2.3(c) depicts a shift, parallel to the ideal

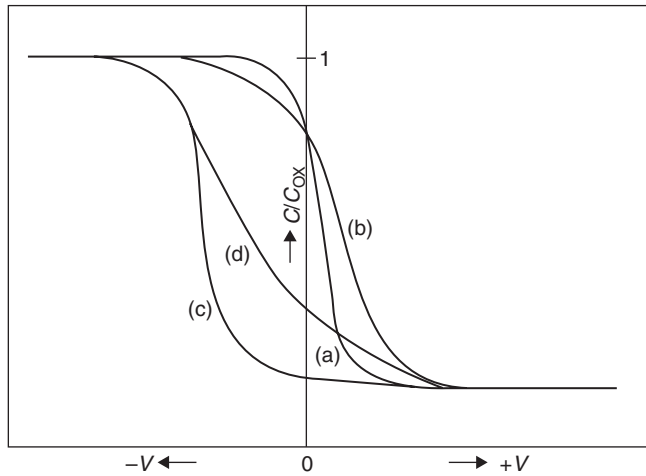

Fig. 2.3 Typical *C–V* curves for ideal (a) and non-ideal behaviors (b), (c), and for a MOS or MIS capacitor on p-type semiconductor (d).

curve, due to a combination of one, two, or all of the following: a difference between the work functions of the metal and semiconductor, mobile and trapped charge densities in the insulator, and semiconductor–insulator interface related charge densities. Thus, a careful study of the *C–V* behavior of an MIS yields a lot of useful information about the insulator. Generally, the insulators (other than thermal SiO_2) and especially polymers provide a poor interface between the insulator and silicon used as semiconductor. To avoid the interface related issues, a practice has been adopted to use a thin layer of thermally grown SiO_2 on Si prior to depositing the insulator under investigation.

Because polarization depends on the structure of the dielectric and the structure can be anisotropic in terms of: (a) spacing between atoms, molecules, or atomic moieties; and (b) number density of these atoms, molecules, or atomic moeities, the dielectric permittivity ε or the dielectric constant κ can be anisotropic. Anisotropicity of κ causes a problem in application of a dielectric as an ILD or as an optical waveguide.

2.2.4 Dielectric dissipation and loss (ac behavior)

When a perfect dielectric is subject to an ac voltage, the voltage lags the current by 90°. However, in a regular dielectric the lag is not 90° but $(90 - \delta)°$ where δ is now called the dielectric loss angle and this behavior leads to a power loss, generally as heat. The dissipation of energy is now described by the terms: (a) dissipation factor that equals tan δ; and (b) dielectric loss factor that equals κ tan δ. The total power loss can be calculated by the equation

$$\text{Power loss (watts)} = 5.56 \times 10^{-11} E^2 f \nu \kappa \tan \delta \tag{2.12}$$

where E is the applied field strength in volts per meter, f the frequency in Hertz, and ν the volume. To minimize the energy dissipation from a given material, one must therefore seek the lowest δ. Finally, it is noted that under ac conditions: (a) polarization and loss are both frequency dependent; (b) at very high frequencies ($> 10^{12}$ Hz) only electronic polarization dominates; and (c) amorphous dielectric materials, in general, polarize at higher frequencies than the crystalline materials of same composition.

2.3 Mechanical properties

The reliability of the semiconductor/microelectronics products is not only related to electrical properties but also to mechanical properties. The physical failures, for example, cracks, buckling, lack of adhesion and thus peeling, stress-related effects specially adhesion failures and stress migration in metallic films in contact with the ILD, fracture during chemical–mechanical planarization, are all associated with the mechanical properties. Table 2.1 lists the mechanical properties of concern together with those parameters (e.g. thickness of the film) that affect these mechanical properties. Many of the properties are interrelated and depend on the process parameters as well. Thus stress, adhesion, fracture and crack resistance, hardness, and stress-migration are process and materials dependent. At the same time, in most cases their affect on the reliability depends on the surroundings. For example, a SiO_2 film may have a different condition of stress on Al than that on Cu with or without an adhesion promoter. Similarly whether the film is subjected to a high or low temperature during the film deposition and subsequent processing will determine the mechanical behavior.

Besides the interest in the stability of the films and the structures they are part of, the understanding of the elastic behavior, the strength and plastic behavior, the micro- and macrostresses, and of the correlation between the thin film behavior and properties to the bulk properties are of considerable interest. The effect of stress on the band gap of insulators and generation of effects such as piezoelectricity are of considerable importance.

2.3.1 Stress

'A body which is acted on by external forces, or, more generally, a body in which one part exerts a force on neighboring parts, is said to be in a state of stress. If we consider a volume element situated within the stressed body, we may recognize two kinds of forces acting upon it. First of all, there are body-forces, such as gravity, which act throughout the body on all its elements and whose magnitudes are proportional to the volume of the element. Secondly, there are forces exerted on the surface of the elements by the material surrounding it. These forces are proportional to the area of the surface of the element, and the force per unit area is called the stress' [29].

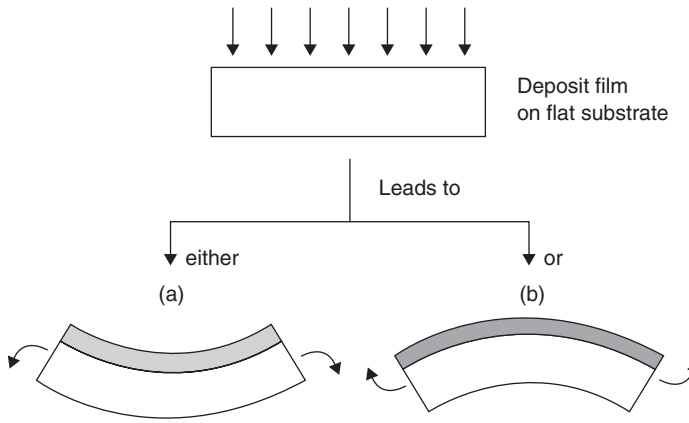

Fig. 2.4 Schematic representation of (a) tensile and (b) compressive stresses in the films deposited on a substrate. Arrows at the ends of film/substrate composites indicate tendency of the substrate to become flat (as it was before the film deposition).

The stress is compressive or tensile if the material under stress will expand or contract, respectively, when the forces causing the stress are eliminated. By convention compressive stresses are considered negative and tensile stresses are considered positive stresses. When a film is deposited on a flat substrate, interacting forces sometimes lead to bending of the substrate to counter the forces resulting from the film deposition. This leads to a stress condition in the film (and opposite stress condition in the substrate) as shown schematically in Fig. 2.4. In Fig. 2.4(a), the substrate will likely become flat by bending in the direction of arrows thus making the film (in equilibrium) tensile. In Fig. 2.4(b), the reverse is true and the film (in equilibrium) is compressive.

When the stresses are high, in extreme cases tensile stress leads to breaks or cracks in the film and compressive stress lead to buckling up or curling. The phenomenon of film cracking or buckling up not only depends on the magnitude of the stress but also on the adhesive forces at the film–substrate interface. Thus, films with stronger adhesion to the substrate will sustain larger stresses prior to the failure. However, there are other reasons for the film lifting or cracking, which are related to surface asperities and cleanliness, impurities, and environmental effects. The stress condition is also influenced by the temperature cycle to which the film–substrate couple is subjected. This effect is related to the difference in the thermal expansion behaviors of the film and the substrate.

Excluding any external influences, the total stress, σ, is a sum of so-called instrinsic stress, σ_i, and the thermal stress, σ_{th}, that is,

$$\sigma = \sigma_i + \sigma_{th}. \tag{2.13}$$

The intrinsic stress is the result of one or more of the following factors: (i) the lattice mismatch between the substrate and the film; (ii) the film microstructure and purity; (iii) the defects in

the film; (iv) the volume changes associated with chemical or metallurgical interactions; (v) the anisotropic growth; (vi) the surface effects such as surface tension; and (vii) the electrostatic effects. For polycrystalline films, the lattice-mismatch contribution to the film intrinsic stress is very small, and the total intrinsic stress is generally considered to be independent of the substrate type or orientation. Thus, as also mentioned earlier, the stress and specifically intrinsic stress is a strong function of the deposition methods and parameters which control most of the above factors.

Intrinsic stress, in many cases, has been minimized or even eliminated by engineering the growth process. However, thermal stress, σ_{th}, which is a function of the difference in the thermal expansion coefficients of the film (α_F) and the substrate (α_S) and of the difference in the growth or anneal temperature (T_2) and the use (or measuring) temperature (T_1), will be finite as long as ($\alpha_F - \alpha_S$) and ($T_2 - T_1$) are not zero. Quantitatively

$$\sigma_{th} = \frac{E_f}{1-\nu_f}\left[\int_{T_1}^{T_2}(\alpha_F - \alpha_S)\mathrm{d}T\right], \tag{2.14}$$

where E_f and ν_f are Young's modulus and Poisson's ratio of the film, respectively, and T is the temperature. The quantity in the square brackets determines the thermal strain. For α values that are independent of temperature one can write

$$\sigma_{th} = \frac{E_f}{1-\nu_f}(\alpha_F - \alpha_S)(T_2 - T_1). \tag{2.15}$$

Generally, α is not independent of temperature. For example, α_{si} goes from $2.6\times10^{-6}\,°C^{-1}$ at 25 °C to ~$3.3\times10^{-6}\,°C^{-1}$ at 900°C. However, for most applications, Eq. (2.15) yields excellent results. Equation (2.15) can be used to determine both $E_f/(1-\nu_f)$ and α_F of the film material by measuring σ_{th} vs temperature for the same film on two different substrates.

It is also noted that many insulator films, in the as-deposited state, do not have bulk densities. On annealing changes in the densities of the films take place due to densification and/or chemical interactions. Such changes considerably affect the state of the stress in the films. For example, a low-pressure chemical vapor deposited (LPCVD) films may be in a near zero stress condition. On annealing, depending on temperature, it may become tensile or compressive [30]. On the other hand, a plasma-enhanced CVD (PECVD) or thermal oxide are in a state of compression and show stability in this room temperature state of stress during annealings.

For ILD applications, assuming that we are able to minimize or even eliminate the intrinsic stress by optimizing the film formation process, thermal stress is the most important. To tailor the thermal stress, materials must be carefully chosen with low values of Young's modulus and thermal expansion coefficient, and temperature excursions must be minimized. Table 2.7 compares these properties for a variety of inorganic and organic ILD materials. It is clear that organic ILD materials will produce considerable low values of thermal stress in spite of the fact that their coefficients of thermal expansion are large.

Table 2.7 Young's moduli (E) and coefficients of thermal expansion (α) of selected ILD materials at or near room temperature.

Dielectric	E (GPa)	α (ppm/°C)
INORGANIC MATERIALS[a]		
Diamond	1049	1
Al_2O_3	375	6–8
AlN	294–343	5
BN	83[b]	1–13
HfO_2	–	5–6
La_2O_3	–	6
MgO	210	12
SiO_2 (amorphous)	52–111	0.5
Si_3N_4	207–310	1.5–3.7
Ta_2O_5	–	0.8
TiO_2	88	8
ZrO_2	150–210	6–9
POLYMERIC MATERIALS[b]		
Acetals	3.1	
Acrylics	2.9	
Cellulosics	3.4–28	
Polyamides	2.8	
Polycarbonates	2.4	
Polyethylene	0.17–0.83	
Polypropylene	1.4	
Polystyrene	3.1	
Polyvinychloride	2.8	
Teflon	0.41	~70
Polyimide siloxanes	0.95–1.8	70–110
Paralyne-N	2.4	50–70
Paralyne-F	2.4	28–36

[a]From Refs [18, 31, 32].
[b]From Ref. [33].

The stress in the film may cause delamination. The force per unit length, σt, where t is the thickness of the film, determines this behavior. Thus, whereas stress is generally considered to be independent of thickness, the delamination force is thickness dependent. For packaging applications where insulator thickness are in the range a few tens to a few hundreds of micrometers, the delamination is of very serious concern and even polymers can delaminate. Thus, for many years there has been an emphasis on very low coefficient of thermal expansion (CTE) of

the interlayer dielectrics, even in ILD applications such that thermal and thus the total stress is the lowest possible.

Stress-migration in metallic films, in contact with ILD, was mentioned earlier. Stress-migration is a result of stress-induced preferential migration of the metallic atoms leading to void or slit generation in metallic interconnections [34]. Metallic films on ILD are generally in a state of tension when $\alpha_m > \alpha_{ILD}$, for example, Al or Cu on SiO_2. When covered with an ILD film with CTE lower than the metal, the tensile stress increases in the metal. To relieve the tension, a vacancy migration toward grain boundaries occurs resulting in a void formation. Thus, lower stress in the dielectric film, as a result of lower thermal mismatch (i.e. lower $\alpha_m - \alpha_{ILD}$), leads to more reliable interconnections.

2.3.2 Adhesion

Adhesion to the substrate and to surrounding walls is of utmost importance. In IC (and many other) applications, a film is said to adhere well to the substrate if the film–substrate or the substrate–film interface is not physically affected during the IC fabrication or service even when subjected to a reasonably low level of stress. Fundamentally, the adhesion is a measure of all interatomic-interactive forces across the film substrate interface. One can group these forces in two categories. In the first, the bonding across the interface is more or less physical and is caused by electrostatic forces and/or van der Waal forces. Atoms, in materials across the interface, are held to each other by electrostatic forces when they are ionized with opposite polarities and thus are attracted. On the other hand, atoms across the interface can also be attracted to each other even when their electron shells are intact but polarized. Polarization creates dipoles that align to cause electrostatic bonding (van der Waal type) across the interface. One can estimate the adsorption energy E_{ad} and hence the adhesion strength using atomic polarizabilities and characteristics vibrational frequencies or ionization potentials [35]. E_{ad} is given as:

$$E_{ad} = -\frac{N\pi}{4}\,\frac{p_1 p_2}{S^3}\,\frac{V_1 V_2}{V_1 + V_2} \tag{2.16}$$

where N is the number of adsorbent atoms per unit volume in the substrate, p_1 and p_2 the polarizabilities of the film and substrate atoms, respectively, V_1 and V_2 their ionization potentials, and S the equilibrium distance of the condensate atom from the substrate surface [35]. Atoms and molecules with large polarizabilities and ionization potentials (or vibrational frequencies) have greater adhesion strengths.

Considerably stronger adhesion is affected by the formation of chemical bonds across the interface. The stronger the chemical bonding the larger will be the adhesion strength. A classic comparison can be made between the lack of chemical adhesion in the case of Au, Cu, or W films on SiO_2 surface and the strong chemical adhesion between aluminum film and SiO_2 surface. Au, Cu, or W are not able to reduce SiO_2 and form chemical bonds. Aluminum reduces

SiO_2 to form strong chemical bonds with oxygen. In most cases a prediction of the possibility of chemical bonding across the interface can be readily made by comparing the free energies of formation of the possible compounds (chemical bonds) that would result by interaction between materials across the interface. Titanium films are commonly used as adhesion promoters mainly because titanium readily forms compounds with oxygen, nitrogen, carbon, and many other elements with considerable lowering of the free energy. This lowering of the free energy per unit interface area determines the strength of chemical adhesion.

The presence of impurities, surface roughness, reactive environment, temperature, and overlying coatings will affect these interfacial bonding forces and the adhesion. To ensure good adhesion there must be: (i) a strong interatomic bonding across the film–substrate interface; (ii) an absence of easy deformation or fracture modes and of the reactive environment that produces stress; (3) a low level of film stress; and (iv) an absence of the long-term degradation modes [36].

In absence of factors (ii) and (iv) the failure of the film or its decohesion depends of factors (i) and (iii) only. Campbell [37] has calculated that stress of about 5×10^9 dyn/cm^2 will be necessary to overcome an adsorption energy of 0.2 eV for a simple case of moving atoms along the (111) surface of an fcc structure from one potential minimum to the next by the easiest possible route. However, the film decohesion also depends on the nature of the film and substrate materials. Evans *et al*. [38] have broadly defined modes of decohesion, depending on the interfacial bonding and film and substrate ductility or brittleness. They have also attempted to quantify the film decohesion process by defining a critical non-dimensional parameter called decohesion number

$$\Omega_c = K_c \, \sigma_0^{-1} h^{-1/2}, \tag{2.17}$$

where K_c is the fracture resistance, σ_0 the stress in the film, and h the film thickness. The equation is analogous to one commonly used to quantify the fracture process by defining fracture toughness as

$$K_{1c} = \gamma \, \sigma_f \sqrt{\alpha \pi}, \tag{2.18}$$

where γ is the non-dimensional parameter, σ_f is the applied stress at failure and α the length of a crack. It is assumed that the specimen thickness (being tested for fracture-related failure) is significantly large compared to the crack dimensions.

In Eq. (2.17) both Ω_c and K_c depend on the sign of σ_0, the ductility of the film and substrate, and their relative elastic modulii. Evans *et al*. [38] have tried to further the understanding of decohesion by correlating Ω_c to the film and substrate elastic properties, substrate thickness, and yield strength. However, further development is clearly needed to formulate the underlying mechanisms. Both Ω_c and K_{1c} are limits to be avoided.

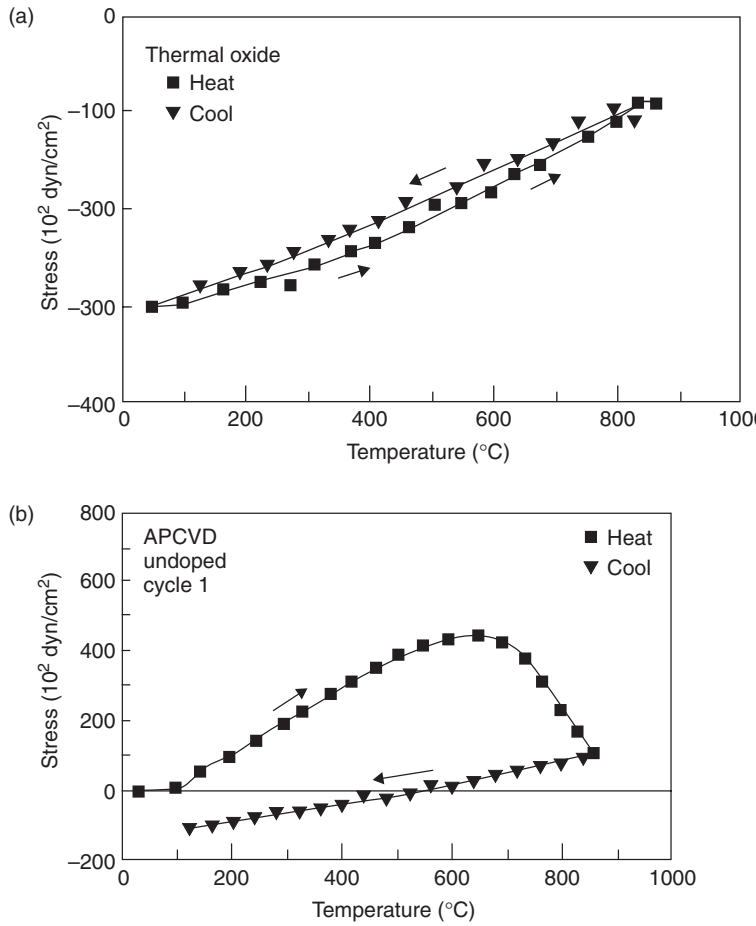

Fig. 2.5 Stress as a function temperature (*in situ* measurements) during heating/cooling cycles of (a) thermally grown SiO_2 films and (b) APCVDSiO_2 films (from Ref. [30]).

2.3.3 Other Properties that affect mechanical stability of ILD films

As listed in Table 2.1, under mechanical property requirements, film thickness uniformity, high tensile modulus and high hardness, low shrinkage and weight loss, and high crack resistance are other characteristics that affect the performance and mechanical stability of ILD films. Many of the undesirable behaviors result from uncontrolled/unoptimized depositions. Figure 2.5 shows stress in the SiO_2 films as a function of the annealing temperature (*in situ* measurements) during heating and cooling cycles of: (a) thermally grown SiO_2 film; and (b) atmospheric pressure CVD (APCVD) film [30]. It is clear that thermal SiO_2 films was stable where as APCVD film went through material changes. Careful chemical analysis and density measurements showed a presence of water in the as-deposited films and approximately 5% porosity. On annealing the

films became dense and lost practically all water, making the film behave like thermal SiO_2 (Fig. 2.5(a)). Water entrapment, in the as-deposited films, can be the result of the oxidation of silane in oxygen or a oxygenated gas and a low temperature deposition. LPCVD and PECVD films show significantly less water content and significantly improved stress–temperature behavior [29].

A non-uniformity in the film thickness results not only in difficulties in further processing of the film but also in non-uniform stress characteristics across the entire surface leading to a variation in delamination forces. Excessive shrinkage and weight loss (as discussed above) that may occur with many organic ILD materials, on the other hand, may lead to cracks in the film. Pores and cracks become fast diffusion pathways for metal leading to leakage and eventually shorts between two levels of metal interconnections.

Since most of the ILD applications will require CMP of ILD films, higher tensile modulus and hardness become important criteria for ILD films. Although CMP induces chemically aided grinding or fracture, a high crack resistance is necessary so that CMP forces do not induce deep or long cracks in dielectric films.

2.4 Chemical and electrochemical properties

Among the chemical properties listed in the Table 2.1, some determine the processability of the dielectric materials and others define their reliability during processing and actual use. High etch selectivity and the etch rate in a given chemical or in a given reactive gas used in dry reactive ion etching (RIE) depend significantly on the density and the impurity content (and type) of the ILD. Moisture sensitivity, solubility of water in the films, and low gas permeability are all dependent on density and impurity content and type plus the physical structure that is a basic characteristic of the ILD material influenced only by the preparation method and post-preparation annealing and densification treatments. A thermal oxide grown at 1000°C has an etch rate of 2.5 nm/min in 100 : 1 H_2O : HF solution, compared to 3, 6, 40, and 3–4 nm/min for CVD oxide films deposited at 700, 450, 200°C (in plasma CVD), and 390–400°C (in PECVD), respectively [39].

Analysis of these SiO_2 films clearly show a strong correlation between the decreasing density and increasing etch rate in HF solutions and the increasing concentration of hydrogen containing species (e.g. –H, –OH, H_2O, H_3O^+, even H_2 and particularly broken or unbroken silane molecules) [40–45]. On annealing these CVD oxides at temperatures above 800°C, a densification takes place and the concentration of H-containing species goes down by a few orders of magnitude below the detection limit of the analysis. Both the density and the concentration of H-containing species, in these annealed CVD oxides, are very similar to those of thermal oxides. These H-containing species cause both the electrical instabilities and the unexpected tensile stress behavior as discussed earlier and in many cases are also responsible for metallic corrosion and underlying device instabilities.

Other impurities like phosphorus, boron, fluorine, germanium or arsenic have been intentionally added to SiO_2 to impart certain desired properties (e.g. barrier against sodium in-diffusion

and lower softening temperatures so that a flow can be induced to impart improved surface planarity). They all lead to considerable changes in both the chemical/dry etch rates, electrical/mechanical properties, and in moisture absorption behavior [46, 47]. It is noted that the CVD oxides use a variety of: (a) source-gases: dichlorosilane (SiH_2Cl_2), silane (SiH_4), or TEOS (tetraethylorthosilicate $Si(OC_2H_5)_4$); and (b) oxidizers: nitrous oxide (N_2O), oxygen, or ozone (O_3). Thus deposited films may contain small amounts of chlorine, nitrogen, and/or carbon. Historically, several attempts have been unsuccessfully made to use deposited oxides instead of thermal oxide used for device isolation or as gate. The failure is related to poor silicon–oxide interface and trapped charges in the CVD oxide, all associated with the chemically produced impurities, as discussed above.

For low-κ organic materials, similar problems, associated with incomplete polymerization, entrapped decomposition fragments, residual solvent, water retention, and dielectric decomposition associated with high temperature and ion-bombardment (e.g. during ion implantation and/or RIE) treatments, lead to a variation in the ILD properties. As discussed in the section on electrical properties, the chemistry of the polymers determine the dielectric constant and its stability during processing and subsequent use. Unsaturated bonds, isomeric transformations, halogenated bonds, phenyl vs alkyl groups, molecular weight, stretching of polymers and their crystallization, extent of cross-linking, and (during this film formation) macromolecules alignment parallel to the substrate, all determine the final applicability and storage life of a given polymer. In addition interactions with underlying and overlying materials, particularly metals is very important. For example, Al, which is considered a stable metal on SiO_2, causes considerable electrical instabilities (at least on some polymers) associated with: (a) chemical interaction; or (b) migration of Al in the polymer when subjected to electrical bias [48, 49]. It has been shown that the flat-band voltage shifts in the *C–V* plots of the metal/polymer capacitors are related: (i) to the tendency of oxidation as defined by the formation free energy of the metal oxides and/or; (ii) to the first ionization energy of the metals. In an investigation of the electric properties of a metal on an organic semiconductor, Hirose *et al.* [50] reported: (a) ohmic behavior with reactive metal (In, Al, Ti) contacts; and (b) interfaces, abrupt and free of gap states, with non-reactive metal (Ag, Au) contacts.

Although SiO_2 does not have significant moisture absorption tendency, most polymers have relatively stronger affinity for water. Also the permeability of water through many polymers is high. This had led to the use of: (a) hermatically sealed packages; and (b) low temperature PECVD silicon nitride as the moisture barrier on the chip.

All ILD films will be subjected to RIE and CMP. Most polymers are relatively easy to RIE but difficult to CMP. The latter behavior is due to: (a) polymer's softness; and (b) polymer's inability to dissolve in common solvents that are used to form CMP slurries. Thus, a CMP process has to be specifically developed for a given polymer chosen as an ILD. In contrast, both RIE and CMP of SiO_2 are established and now well controlled. Both RIE and CMP, however, chemically modify the ILD-surface, modification being associated with plasma damage in the

case of RIE and mechanical abrasion and pressure in the case of CMP. In both cases, a post-process anneal restores the original surface behavior.

It is important to point out that the insulator surfaces, when immersed in a liquid, are usually charged by the adsorption of the ions from solution. This charge on the surface in liquid is balanced by an equal but oppositely charged layer in the adjacent liquid, resulting in a so-called electric double layer [51]. In addition, ions in solution are normally solvated (i.e. they also attract polar water molecules). The double layer formation affects how easily the reactants can approach the surface and products can move away from the surface, in effect controlling the chemical etch behavior and thus requiring the agitation to minimize this effect. This electrostatic charge behavior is also important particularly during CMP of ILD materials. The abrasive used in the CMP process is also an insulator (like SiO_2 or Al_2O_3 particles). They may as well form the electric double layer and thus experience an electrostatic interaction with charges at or near the ILD surface immersed in the same liquid. In a liquid with ions and molecules under constant thermal motion, one expects a diffused zone of charges in the solution and a compacted layer on the solid surface. When the liquid, the particle, or the surface is in motion (with respect to each other), the compacted layer on the solid surface moves with the surface movement whereas the diffused zone of charges in liquid moves with the liquid. The boundary between the two regions of charges is a shear plane at which an electrokinetic potential or zeta potential is defined. Zeta potential is obviously a function of the chemistry of the solution and its pH. When the sign of the zeta potential of the particle and of the surface (of ILD, for example) is the same and the absolute value is large, a strong repulsion occurs between the particle and the surface, leading to particle separation from the surfaces of interest and eventually: (a) to cleaning; and (b) to lower abrasion rates in case of CMP [52–54]. Besides zeta potential, another electrochemical parameter called isoelectric point (IEP) has been defined as the pH at which the net surface charge is zero. IEP values have been listed for many insulator/ceramic materials [55]. Generally accepted values of IEP for SiO_2 and Al_2O_3 are 2.2 and 8.9, respectively. Charging of the surfaces and its impact on dry reactive ion etching have also been found to occur, especially for the insulating ILD [56].

Polymeric surfaces are expected to behave in a manner similar to inorganic insulator surfaces. For example, polyvinyl alcohol showed a zeta potential behavior similar to that of SiO_2 [54].

Also, there is considerable interest in porous dielectrics. Both inorganic (mainly SiO_2 based) and organic materials with varying porosity are being created and evaluated. By adding these pores, the volume density, mechanical strength, and in some cases electrical dielectric strength and thermal conductivity decreases together with the desired drop in the dielectric constant. Porous materials must be very carefully evaluated not only for their dielectric properties but also for mechanical strength, adhesion, trapped species (e.g. water) in the pores, chemical stability and entrapment during deposition and processing and interactions with the metal and surrounding materials. An understanding of the dielectric properties of the porous materials in terms the pore size, pore-size distribution throughout the volume of the material, and the

percent porosity (and density of the films) is very essential to produce reproducible films for ILD applications.

2.5 Thermal and thermodynamic properties

Thermal stability of ILD materials determines their deposition, processing, and reliability. We are not only concerned with the high-temperature exposures during various deposition, etching, and thermal treatments required to correct and stabilize device performance, but also with Joule heating of the interconnects leading to considerable amounts of power dissipation in the ILD and through the ILD into the other surroundings. Such thermals excursions, including those due to devices in the semiconductor, are projected to dominate the interconnection performance and their design in future high-performance circuits. Thus, thermal properties: CTE, thermal shrinkage, specific heat capacity, thermal conductivity, melting points, and glass transition temperature, T_g, become very important when determining the usefulness of an ILD material. ILD films are surrounded by the metal interconnects carrying electric currents as high as 10^6–10^7 A/cm^2. Heat is generated in the metal due to the passage of current and this heat is then dissipated to the surrounding dielectric and through the dielectric to the rest of the chip and chip-surrounds. The dissipation of heat is a function of the thermal conductivity of the metal and the temperature gradients and thermal conductivity of the surrounding dielectric and the effective cooling (leading to enhanced thermal gradients) employed to cool the chip. There is an effective temperature rise in the ILD film depending on its heat capacity and the rate at which it looses the heat, determined also by ILD's thermal conductivity. One can compare the ILD materials (leading to those with lowest temperature rise) by imposing an artificial adiabatic condition under which the ILD receives a thermal energy Q and no dissipation away from the dielectric into its surroundings is allowed. The adiabatic temperature rise ΔT is then given as

$$\Delta T = \frac{Q}{C_m \cdot m} \tag{2.19}$$

where C_m is the molar heat capacity and m the number of moles of the dielectric material receiving the energy Q. It is now apparent that higher heat capacity materials are needed. Higher thermal conductivity is necessary to allow larger dissipation of heat into the surroundings. ILD materials, with the exception of diamonds, invariably have very low thermal conductivities and high molar heat capacities. Polymers have thermal conductivities that are much lower, about a factor of 100 or more lower compared to inorganic dielectrics (e.g. thermal conductivity of Teflon, PVC and Parylene-N are, respectively, in the range of 0.002–0.003, 0.0012–0.0017, and 0.0012 W/cm/°C [57]). Molar heat capacities of polymers are, in general, larger and depend on the molecular weight.

The role of the CTE in determining the stress in the ILD films and thus on their mechanical stability has been discussed earlier. Here it is pointed out that the magnitude and the sign

(tensile positive, or compressive negative) of the stress depends on the sign of $(\alpha_F - \alpha_S)$ and of $(T_2 - T_1)$, see Eq. (2.15). T_1 is the stress measurement or the use temperature and when $T_1 > T_2$, the stress changes sign for a given $(\alpha_F - \alpha_S)$. If the circuit temperatures are high, the stress is expectedly lower in magnitude since $(T_2 - T_1)$ decreases (until $T_2 - T_1$ is zero). One can envisage tailoring of the new dielectrics such that α_F's temperature dependency either compensates for the effect of $(T_2 - T_1)$ or controls the sign of the stress. Such tailoring is morely likely with a polymer or porous materials than with a theoretically dense inorganic dielectrics.

Almost all ILD materials (inorganic oxides and glasses and polymers), when cooled from a molten state, transform into a undercooled liquid and then to a glass or into an amorphous state prior to changing to a glass. The temperature, below which a rigid glassy structure results, is referred to as the glass transition temperature, T_g. On heating an ILD material, the reverse happens. At and above T_g, the material transforms from the rigid solid form to a semi-viscous state. One can determine T_g by measuring density or CTE of these materials as a function of the increasing temperature. Above T_g, the density decreases and CTE increases more rapidly with temperature than the rate of change in these quantities at temperatures below T_g. For ILD applications such transformations must be avoided, leading to a required high T_g value.

It is noted that the glass transition temperature is a function of the impurity content of the ILD material, as is reflected much more significantly in inorganic glasses. IC industry has used P, B, As, and Ge additions, individually or in combinations, to lower the T_g of the deposited SiO_2 films, thus allowing a viscous flow to flatten the top surface topography. For polymers, the molecular weight, chemical structure, diluents and copolymerization, and cross-linking – all influence the T_g [58]. Dependence of the T_g on the molecular weight $\overline{M_n}$ (generally a number average of the degrees of polymerization is used, as indicated by the bar over M_n) is given as [59, 60]:

$$T_g = T_g^{\infty} - \frac{K}{\overline{M_n}} \tag{2.20}$$

where T_g^{∞} is the glass transition temperature for an infinite molecular weight polymer, and K is a constant specific to a polymer. Thus, higher molecular weights will lead to higher T_g. Similarly, polymers with stiffer chains, stronger inter-molecular interactions, increased cross-linking, and increased crystallinity are expected to have higher T_g. Note that as far as cross-linking is concerned, the increase in T_g due to increase in cross-linking depends not only the increase in the extent of cross-linking but also on their distribution in the polymer. For a copolymer, one can approximate the T_g by [58].

$$\frac{1}{T_g} = \frac{W_1}{T_g(1)} + \frac{W_2}{T_g(2)} \tag{2.21}$$

where W_1 and W_2 are the weight fractions of polymer (1) and (2) in the copolymer and $T_g(1)$ and $T_g(2)$ are their respective glass transition temperatures in pure form. Some of the known T_g values of polymers are listed in Table 2.6.

As the temperature rises in the dielectric during the operation of the circuit or during processing, the dielectric may interact with the surroundings. Such interactions are determined by thermodynamic and kinetic properties, for example, the free energies of the formation of reaction products formed as a result of the interactions at the ILD-surroundings interfaces and the inter-diffusion coefficients. Adhesion of the ILD to the surrounding materials is also affected by these thermodynamic and kinetic behaviors and the stress is related to the difference in the CTEs of the film and the substrate (and the materials in contact with the ILD) and the temperature excursions the ILD is subjected to. ILD materials are in contact with: (a) the contact metal (e.g. W, $CoSi_2$, or any other silicide); (b) the diffusion barrier and adhesion promoter (e.g. Ti/TiN or TaN_x); and (c) the interconnection metal (e.g. Al or Cu or their alloys). Thus, we are concerned with the thermodynamic properties and interdiffusion parameters of the ILD materials (e.g. SiO_2, low-κ materials), W, Ti, TiN, Al or Al alloys, TaN_x and Cu or Cu-alloys.

The known thermal and thermodynamic properties of metals and related compounds have been tabulated in Chapter 2 of Ref. [34]. Only the properties of ILD materials are presented and discussed here. Table 2.8 lists known thermal and thermodynamic properties of

Table 2.8 Thermal and thermodynamic properties of inorganic dielectrics[a]

ILD material	ΔH_f (kJ/mol)	Melting point (°C)	Thermal Conductivities (W/cm/K)	Molar heat capacity (J/mol/K)
BN	252	2730	0.015	19.6
Diamond	–	> 3550	~20	6.1
MgO	602	2800	0.36 at 100°C	37.2
Al_2O_3	1676	2015	0.26 at 100°C	78.8
AlN	318	> 2200	0.67	30.1
SiO_2	911	~1725	0.014 at 0°C	44.6
Si_3N_4	745	~1900	0.023	99.1
TiO_2	944	1840	~0.065 at 100°C	55.1
V_2O_5	1550	690	0.044	127.3
Cr_2O_3	1135	2265	–	104.5
Y_2O_3	1905	2410	0.063	102.9
ZrO_2	1101	2677	~0.02 at 100°C	56.0
Nb_2O_5	1900	1485 ± 5	–	132.1
La_2O_3	1795	2307	–	108.8
CeO_2	1090	2600	–	61.52
HfO_2	1118	2777	0.046	60.2
Ta_2O_5	2046	1872 ± 10	–	134.8
Si	–	1412	1.39	4.8

[a]Best values selected from Ref. [18].

inorganic dielectrics. A similar table could not be produced for the organic or porous dielectrics due to both the lack of information and the uncertainties associated with the polymer molecular weight, polymerization by-product retention in the films, and accurate and reproducible generation of polymer materials. For polymer/metal interactions, one can compare the diatomic bond strengths (listed in Table 2.9) of bonds that form the polymer and the bonds that may result as a result of interaction with a deposited metallic film or the ambient. It is apparent that C–C, C–H, C–N, C–F, and C–O bonds are ones with strongest bond strengths and therefore, difficult to break by an interaction that will lead to the lowered system energy. However, polymers also exhibit a large member of less stable bonds; (a) double and triple bonds that are relatively easy to break; and (b) bonds with active group like –OH, $–NH_2$, C═O, etc. that may participate by losing part of their character (e.g. H, or C═O→C–O–).

Diffusion of metallic and/or ambient species (e.g. H_2O, O_2) into dielectrics is known to change the dielectric properties significantly. Some of these are described earlier. For polymers, specially, there are several preparations related factors that influence the diffusion of the above mentioned species into the polymer films [57]. For example, the entrapped solvents and plasticizers increase the water permeability. On the other hand, increased degree of cross-linking, crystallinity, and non-polarity decreases the water permeability. Hydrophobic polar groups enhance the tendency to absorb water. Porous materials provide significantly more challenge in

Table 2.9 A comparison of diatomic strengths of interest [18]

Bond	Strength (kJ/mol)	Bond	Strength (kJ/mol)	Bond	Strength (kJ/mol)
C–C	607 ± 21	O–Cu	269.0 ± 20	H–Ti	204.6 ± 8.8
C–Cl	397 ± 29	O–Al	571 ± 3	N–Ta	611 ± 84
C–F	552	F–Si	552.7 ± 2.1	N–Al	297 ± 96
C–H	338.32	C–Ce	444 ± 13	N–Ti	476.1 ± 33.1
C–N	754.3 ± 10	C–Hf	540 ± 25	N–V	477.4 ± 17.2
C–O	1076.5 ± 0.4	C–La	462 ± 20	N–Y	481 ± 63
C–P	513.4 ± 8	C–Mo	481 ± 15.9	N–Zr	564.8 ± 25.1
C–Si	451.5	C–Nb	569 ± 13.0	F–Al	663.6 ± 6.3
H–N	⩽ 339	C–Os	⩾ 594	F–Cu	413.4 ± 13
H–O	427.6	C–Pt	598 ± 5.9	F–Hf	650 ± 15
H–Si	⩽ 299.2	C–Rh	580.0 ± 3.8	F–Mg	461.9 ± 5.0
H–Cu	277.8	C–Ru	616.2 ± 10.5	F–Mo	464.8
N–F	343	C–Ti	423 ± 29	F–Ta	573 ± 13
N–O	630.57 ± 0.13	C–V	427 ± 23.8	F–Ti	569 ± 33
N–P	617.1 ± 20.9	C–Y	418 ± 14	F–V	590 ± 63
N–Si	470 ± 15	C–Zr	561 ± 25	F–Y	605.0 ± 20.9
O–F	222 ± 17				

understanding the penetration of metallic or ambient species because of the variabilities introduced by pore density, pore-size, and pore distribution in the bulk and near the surface of films.

It is also noted that crystalline materials may not necessarily provide all the good properties unless they cover the underlying substate as one crystal with no grain boundaries and crystalline defects, for example, dislocations. Polycrystalline films provide fast diffusion paths and are thus avoided. Free volume in the ILD, such as those in amorphous SiO_2, polymers, or porous dielectrics, also leads to significant impurity in-diffusion. For example, amorphous SiO_2 films are known to readily allow sodium migration. By adding phosphorus, which apparently goes to the free volume sites, a barrier to the fast diffusion of Na (thermally or bias-temperature induced diffusion) is created. However such additions affect other properties.

2.6 Summary

This chapter has reviewed, listed, and discussed the required properties of dielectric material for possible applications as an interlayer dielectric in the integrated circuits. It is apparent that at present we have a very limited understanding of the most of these materials because of the lack of atomic/molecular order in these solids. Thus, considerable effort needs to be expended to engineer the dielectric for ILD application. At the same time more effort is needed to generate fundamental understanding of such materials especially the low-κ polymer/porous dielectrics.

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Interlayer Dielectrics for Semiconductor Technologies
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Chapter 3
Characterization of low dielectric constant materials

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Abstract

As integrated circuit dimensions continue to decrease, RC delay, crosstalk noise and power dissipation of the interconnect structure become limiting factors for ultra-large-scale integration of integrated circuits. Materials with low dielectric constant (κ) are being developed to replace silicon dioxide as interlevel dielectrics. In this review, the general approach to reduce the dielectric constant is first discussed, emphasizing the correlation of dielectric polarizability with bonding characteristics and the tradeoff of dielectric constant and mechanical properties. Then the material characterization techniques are described, including several recently developed for porous low-κ materials. These techniques have been applied extensively to evaluate the properties of low-κ dielectrics. Characteristics of three classes of materials are summarized: polymers, silsesquioxianes and porous dielectrics, focusing on the correlation of molecular structure and material properties. Results from porous organosilicate films revealed that while dielectric constant and thermal conductivity scale with the average density of the material, the thermomechanical properties degrade significantly beyond the percolation point when pores become interconnected. This points out the challenge for development of porous low-κ dielectrics.

3.1 Introduction

Continuing improvement in device density and performance has significantly impacted the feature size and complexity of the wiring structure for on-chip interconnects. As the minimum

device dimensions reduce beyond 250 nm, the increase in propagation delay, crosstalk noise and power dissipation of the interconnect structure become limiting factors for ultra-large-scale integration (ULSI) of integrated circuits. To sustain chip improvements by device scaling, new materials with lower resistivity and dielectric constant have to be developed for use as metal lines and interlevel dielectrics (ILDs) to replace the conventional Al(Cu)/SiO_2 metallization. This has prompted the development of Cu/oxide interconnect announced in 1997 [1, 2]. The Cu interconnect structure is fabricated using the damascene process where Cu is deposited into wiring channels patterned into the ILD layer and then planarized using chemical–mechanical polishing (CMP). The damascene structure introduces a new set of structural elements and processes that are distinctly different from the standard AlCu interconnect. The subsequent development of Cu interconnects with low-κ ILD was highlighted in the 1997 National Technology Roadmap for Semiconductors [3]. It was not fulfilled, however, until 2000 when IBM announced the development of Cu interconnects with SiLK [4], a low-κ dielectric developed by the Dow Chemical Company with κ about 2.7 [5]. Subsequently, several companies have announced the development of Cu interconnnects incorporating various low-κ dielectrics with κ in the range of 2.7–3.0. At this time, there is intensive effort in the industry to develop Cu/low-κ interconnects with porous dielectrics with κ of about 2.3.

The delay in the implementation of low-κ ILD can be largely attributed to the many challenges associated with the successful integration of these materials into the dual damascene interconnect structures. In addition to low dielectric constant, candidate materials must satisfy a large number of diverse requirements in order to be successfully integrated. The requirements include high thermal and mechanical stability, good adhesion to the other interconnect materials, resistance to processing chemicals, low moisture absorption, and low cost [6]. A particularly difficult challenge for material development has been to obtain the combination of low dielectric constant and good thermal and mechanical stability. Generally, the types of chemical structures that impart structural stability are those having strong individual bonds and a high density of such bonds. However, the strongest bonds often are the most polarizable, and increasing the bond density gives a corresponding increase in polarization. For example, the rigidity and thermal stability of SiO_2 is in part due to the dense (2.2–2.4 g cm^{-3}) chemical network. Unfortunately, the high bond and material density in SiO_2 leads to a large atomic polarizability, and therefore a high dielectric constant.

The mechanical properties of the organic polymers are likewise inferior to those of oxide for similar reasons. Organic materials most resistant to thermal decomposition and mechanical deformation are those incorporating double and triple bonds, which tend to increase the dielectric constant of these materials. Since it is difficult to reduce the dielectric constant below 2.5 with fully dense materials, it may be necessary to introduce micro or mesoporosity to achieve low-κ values below 2.0. The pores are incorporated into a network material that can be organic, inorganic, or a hybrid material. Because introduction of voids will compromise other material properties, such as mechanical strength, the chemical structure of the porous network must be

carefully designed to achieve sufficient thermomechanical stability. The material properties of porous low-κ dielectrics will be examined in this review as a function of porosity.

The fabrication of multi-level structures requires as many as 10–15 temperature excursions, which may reach 400–425°C. Therefore, thermal cycling during processing requires future ILD materials to have high thermal stability and properties, which are relatively insensitive to thermal history. Outgassing of volatiles due to decomposition or to trapped solvent or reaction products can cause via poisoning and delamination and blistering in the ILD. Thermal cycling also causes stresses in the interconnect structure due to the coefficient of thermal expansion (CTE) mismatch between the ILD material and the metal or substrate. Such stresses may cause delamination if adhesion is poor. Adhesion strength is determined by chemical bonding at the metal/ILD interface and the energy dissipation originated from the mechanical interaction between the metal and ILD. Thus, future ILDs should ideally have good mechanical properties such as a large Young's modulus (E), tensile strength, and elongation-at-break, although it is not yet clear what constitutes sufficient mechanical strength for successful integration into a manufacturable process. A high modulus retention at elevated temperatures, $E(T)$, is required for the ILD to maintain its structural integrity and dimensional stability during subsequent processing steps. Related to $E(T)$ is the glass transition temperature, T_g. Exceeding the T_g causes a large decrease in the modulus and yield stress in amorphous, non-crosslinked polymers, so a T_g greater or equal to the highest processing temperature is desired. The thermal conductivity of most low-κ materials is typically about four to five times smaller than that of PE-TEOS ($K_{th} = 1.1\,W\,m^{-1}K^{-1}$) [7–11] making Joule heating effects in a low-κ ILD a major reliability concern.

Recent X-ray measurements on thermal stresses in Cu/low-κ line structures revealed that the barrier and cap layers in the damascene structure are important in reinforcing the low-κ ILD to confine the thermal deformation of the Cu lines [12]. This leads to a stress state in the Cu lines distinctly different from that in the AlCu/low-κ lines not integrated with the damascene structure. This will affect the long-term reliability of chips fabricated using low-κ materials, which must also be evaluated. Electromigration and stress voiding are primary failure mechanisms in integrated circuits [13–15], where damages are caused by local divergence of mass transport driven by electrical current and thermal stress. The damage mechanism has been investigated for electromigration in Cu/oxide and Cu/low-κ interconnects and found to be associated with the damascene structure and distinctly different from AlCu interconnects [16, 17]. Statistical studies of Cu interconnects have revealed multi-mode failures with the early failures dominated by void formation at the via bottom interfaces [16]. In Cu/low-κ structures, the weak mechanical strength of low-κ ILD is less effective in confining mass transport induced by electromigration and failures were observed due to Cu extrusion at the dielectric/cap layer interface [18]. These results indicate that material properties and structural integrity are important in sustaining the Cu interconnect reliability. While a review of the reliability studies is beyond the scope of this article, more work is clearly required to fully understand the impact of low-κ material integration on interconnect reliability.

In this review, the general approach to reduce the dielectric constant is first discussed, emphasizing the correlation of dielectric polarizability with bonding characteristics and the trade-off of dielectric constant and mechanical properties. Then the material characterization techniques will be described, including several recently developed for porous materials. These techniques have been applied extensively to evaluate the properties of low-κ dielectrics. Finally, results for three types of materials: polymers, silsesquioxianes and porous dielectrics will be discussed, focusing on the correlation of molecular structure and material properties. Material properties of porous organosilicate films are of particular interest, revealing the degradation of thermomechanical properties with increasing porosity beyond the percolation point where the pores become interconnected. In discussing the properties of low-κ dielectrics, some of the challenges in the integration of low-κ dielectrics will be highlighted, particularly for further scaling of interconnect dimensions.

3.2 Dielectric constant and bonding characteristics

In order to reduce the κ value relative to that of SiO_2, it is necessary to either incorporate atoms and bonds that have a lower polarizability, or else to lower the density of atoms and bonds in the material, or both. With regard to the first effect, there are several components contributing to the polarizability that must be minimized in reducing the dielectric constant. The polarization components usually considered are the electronic, atomic, and orientational responses of the material. The latter two components constitute the nuclear response and are important at lower frequencies ($< 10^{13}\,s^{-1}$), while the electronic response dominates at higher frequencies. At typical device operating frequencies, currently $< 10^{9}\,s^{-1}$, all three components contribute to the dielectric constant, and should be minimized for optimum performance.

Some typical electronic polarizability and the associated bond enthalpy data are shown in Table 3.1. The data indicates that single C–C and C–F bonds are among those having the lowest

Table 3.1 Electronic polarizability and bond enthalpies

Bond	Polarizability (Å^3)[a]	Average bond energy (kcal mol^{-1})[b]
C–C	0.531	83
C–F	0.555	116
C–O	0.584	84
C–H	0.652	99
O–H	0.706	102
C═O	1.020	176
C═C	1.643	146
C≡C	2.036	200
C≡N	2.239	213

[a]Ref. [19].
[b]Ref. [20].

electronic polarizability, making fluorinated and nonfluorinated aliphatic hydrocarbons potential candidates for low-κ applications. Incorporation of fluorine atoms is particularly effective in lowering the polarizability [21] due to their high electronegativity, which leads to tight binding of electrons. Conversely, the electronic polarizability is high for materials having less tightly bound electrons. For example, materials containing a large number of carbon double and triple bonds can be expected to have a large polarization due to the increased mobility of the π electrons. Conjugated carbon double bonds in aromatic structures are a common source of extensive electron delocalization leading to high electronic polarizability. Note, however, that there is a trade-off in achieving low dielectric constant and high bond strength, as the low-polarizability single bonds are among the weakest, while the double and triple bonding configurations have much higher bond enthalpies. Here lies one of the fundamental difficulties for development of low-κ dielectrics, particularly for porous materials where the thermomechanical properties generally degrade further with incorporation of pores. This problem will be examined in a later section in connection with the discussion of development of porous organosilicate materials and results from a recent study of the porosity effect on the material properties will be reviewed.

The nuclear dielectric response results from the polarization due to both permanent and transition dipoles in the material. The response is often dominated by polar substituents, such as hydroxyl and carbonyl groups, which can increase the orientational component of the polarizability. The relative importance of the electronic, compared with the nuclear, response for a material can be shown by examining the differences between the κ values measured at high and low frequencies. The high frequency value (633 nm or 4.74×10^{14} Hz), reflecting the electronic component, can be obtained through the optical refractive index according to $\kappa = n^2$ [22]. This relationship assumes no absorption at the optical frequency used in the measurement. The low frequency κ value, representing both the electronic and nuclear components, can be determined from capacitance measurements of metal–insulator–semiconductor (MIS) or metal–insulator–metal (MIM) structures at 1 MHz.

Table 3.2 shows the high frequency electronic response, obtained from the optical index at 633 nm, and the total low-frequency κ value at 1 MHz for a number of low-κ dielectrics. The difference in the two measurements represents the nuclear components in the dielectric constant. The data indicates that for many low-κ materials under consideration, the nuclear components are small relative to the electronic part of the response. In contrast, SiO_2 has a large nuclear component, largely due to the strong atomic polarization. The κ value of SiO_2 can be reduced to 3.3–3.7 by incorporating fluorine into the material. Yang and Lucovsky have shown that the decrease is largely due to weaker atomic (infrared) activity [23].

Adsorbed moisture is particularly troublesome in raising the orientational component of the dielectric constant in thin films. Since water has a large permanent dipole moment, a small amount of moisture can substantially impact the dielectric constant. Therefore, when designing low-κ materials it is desirable to avoid the use of highly polar substituents that attract and bind water. Nevertheless, many dielectric films absorb water to some extent, so the dielectric constant and the loss factor depend strongly on the history of moisture exposure. When comparing

Table 3.2 Dielectric properties of low-κ materials

Material	n_{in}	n_{out}	κ_{out}	${n_{out}}^2$	$\Delta = \kappa - {n_{out}}^2$
PTFE	1.350	1.340	1.92	1.796	0.12
BPDA-PDA	1.839	1.617	3.12	2.615	0.50
PMDA-TFMOB-6FDA-PDA	1.670	1.518	2.65	2.304	0.35
PAE #1	1.676	1.669	3.00	2.787	0.11
FLARE #2	1.671	1.672	2.80	2.796	0.00
BCB™	1.554	1.554	2.65	2.415	0.24
SiLK™	1.630	1.624	2.65	2.637	0.01
OXZ (fluor.Poly.)	1.566	1.551	2.406	2.493	0.08
MSQ/HSQ hybrid	1.374	1.373	2.52	1.886	0.63
OSG (13% C)	1.433	1.435	2.059	2.69	0.63
OSG (30% C)	1.438	1.482	2.195	2.60	0.40
SiO_2	1.47	1.47	4.0	2.16	1.8

dielectric constants, measured in the megahertz range, it is important to specify sample treatment and humidity to account for the moisture uptake. Especially oxide-based materials like organosilicate glasses (OSGs), tend to absorb moisture. This can be observed in the form of a weak silanol absorption band around 3200–3700 cm^{-1} by FTIR, although FTIR usually lacks the sensitivity for a trace amount of water which also has strong effects on the dielectric constant. Porous, oxide-based materials are usually surface treated to obtain hydrophobic surfaces. Silylation has been shown to provide hydrophobic surfaces by replacing terminating OH groups with non-polar groups such as $Si(CH_3)_3$ [24, 25]. However, many of the materials tested so far still showed increasing dielectric constants when exposed to the lab ambient.

Dielectric constant is determined not only by the type of atoms and bonds, but also by the atom and bond densities, so its value for any material can be reduced by decreasing the density. The density can be lowered by using lighter atoms and/or by incorporating more free space around the atoms. For example, the lower dielectric constant of organic polymers relative to SiO_2 is partly due to the lighter C and H atoms vs. Si and O, and to the low packing density of most polymer chains relative to the crosslinked silica network. Likewise, the incorporation of light, space-occupying groups such as H or CH_3 into the silica network can significantly lower the material density, and therefore the dielectric constant, of materials such as spin-on glasses (SOG) relative to dense oxide.

Introduction of nanometer-sized pores into the material is a natural extension of this strategy to increase the free space and decrease the material density. The effect of porosity on the dielectric constant can be predicted using a simple model, such as the Bruggeman effective medium approximation [37]

$$f_1 \frac{\kappa_1 + \kappa_e}{\kappa_1 + 2\kappa_e} + f_2 \frac{\kappa_2 - \kappa_e}{\kappa_2 + 2\kappa_e} = 0 \tag{3.1}$$

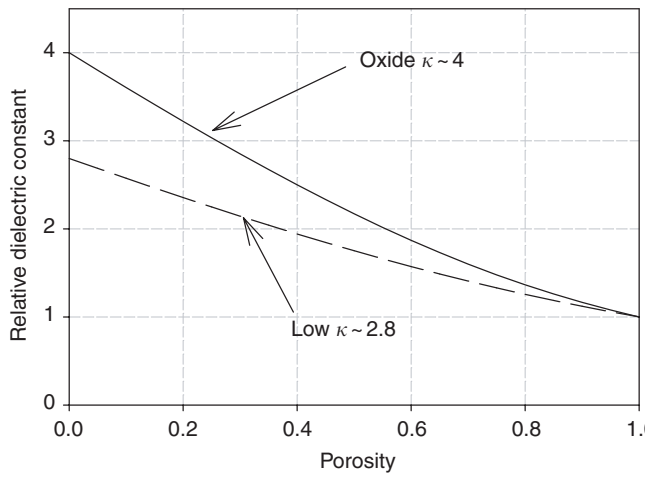

Fig. 3.1 Bruggeman's EMA showing dielectric constant vs. porosity for oxide and a low-κ material.

where $f_{1,2}$ represents the fraction of the two components, $\kappa_{1,2}$ the dielectric constant of the components, and κ_e is the effective dielectric constant of the material. The model assumes two components to the film, the solid wall material and voids. Figure 3.1 shows the dielectric constant as a function of porosity predicted by the model for SiO_2 ($\kappa = 4.0$) and for a lower $\kappa = 2.8$ wall material. The plots show that the κ value decreases slightly faster than linearly. Although the model is simple, the predicted results appear to be in reasonable agreement with recent experimental measurements on methyl-silsesquioxane [27] and oxide porous films. Difference between the theoretical prediction and experimental results is likely related to surface chemistry, such as the presence of terminating OH groups and adsorbed water, and to the pore geometry.

One point demonstrated in Fig. 3.1 is that significantly lower porosity would have to be incorporated into the lower κ material than into the SiO_2 in order to obtain a given κ value. For example, to get to $\kappa = 2.0$ about 55% porosity would be needed in an oxide material, whereas only ~35% would be needed in the lower κ material with κ of 2.8. Since percolation of pores can occur in a high-porosity film causing a number of yield and reliability concerns, there is a definite advantage using a lower κ starting material to minimize the amount of porosity needed.

3.3 Characterization techniques

Since ILD materials will be used as thin films ($\leqslant 1\,\mu m$ thick), and since thin film properties can differ appreciably from bulk properties or even from thick film properties for a given material, it is important to have characterization techniques applicable to thin films. In fact, many materials such as OSGs and porous silica cannot even be prepared in thickness much greater than about $1\,\mu m$ without cracking. Because it is difficult to remove such thin films from a substrate

for free standing-film measurements, it is usually necessary to perform thin film characterization using on-wafer techniques. As a result, there has been a great deal of work done to develop material testing methods capable of measuring the properties of very thin film on-wafer. Some of those will be described in this section. Table 3.3 lists a number of methods used for characterization of thin dielectric films that will not be discussed in further detail. The reader is referred to textbooks or review articles cited in the table.

Table 3.3 Characterization methods for thin film dielectrics

Property	Methodology
Refractive indices (in-plane and out-of-plane)	Prism coupling; optical measurement $\lambda = 632.8$ nm [28]; Ellipsometry [25, 29]
Dielectric constant (out-of-plane)	Metal–insulator–semiconductor (MIS) or metal–insulator–metal (MIM) parallel plate capacitance measurement; typically 1 MHz
Dielectric constant (in-plane)	Calculated based on the measured in-plane refractive index; Measured using line structures and capacitance simulation
Dielectric breakdown voltage	MIS or MIM capacitors
Leakage current	MIS or MIM capacitors, or serpentine line structure
Thermal stability	Isothermal thermogravimetric analysis (TGA) at 350 and 425°C for 8 h [30, 31]
	Change in thickness after 8 h anneal at 350 and 425°C
Chemical resistance	Treatment with chemicals including: boiling water, NMP, BOE, 2% NaOH, and photoresist stripper. Measured are chemical signature (FTIR), changes in thickness and adhesion to the Si wafer
Adhesion tests	Scotch tape pull, ASTM standard testing protocol.
Lateral thermal expansion coefficient	Thermal mechanical analysis (TMA). Free-standing films with a thickness of 5–10 μm [30, 31]
Vertical thermal expansion coefficient	Home-built differential capacitance system; measurements made on a Cu/dielectric/Si structure with a 0.2°C min^{-1}. heating rate; film thickness: 5–20 μm
Glass transition temperature	TMA and/or thermal stress measurement [30, 31]
Thermal stress	Wafer curvature or bending beam measurement [32, 33]
Tensile strength (MPa)	Stress–strain characterization performed using a custom-built micro-tensile tester. Five micrometers thick free-standing films [34]
Young's modulus (GPa)	Stress–strain measurement using micro-tensile tester; 5 μm thick freestanding films [34]. Nanoindentation, on wafer [19]
Young's modulus as a function of temperature	Dynamic mechanical analysis (DMTA) >5 μm thick, free-standing films [30, 31]
Chemical signature	FTIR [20, 35], XPS [36]
Phase transformations	Differential scanning calorimetry (DSC) [30, 31]
Wide angle X-ray diffraction	Crystallinity as a function of temperature

As a full evaluation of a low dielectric constant material for process integration requires time and cost intensive fabrication of single or multilevel Cu damascene test structures, an effective screening of materials properties is useful for selecting materials for further evaluation. The following is a list of properties and techniques for materials screening to identify promising materials. All measurements can be performed for 1 μm thick blanket films, requiring a minimum of sample processing. Although some of the techniques employ relatively advanced equipment, they allow evaluation of a large number of new materials in a relatively short period. To simplify the screening test, the dielectric constant is measured at 1 MHz, which is considerably below the device operating frequency. The dielectric constant, particularly the loss factor, of low-κ material at device operating frequencies may vary from its value determined at 1 MHz. Specialized techniques have been developed for such measurements and are described elsewhere [37].

- Dielectric constant (1 MHz): MIS capacitance,
- Thickness uniformity and anisotropy: optical prism coupling,
- Thermal stability: TGA,
- Moisture uptake: quartz crystal microbalance (QCM) or SANS,
- Adhesion to SiO_2, Si_3N_4, Ta, TaN: m-ELT and four-point bend,
- Young's modulus: dual substrate bending beam,
- CTE: dual substrate bending beam,
- Chemical signature and chemical resistance: FTIR,
- Density, porosity, and pore structure: SXR, SANS, PALS.

3.3.1 Adhesion

Adhesion of ILDs to the surrounding materials is one of the most critical issues for process integration. Although a wide variety of adhesion tests exist, yet the correlation of test data to the actual integration requirements remains difficult. The measured adhesion strength consists of contributions from several mechanisms such as intrinsic adhesion, plastic deformation or interface roughness and depends strongly on sample and load geometry as well as the test environment [38–41]. In general, it is difficult to compare adhesion energies determined from different methods or between materials with different plasticity, for example, polymers and OSGs are difficult. Among the commonly used methods, the m-ELT (modified edge delamination test) technique [42, 43] and the four point bend technique [44] were adopted by our laboratory to quantify the adhesion strength of dielectric films to various substrates.

The m-ELT method was developed by Ed Shaffer [42, 43] at Dow Chemical. In this test, a thick (50–200 μm) layer of epoxy is applied to the top of the film, and delamination is induced by lowering the temperature of the sample until the stored strain energy in the epoxy layer exceeds the adhesion energy of one of the interfaces. From the temperature at which debonding

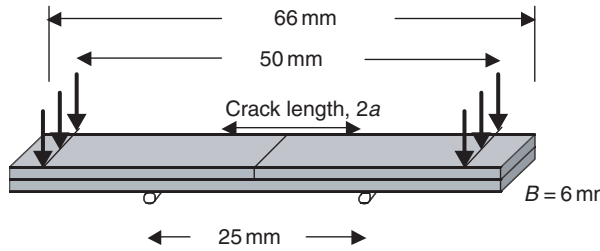

Fig. 3.2 Typical sample configuration for four-point bend test.

is observed by optical inspection, the fracture toughness can be calculated, if the stress temperature profile of the epoxy layer is known. After delamination the sample is examined to determine the interface at which debonding occurred. This method allows us to measure the adhesion energy of a material to various substrates or capping layers using blanket films with a minimum of sample preparation.

In the four-point bend test, the test structure is formed by bonding a silicon wafer with thin film layers of interest to another silicon wafer face to face, placing the film stack at the center of the sandwich structure [45]. A typical sample configuration with dimensions is shown in Fig. 3.2. As the bending moment increases, a precrack initiates from the top surface and propagates vertically to the interface. If the interface is sufficiently weak, the crack deflects into the interface and propagates along it. When the crack tip is far enough away from the vertical precrack, the strain energy release rate becomes independent of the crack length. This is a characteristic of steady-state crack growth that simplifies the measurement of the fracture energy without an accurate determination of the crack size. Applying the beam theory, the strain energy release rate, or the fracture energy can be determined as [44]:

$$G_c = \frac{21(1-\nu^2)P_c^2 l^2}{16EB^2h^3} \tag{3.2}$$

In this expression, E is Youngs modulus, ν the Poisson ratio, B the sample width, h the sample half-thickness, P the load, and l the distance between inner and outer loading points. Due to the different mode of the load driving crack formation, or 'mode mixity', it is not straightforward to compare the adhesion energies obtained by m-ELT and the four-point bend techniques although the trends observed by these techniques for specific materials are usually consistent.

3.3.2 Moisture uptake

On-substrate moisture absorption measurements for thin film ILD materials are difficult, because direct gravimetric methods can not be applied due to the extremely small mass of the

dielectric films as compared with the substrate mass. One method for measuring moisture uptake is to perform a SANS analysis as described in the next section on a sample immersed in deuterated water. The difference in SANS intensity as compared with a dry sample can be converted to a volume fraction of the absorbed water [46].

In our laboratory the amount of moisture absorbed by low-κ dielectric candidate materials is measured using a QCM. In the QCM experiment, a quartz crystal is coated with a thin film of the ILD material and the resonance frequency of the crystal is measured while exposing the specimen to water vapor. Changes in resonance frequency can be correlated with the mass of the absorbed moisture using the Sauerbrey equation [47]:

$$\Delta m = \frac{\sqrt{\rho_Q \mu_Q}}{2}\left(\frac{\Delta f}{f_0^2}\right) \tag{3.3}$$

where ρ_Q is the density of quartz and μ_Q the shear modulus of quartz.

As this technique relies on the measurement of the resonance frequency (≈ 6 MHz) of a quartz oscillator the required resolution of < 0.1wt% is easily achieved. However, one of the main disadvantages of this technique is that the material has to be coated onto quartz oscillators, which are typical 0.5 in. quartz disks with gold electrodes.

To obtain the moisture uptake relative to the mass of the dielectric film, the resonance frequency of a blank quartz crystal, f_0, is measured, then the crystal is coated with an ILD film. By measuring the resonance frequency for the dry film, the mass of the coating is determined. Then the chamber is back-filled with water vapor from a constant-temperature vapor source and the frequency of the crystal with the ILD material is monitored as a function of time until saturation is observed. By subsequent evacuation of the chamber and back filling with water vapor the total moisture uptake and its time dependency can be measured. Assuming a Fickian diffusion mechanism the initial moisture uptake can be quantified as:

$$\frac{M_t}{M_\infty} = 2\left(\frac{D}{\pi}\right)^{1/2}\left(\frac{t^{1/2}}{l}\right) \tag{3.4}$$

where M_t and M_∞ indicate the mass changes at time t and at saturation, respectively, l the film thickness and D the diffusion coefficient ($cm^2\,s^{-1}$). Linear regression of the initial moisture uptake data yields a line with a slope $2(D/\pi)^{1/2}$ from which the diffusion coefficient can be calculated.

3.3.3 Dual-substrate bending beam

Traditionally, the modulus of polymer thin films is determined by stress–strain curves obtained from microtensile testing of free-standing films. This type of experiment normally requires films of at least 3–5 μm thick. In order to make measurements on materials that cannot be prepared in free-standing form, either because they are too thin or too brittle, wafer curvature methods

have been developed to obtain the modulus from thermal stress measurements. The substrate curvature as a function of temperature is normally measured optically by monitoring the reflection of a laser off the wafer. The stress is calculated from the curvature using Stoney's equation [48]:

$$\sigma = \frac{M_s t_s^2}{6Rt_f} \tag{3.5}$$

where M_s is the biaxial modulus of the substrate ($M = E/(1-\nu)$, where ν is the Poisson ratio), t_s the substrate thickness, t_f is the film thickness, and R the radius of curvature. The application limit of the Stoney's equation has been discussed in the literature [49, 40]. Generally, the relationship of Eq. 5 is applicable to thin films on thicker, rigid substrates.

In our laboratory, we use a bending beam variation of the curvature method [32, 33], as shown in Fig. 3.3. The curvature of a narrow beam of a rigid substrate (3 mm × 48 mm) due to the thermal stress of a thin (~1 μm) film coated on top is optically measured. We use thin Si substrates (125–250 μm) to amplify the curvature change that occurs with thermal cycling, and monitor changes in curvature using position-sensitive detectors. Recently the sensitivity of the system has been improved, making it possible to perform the measurement on 600–650 μm thick Si substrate. A long light path (1–4 m) offers improved sensitivity compared with commercial instruments, and allows measurement of the relatively small stresses (5–50 MPa) present in low-κ films.

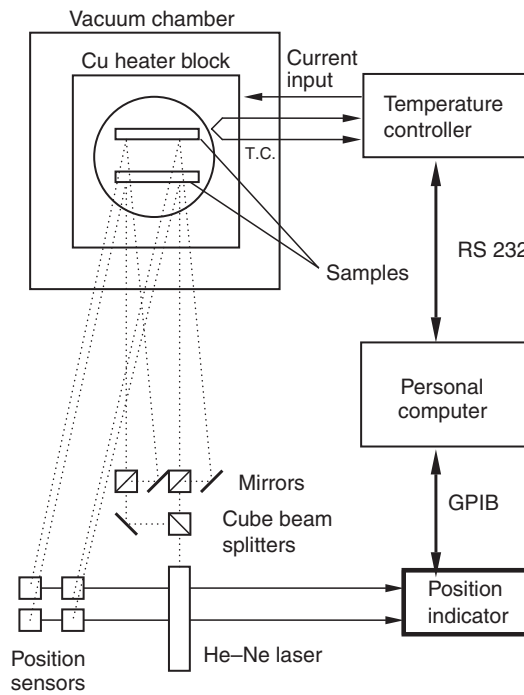

Fig. 3.3 Bending beam system for measuring thermal stress of thin films. Two beams can be measured simultaneously.

The slope of the stress vs. temperature curve due to the CTE mismatch between a film and a rigid underlying substrate, such as Si, is

$$\kappa = \frac{\mathrm{d}\sigma}{\mathrm{d}T} = M_\mathrm{f}(\alpha_\mathrm{s} - \alpha_\mathrm{f}) \tag{3.6}$$

where α_s and α_f denote the substrate and film CTE, respectively, and M_f is the film's biaxial modulus. By measuring the slope of the stress curve for film samples deposited on two substrates having different CTEs, one obtains two equations that can be simultaneously solved to determine both M_f and α_f [51].

$$\alpha_f = \frac{k_2\alpha_{\mathrm{s}1} - k_1\alpha_{\mathrm{s}2}}{k_2 - k_1} \tag{3.7}$$

$$M_\mathrm{f} = \frac{k_2 - k_1}{\alpha_{\mathrm{s}2} - \alpha_{\mathrm{s}1}} \tag{3.8}$$

where $k_{1,2}$ are the stress vs. temperature slopes on the two different substrates, and $\alpha_{1,2}$ are the associated substrate CTEs. In our lab Ge (CTE 5.8 ppm °C^{-1}) has been used as a substrate in conjunction with Si (CTE 2.6 ppm °C^{-1}) [52].

It should be noted that high precision and accuracy in the slope measurement is essential for a reliable measurement, particularly when the difference in slopes or in substrate CTE is small. Fig. 3.4 shows the intervals where the calculated CTE and biaxial modulus have errors of 10% or less based on the calibration of the setup currently used and data for different materials. Although the method is still applicable beyond the intervals shown, extra care has to be taken to improve the precision of the slope measurement. This can be achieved by taking data over an extended temperature range or by enhancing the sensitivity of the instrument with extended light path. However, the repeatability and precision of the slopes have to be checked carefully. In data analysis, the temperature dependence of the parameters in Eqs (3.7) and (3.8) should be taken into account, or if possible, the stress measurement should be performed over a limited temperature range to minimize the variation of these parameters. In any case the CTE and modulus determined are implicitly averaged values over certain temperature ranges. The technique has been used successfully to measure the properties of polymers, OSGs, and several porous silica-based films. Results for HSQ [33] are shown in Fig. 3.5.

3.3.4 3ω Method for thermal conductivity

The thermal conductivity (K_th) of the ILD is important, because if heat is not conducted away from interconnect fast enough, Joule heating can cause temperature-induced reliability problems. Because most low-κ materials are expected to have a significantly lower K_th than TEOS-oxide (K_th = 1.2–1.4 W m^{-1} °C^{-1}) [44, 45], measurement of K_th is useful for evaluating the severity of potential problems associated with heat dissipation.

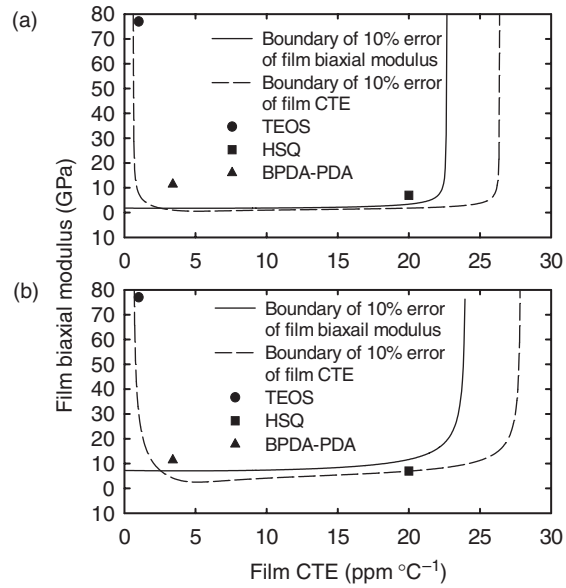

Fig. 3.4 Applicable regions of dual substrate bending beam method for 1 μm thick films: (a) 125 μm thick Si and Ge; (b) 250 μm thick Si and 300 μm thick GaAs. Plot assumes 0.5% error in film, substrate thickness and substrate modulus and a CTE, curvature error of 2.1×10^{-4} m^{-1}.

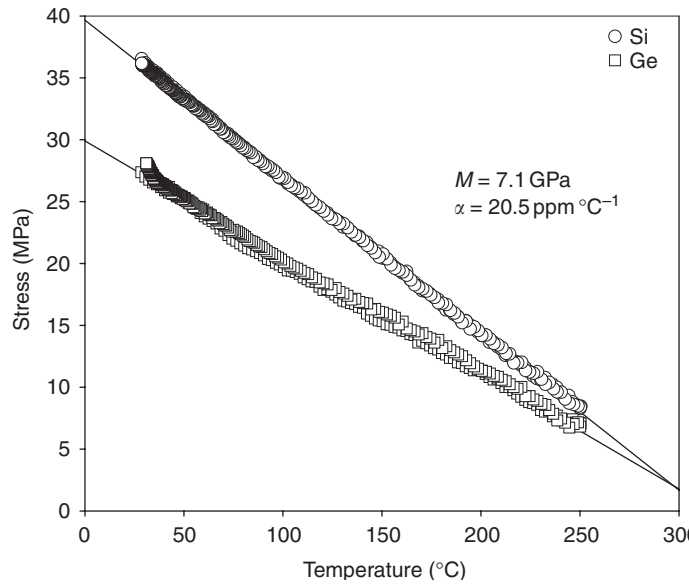

Fig. 3.5 Thermal stress data from dual-substrate bending beam measurement of 0.5 mm thick HSQ films on Ge and Si substrates. The biaxial modulus and CTE were determined to be 7.1 GPa and 20.5 ppm °C^{-1}, respectively.

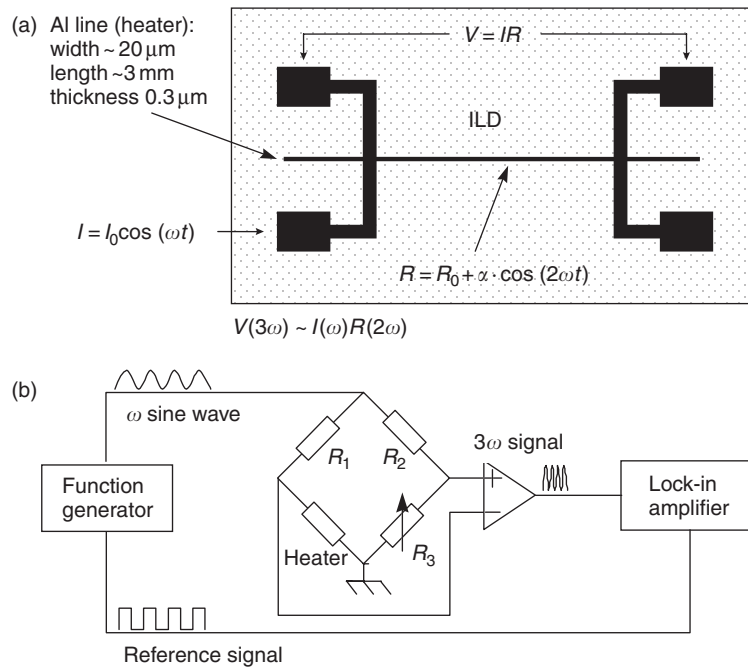

Fig. 3.6 (a) Top view of 3ω sample showing the metal line structure; (b) Experimental configuration for 3ω measurement. The sample (heater) is incorporated into a Wheatstone bridge to eliminate noise, while the signal is isolated using a lock-in amplifier.

In our laboratory a variation of the 3ω technique has been developed [53, 55–57], for measuring K_{th}. This technique determines the thermal conductivity by measuring the thermo-electrical response of a thin-film conductor patterned on the dielectric film. The experimental setup of the 3ω method used is schematically shown in Fig. 3.6. The test structure was made up of a dielectric film deposited on a Si substrate and a metallic heater element patterned on top of the dielectric film with a lithography tool. The heater element, which served also as a thermometer to sense the temperature increase, was processed as a 300 nm thick Al line structure with a 5 nm Cr adhesion promoter underneath. To minimize the edge effect at the contact pads, the length of the heater, typically 3 mm, was chosen to be about 100 times larger than its width (30 μm). The heater was then incorporated as one arm of a Wheatstone bridge circuit. Three other resistors completed the circuit, which were chosen to have a low temperature coefficient of resistivity in order to minimize their contributions to the 3ω signal. When a current at frequency ω is applied to the heater element, the Joule heating causes a small increase in resistance modulating at a frequency of 2ω:

$$R = R_0 + \alpha \Delta T \cos(2\omega t + \phi) \tag{3.9}$$

where α is the temperature coefficient of the electrical resistivity, ΔT the change in temperature and R_0 the resistance at a reference temperature. By measuring the voltage drop $I(\omega)R(2\omega)$ across the heater element, there is a small 3ω component directly corresponding to the temperature increase:

$$V = I \cdot R = I_0 R_0 \cos(\omega t) + \tfrac{1}{2} I_0 \alpha \Delta T \cos(\omega t + \phi) + \tfrac{1}{2} I_0 \alpha \Delta T \cos(3\omega t + \phi) \tag{3.10}$$

By measuring the amplitude $1/2\,\alpha \cdot \Delta T \cdot I_0$ of the 3ω component, we can determine the temperature change of the heater as a function of the frequency ω. The temperature coefficient of electrical resistivity is measured separately for each sample to calibrate the temperature measurement. To extract the 3ω component, an operational amplifier is coupled with lock-in amplification to achieve the precision required.

The experiment is performed as a function of modulation frequency. The sensitivity of the technique results from measuring only the incremental resistance rise, rather than the much larger total resistance of the line. The use of heaters with small surface area suppresses heat convection and radiation. Wheatstone bridge filters out the 3ω noise generated by the power supply. These designs enable the lock-in amplifier to pick up very small change in the 3ω component of the line resistance. So very small temperature changes (< 0.1°C) can be readily measured. As a result, the thermal conductivity of very thin films, possibly as thin as 50 nm, under only a small temperature gradient can be measured. The temperature change is related to thermal resistance R_{th} as

$$R_{\text{th}} = \Delta T / P \tag{3.11}$$

where P is the applied electrical power. R_{th} has two contributions: from the Si substrate, and the ILD film. The film contribution can be extracted by measuring R_{th} of a line deposited on bare Si (with its thin native oxide layer for insulation) and subtracting it from the measurement of the ILD on Si sample.

Normally, the film thickness and modulation frequency (ω) are chosen so that the thermal diffusion length inside the film (L_{th}),

$$L_{\text{th}} = \sqrt{\frac{\Lambda}{\omega}} \tag{3.12}$$

is much larger than the film thickness, where Λ is thermal diffusivity. For low-κ films of about 1 μm thickness this is usually satisfied if the frequency is chosen below 1 kHz. In this case the thermal conductivity of the film can be calculated from R_{th}^{f} the film contribution to thermal resistance:

$$K_{\text{th}} = \frac{t}{R_{\text{th}}^{\text{f}} l w} \tag{3.13}$$

where t is the thickness of the film and w the width of the heater. Under these conditions R_{th}^{f} is frequency independent. The calculation leading to Eq. (3.13) assumes a one-dimensional (1-D) vertical thermal flow, which should be a good approximation when the film thickness is small

compared to both the line width and the thermal diffusion length in the film, L_{th}, $w \gg t$. Also, the line end effects are ignored, which is reasonable when $l \gg w$. These assumptions have been verified by finite element analysis, showing that for our geometry the corrections for 2-D heat flow are negligible when the thermal conductivity exceeds $0.06\,W\,m^{-1}\,K^{-1}$ [53].

We have recently performed K_{th} measurements for a number of ILD films (Table 3.4). The result for TEOS is in good agreement with measurements of SiO_2 reported in Refs. [54] and [58] and the BPDA-PDA value agrees well with that obtained by photothermal measurement [59]. The K_{th} values for xerogel samples suggest that thermal conductivity decreases significantly with increasing porosity. The thermal resistance data for 48% porous xerogel are plotted in Fig. 3.7, where both the in-phase and out-of-phase component are shown. The in-phase component measures thermal conductivity while the out-of-phase component is due to heat dissipation.

Table 3.4 Thermal conductivities of low-κ thin films (~1 μm)

Material	K_{th} ($W\,m^{-1}\,°C^{-1}$)
XEROGEL[a]	
48% porous	0.250
63%	0.157
70%	0.108
77%	0.065
BPDA-PDA	0.209
TEOS	1.26

[a]Porosity determined by RBS.

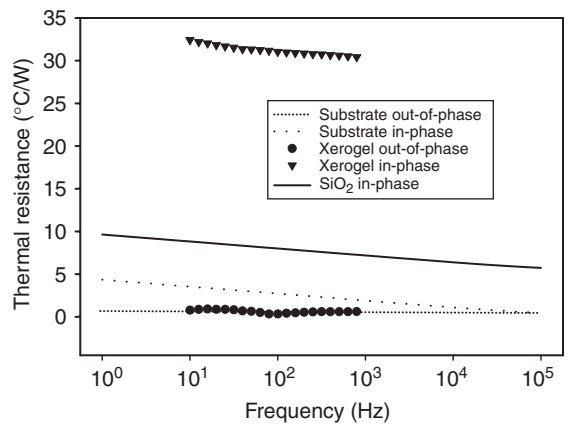

Fig. 3.7 Experimental 3ω data for in-phase and out-of-phase thermal resistance of a 0.60 μm thick 48% porous xerogel film. The calculated thermal resistance for the substrate and a SiO_2 film are also shown for comparison. Note that the thermal resistance is calculated from the in-phase component.

When $L_{th} \gg t$, there is negligible dissipation in the film, and the out-of-phase component of the 3ω signal of the film goes to zero. (There *is* dissipation in the substrate, but the substrate contribution is subtracted from the data.) Also shown in the figure for comparison are results for SiO_2.

3.3.5 New methods for porous materials

Several on-wafer techniques that were recently applied to characterize porous thin films are summarized in Table 3.5 and are illustrated using results from ~0.9 μm thick mesoporous silica films (a xerogel) from AlliedSignal, Nanoglass™ K2.2-A10B [58]. Three of the techniques listed in Table 3.5 are standard methods: MIS dot capacitors for dielectric constant measurements, Rutherford backscattering (RBS) and variable-angle spectroscopic ellipsometry (VASE). RBS and VASE have previously been used to measure the total porosity of thin films on Si substrates [61–63]. RBS directly measures the area density of the film, so the film thickness must be accurately known to determine the average film density, ρ. The chemical composition (stoichiometry) is also necessary for RBS to determine the area density, but RBS can provide compositions for heavier elements such as silicon, oxygen, and carbon. RBS cannot accurately quantify light elements such as hydrogen, and hydrogen content is often ignored when calculating the area

Table 3.5 Characterization data reported for a mesoporous silica film from AlliedSignal Nanoglass™ K2.2-A10B. Literature values are reported for TEOS oxide for comparison

Material property	Method	Nanoglass™ K2.2-A10B	TEOS
Dielectric constant (1 MHz)	MIS	2.29	~4.2
Film density	SXR	0.548 g cm^{-3}	2.0–2.25 g cm^{-3}
Matrix (connecting material) density	SANS	1.16 g cm^{-3}	2.0–2.25 g cm^{-3}
Total porosity	SXR	75.6%	
	RBS	76–79%	0
	VASE	71%	
Mesoporosity	SXR/SANS	52.9%	
Average pore size	SANS	6.48 nm	No pores
	PALS	7.5 nm	
Moisture uptake	SANS	2.99 wt%	~3–4 wt%
Modulus, CTE, T_g	Bending beam	Film too soft, $E < 1$ GPa (estimated)	E ~ 77 GPa CTE ~ 1 ppm °C^{-1}
CTE	SXR	62.2 ppm °C^{-1}	
Pore structure	SANS	22.4% of pore connected	No pores
	PALS	100% of pores connected	

density of oxide-based materials. The porosity is calculated from the average film density by volume averaging based on the density of its non-porous analog, that is, the density of the connecting material or the pore wall density, ρ_w. For oxide-based materials such as xerogels, the total porosity is commonly calculated using the relationship: $1 - \rho/\rho_w$ with the density of the connecting material (ρ_w) assumed to be the density of thermal oxide. The VASE technique can measure the total porosity by modeling the porous material using an effective medium approximation such as the Lorentz-Lorentz, Maxwell-Garnet or Bruggeman models [29, 37]. However, extreme care is necessary for data analysis because the porosity values can significantly vary depending on the model used and the operator. In Table 3.5, the RBS and VASE measurements on Nanoglass films are in reasonable agreement, but the total porosity measured by VASE is somewhat lower than both the RBS and SXR results for porous silica films.

3.3.5.1 Specular X-ray reflectivity

Specular X-ray reflectivity (SXR) [64, 65] provides a very precise and direct measurement of thin film density, and it has only recently been applied to characterize porous low-κ film up to 1 μm thick [46, 60, 66]. Like RBS and VASE, SXR alone can measure the porosity by comparing the measured film density to an assumed density of the non-porous material. SXR has an advantage over RBS in that the film thickness is not required for determining the average film density. Also, modeling is not needed to determine the porosity, as is the case with VASE.

In SXR, an incident beam of X-rays is directed toward the sample surface at an angle θ to the surface normal. When X-rays cross an interface between two media, they are refracted according to Snell's law: $n_1 \cos\theta_1 = n_2 \cos\theta_2$. The refractive index is $n = 1 - \delta + i\beta$, where δ is proportional to the electron density of the sample and β is related to absorption of X-rays. For most materials, the refractive index is less than one for X-rays with wavelengths of a few tenths of a nanometer. Hence, there is a critical angle defined as the grazing-incidence angle at which a well-collimated beam of X-rays is no longer totally reflected off the free surface, but starts penetrating into the sample. Below the critical angle, the X-rays undergo total external reflection, and the critical angle is given by:

$$\theta_c = \lambda \sqrt{\frac{\rho_c \gamma_c}{\pi}} = \sqrt{2\delta} \tag{3.14}$$

where λ is the wavelength, ρ_c the electron density, and γ_c the classical electron radius. Thus, the average electron density of a film is directly determined from the critical angle, and the average mass density of the film can be calculated if the sample stoichiometry (or chemical composition) is known. We typically use RBS (for quantifying heavier elements) and forward recoil elastic scattering (FRES, for quantifying hydrogen) to measure the chemical composition of the film [67]. SXR results are typically presented as the logarithm of the ratio of the reflected beam intensity to the incident beam intensity vs. Q_z as shown in Fig. 3.8 which displays SXR results

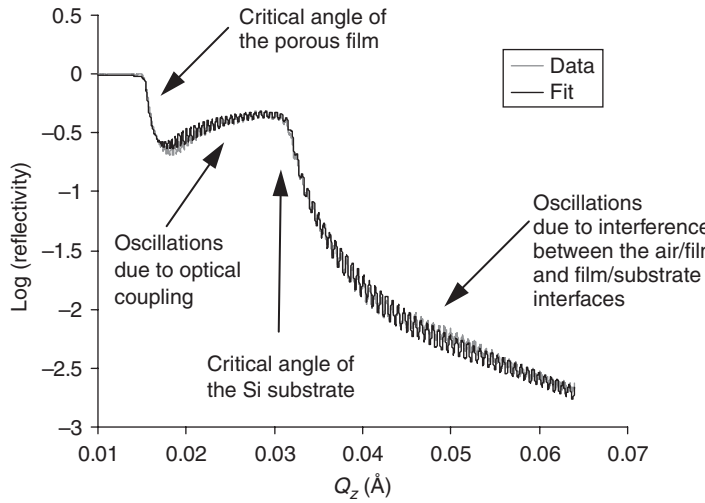

Fig. 3.8 Specular X-ray reflectivity curve showing the log of the reflectivity vs. the momentum transfer normal to the sample surface, Q_z, for 0.9 μm thick film of Nanoglass coated on a silicon wafer substrate. Also shown in the plot is the best fit to the data by modeling the film as a series of layers using a 1-D Schrödinger equation that gives an electron density depth profile for the film shown in Fig. 3.9. The steep drop near $Q_z = 0.0155$ Å is the critical edge of the film and corresponds to the average electron density of the film. The oscillations in the curve provide a sensitive measure of the film thickness.

from a 0.9 μm thick Nanoglass film on a silicon substrate. Q_z is the magnitude of the X-ray momentum transfer in the film thickness direction and is defined as $(4\pi/\lambda)\sin\theta$, where λ is X-ray wavelength and θ is the grazing incident angle. The data in Fig. 3.8 shows two critical angles. The first critical angle is that of the Nanoglass film, and an average film density of 0.548 g cm^{-3} is determined from this critical angle and the sample stoichiometry. The average film density is simply $\rho_w(1 - P)$, where P is the porosity. Assuming that non-porous Nanoglass has the same density as thermal oxide (assume $\rho_w = \rho_{oxide}$), then the total porosity of Nanoglass is calculated to be 75.6% which is in good agreement with the RBS measurement. The second critical angle corresponds to the electron density of the silicon substrate.

The oscillations between the first and second critical angles are due to optical coupling where the Nanoglass film acts as an X-ray waveguide. The oscillations at angles above the silicon critical angle are due to the interference of X-rays reflected from the Nanoglass film surface and the film/substrate interface. The film thickness is accurately determined from the spacing of these interference fringes. The vertical CTE is measured by measuring the film thickness at several temperatures [68]. The thickness of the Nanoglass film was measured at several temperatures up to 225°C from which an out-of-plane CTE of 62.2 ppm °C^{-1} was determined. The CTE measurement is corrected for the Poisson effect and substrate confinement using an assumed Poisson's ratio of 0.34. It is important to note that the interference fringes are attenuated or not

present if the film is too rough over the 2–5 cm^2 spot size. Thus, the thickness and CTE cannot be measured for films that have severe striations after spin coating. However, the density and porosity can still be determined.

SXR can also measure the density and porosity as a function of depth through the film thickness by modeling the electron density as a series of layers through the film using a 1-D Schroedinger equation [69]. Fig. 3.9 displays the depth profile results for the Nanoglass film. The results are consistent with a film having a uniform density except at the first few hundred Angstroms at the top and bottom interfaces. The modeling results in Fig. 3.9 ensure that the average film density determined by the Nanoglass critical angle is representative of the density through the entire film thickness.

Both SXR and RBS determine the total porosity from the average film density relative to the assumed density of the non-porous analog. However, the density of the connecting material between pores (pore wall density) is not necessarily the same as the density of the non-porous analog. Thus, for a mesoporous solid, SXR and RBS alone measure the total porosity in the film that includes any additional free volume (or micropores) in the connecting material that may not be present in the non-porous analog. For example, the density of the connecting material in Nanoglass may be much lower than that of thermal oxide.

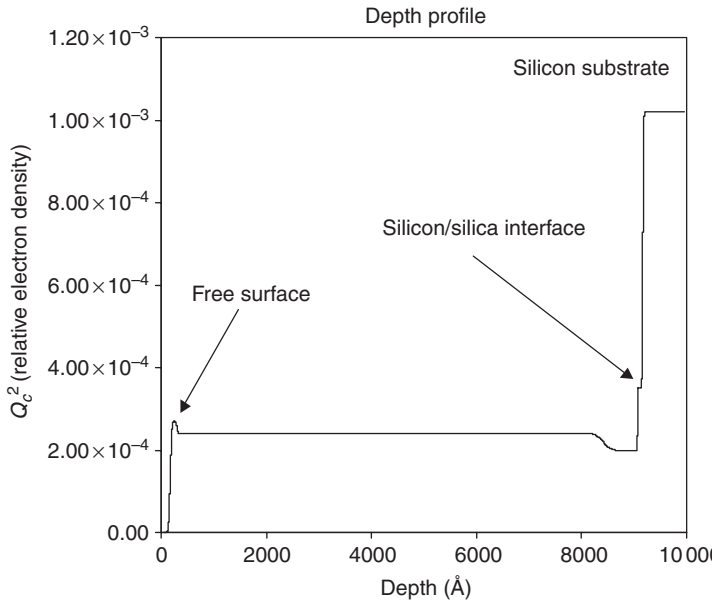

Fig. 3.9 The electron density space profile corresponding to the best fit to the data. At the free surface, a surface 'skin' about 5 nm thick with an electron density slightly higher than the bulk film is observed. A similar layer is observed at the film/silicon interface. The rest of the film has a uniform density.

3.3.5.2 Small-angle neutron scattering

Small-angle neutron scattering (SANS) is a complementary technique to SXR in that it can directly measure the density of the connecting material [46, 70]. The porosity calculated from the average film density (measured by SXR) relative to the pore wall density (measured by SANS) is the mesoporosity due only to the mesopores in the film.

The details of SANS experiments have been previously described [46, 70]. Briefly, a neutron beam is incident along the surface normal of the thin film sample on a silicon substrate. The resultant scattering vector, q, ranged from 0.01 to 0.18 Å^{-1}, where $q = (4\pi/\lambda)\sin(\theta/2)$, λ is the wavelength and θ the scattering angle from the incident beam path. For thin film samples (~1 μm thick), the scattering signal is enhanced by stacking several pieces of the sample together. The silicon wafer that supports the porous thin film sample is transparent to the neutrons, and the scattering angles of interest are due only to the porous film. The scattering contrast arises from the difference in the neutron scattering length of the connecting material and the pores themselves (the neutron scattering length is assumed to be zero).

To analyze the SANS data, the porous film is modeled using a density correlation function developed by Debye and coworkers [71] for random, two-phase structures: $\gamma(r) = \exp(-r/\xi)$ where ξ is the correlation length. Using this model, the average pore dimension (average pore size) or chord length is $\xi/(1-P)$ where P is the porosity. The SANS intensity based upon the Debye model takes the form of

$$\frac{1}{[I(q)]^{1/2}} = \frac{1}{(c\xi^3)^{1/2}} + \frac{\xi^2 q^2}{(c\xi^3)^{1/2}} \tag{3.15}$$

The quantities c and ξ can be determined from the slope and zero q intercept of the SANS data plotted as $[I(q)]^{-1/2}$ vs. q^2 as shown in Fig. 3.10. The SANS data in Fig. 3.10 follows the relationship in Eq. 3.15 except in the low-q region, indicating that the Debye model is a valid description of the Nanoglass film. The deviation in the low-q region is commonly observed in silica gels, crosslinked polymers and porous materials such as shale and is referred to as strong forward scattering. The quantity c in Eq. (3.15) is related to the porosity P and the mass density of the connecting material (pore wall density), ρ_w, as $P(1-P)\,\rho_w{}^2$. SXR measures the average film density, $\rho_w(1-P)$. Thus, from the slope and zero q intercept of the $[I(q)]^{-1/2}$ vs. q^2 plot and the average film density from SXR, the mass density of the connecting material (pore wall density) and the average chord length (a measure of the average pore size) can be calculated. For the Nanoglass films, SANS measured the pore wall density, ρ_w, as 1.16 g cm^{-3}, the mesoporosity as 52.9% and the average pore size (chord length) as 6.48 nm. The mesoporosity is much less than the total porosity. The total porosity is calculated assuming that the pore wall density is the same as that of thermal oxide. However, the pore wall density measured by SANS is much less than the density of thermal oxide (2.25 g cm^{-3}), indicating that the pore wall material has a lot of free volume or microporosity relative to thermal oxide. The pore size determined using

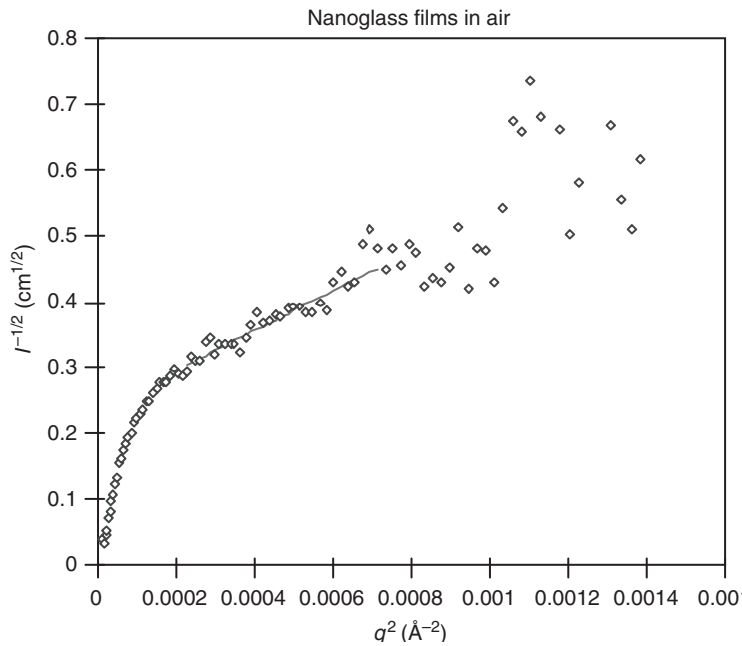

Fig. 3.10 Debye plot derived from an SANS experiment on a stack of Nanoglass thin films coated on silicon substrates. The slope of the fitted line provides the correlation length of the porous structure from which the chord length (average pore size) is calculated. The intercept of the fitted line at $q^2 = 0$ gives a measure of the porosity and the mass density of the connecting material between the pores (pore wall material).

SANS (6.48 nm) is in excellent agreement with a BET gas absorption measurement using a powdered samples [72]. Gas absorption is the conventional method to measure pore size and pores size distribution, but it is difficult to apply to 1 μm thick films coated on industry standard 8 in. silicon wafers [73].

SANS can also measure moisture uptake and the fraction of connected mesopores by immersing the sample at 25°C in deuterated water (*d*-water) and deuterated toluene (*d*-toluene), respectively [46]. As the mesopores are filled with a solvent, the scattering contrast changes which, in turn, changes the scattering intensity. If all of the mesopores are filled with *d*-toluene (or *d*-water), the SANS intensity is much larger than and is easily related to that of the dry sample. However, the scattering intensity of Nanoglass films immersed in *d*-toluene is much less than expected if all of the mesopores are filled. A two-layer model was developed to calculate the fraction of pores filled, and the analysis showed that 22.4% of the mesopores filled with *d*-toluene. This suggests that only 22.4% of the mesopores are connected to the Nanoglass surface, but the size of the *d*-toluene molecule may severely limit its ability to enter all the pores. In fact, a positron annihilation lifetime spectroscopy study demonstrated that all of the pores in Nanoglass are connected to the film surface. Similarly, SANS measures moisture uptake by

measuring the fraction of voids that are filled with deuterated water and then calculating the weight percent of water uptake. Nanoglass showed only 3.00% uptake of moisture.

3.3.5.3 Positron annihilation lifetime spectroscopy

Positron annihilation lifetime spectroscopy (PALS) [74–76] using radioactive beta-decay positrons is commonly used to study void volume in polymers. However, the high-energy beta-decay positrons are too penetrating (~0.3 mm) for thin film studies. Low energy beam PALS varies the beam transport energy to implant positrons to depths ranging from about 50–2000 Å [72]. Low energy beam PALS was used to determine the average pore size, pore structure and measure metal diffusion into Nanoglass [77].

Implanted positrons will interact with the material in a dielectric film in many ways as illustrated in Fig. 3.11. One fate of the positron is to form a hydrogen-like atom with an electron called positronium (Ps). Positronium has a vacuum lifetime of ~142 ns before it annihilates into gamma rays that can be detected. In porous films, the formation of Ps occurs preferentially in the voids of the film, and the Ps annihilation lifetime is shortened from the vacuum lifetime due to collisions with the pore walls. This effect provides a means of determining the average pore size from the Ps lifetime in the porous film. If all of the pores are connected, the Ps has a single lifetime as it samples all of the pores in the film, and a single average pore size is measured.

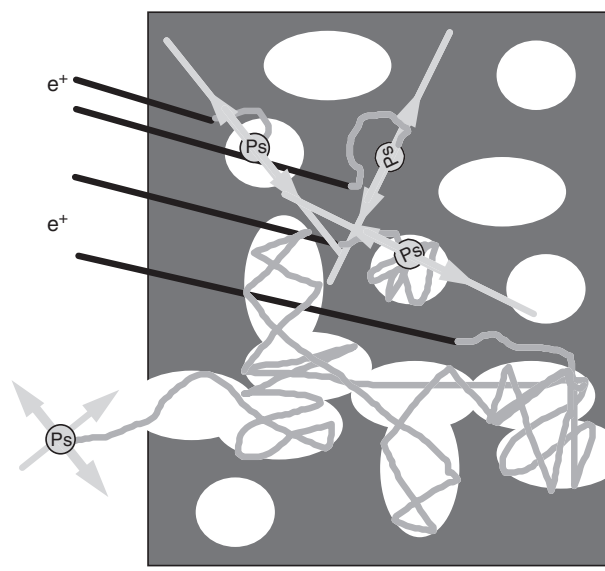

Fig. 3.11 An illustration of (PALS). The vacuum Ps lifetime (~142 ns) is shortened in the voids due to collisions with the void walls that increase the probability of annihilation into gamma rays. The Ps lifetime is measured by monitoring the gamma rays, and the lifetime is related to the average pore size.

If the pores are isolated, the Ps has many lifetime components each corresponding to a different pore size. Thus, in closed pore materials, PALS has the potential to provide pore size distribution information. PALS potential to measure pore size distribution in materials with isolated pores is very exciting, especially since gas absorption measurements of pore size distribution are limited if the gas cannot access the pores from the surface of the film.

The Ps lifetime in a Nanoglass film capped with a 100 nm TEOS oxide layer was 98 ns which corresponds to an average pore size of 7.7 nm. The average pore size measured by PALS is actually a mean free path, and it is somewhat different from the chord length measured by SANS. Nevertheless, the PALS result agrees reasonably well with the SANS and BET gas absorption results [60].

When the Nanoglass is not capped, all of the Ps diffuses out of the film and into the vacuum chamber giving a Ps lifetime nearly equal to the 142 ns lifetime in a vacuum. This observation demonstrates that all of the pores in Nanoglass are connected to the surface of the film. When Nanoglass films are capped using sputtered Al, keeping the film at ~25°C during the metal deposition, the sample exhibits the same 98 ns lifetime observed in the TEOS oxide capped samples. However, another 3 ns lifetime component appears with the 98 ns component when the sample is annealed. The 3 ns component indicates that Al is diffusing into the material and coating and closing some of the pores. The onset of Al diffusion into Nanoglass is ~450°C as determined from the appearance of the 3 ns Ps lifetime component (Fig. 3.12). At higher temperatures, the 3 ns component begins to dominate the 98 ns lifetime component as more Al diffuses into the film. Interestingly, if the Al cap is thermally evaporated (sample temperature $\ll$ 450°C), both lifetimes are present even without annealing the sample which indicates that some pores were coated and closed by mobile Al during deposition.

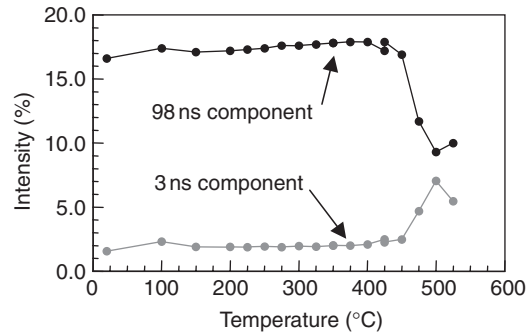

Fig. 3.12 Ps lifetime intensity as a function of annealing temperature after 1 h. for positrons implanted into a Nanoglass film capped with sputtered aluminum. The 98 ns component is characteristic of the 7.7 nm pores that were measured in TEOS-capped Nanoglass films. The 3 ns component is characteristic of pores coated and closed off by diffused aluminum.

3.4 Properties of low-κ materials

3.4.1 Thermomechanical properties

In addition to low dielectric constant, candidate ILDs must have sufficient thermal and mechanical stability to withstand the elevated processing temperatures and high stresses that can occur in the interconnect structure. Resistance to thermal decomposition is important because decomposition will severely degrade many other material properties of the dielectric, and outgassing of molecular fragments can cause other reliability problems, such as film delamination, blistering and via poisoning. Stability with regard to decomposition can be enhanced by strengthening chemical bonds and incorporating rings, crosslinks and network structures so that multiple bonds have to be broken in order for molecular fragments to be released.

Thermal stability with regard to decomposition is often determined using isothermal thermogravimetric analysis (TGA), which measures weight loss as a function of time at a given temperature. Few organic materials are thermally stable at the typical maximum BEOL processing temperatures of 400–450 °C used for subtractive Al processes. Cu processing, which can be as low as 350°C, allows a greater number of alternative materials due to the less demanding thermal requirements. More stable organic materials typically incorporate double bonds and aromatic structures. Thermal decomposition is less of a problem for inorganic silica-based materials, including SOGs. However, Si–H and Si–C bonds in some of these materials are still susceptible to decomposition at elevated temperatures, especially in an oxygen-rich environment [78, 79].

Mechanical strength is another important requirement, because if the film cannot withstand stresses occurring during processing, structural integrity of the interconnect will be compromised. For example, thermal stresses can lead to extrusion in the metal lines or buckling of overlying layers [4]. Additionally, CMP processes can severely damage films that do not have sufficient mechanical strength. The value of the elastic, or Young's modulus (E) is often used as an indication of mechanical stability for low-κ candidate materials. Young's modulus of most organic and inorganic low-κ candidate materials is at least an order of magnitude lower than that of standard SiO_2 films prepared from tetraethoxysilane (TEOS) ($E \sim 59$ GPa) [32]. As a result, the mechanical reliability of these alternative dielectrics is an important integration concern.

In addition to the modulus, the film's CTE is also of importance, since most of the stresses that occur in the interconnect are thermally induced, resulting from CTE mismatches between various materials in the interconnect structure. For example, the CTE of SiO_2 is 0.5 ppm °C^{-1}, Cu is 16.5 ppm °C^{-1}, Al is 23.1 ppm °C^{-1} [78]. The CTE of many organic dielectrics is $>$ 50 ppm °C^{-1}, which can lead to high tensile stresses in the film following high-temperature processes. It would be desirable to minimize the thermal mismatches, especially for dielectrics with a low modulus, by using a low CTE dielectric. Table 3.6 summarizes data on thermal stability, mechanical strength, and thermal expansion for a number of low-κ materials.

Table 3.6 Selected dielectric and thermomechanical properties of low-κ thin films

Material	κ	Young's modulus (GPa)	Lateral CTE 25–225°C (ppm °C^{-1})	T_g (°C)	TGA % weight loss (425°C, 8 h)
PTFE	1.92	0.5	135	250	0.6
BPDA-PDA	3.12	8.3	3.8	360	0.4
Crosslinked PAE	2.8–3.0	2.7	52	350	2.5
Fluorinated PAE	2.64	1.9	52	>400	×
BCB	2.65	2.2	62	–	30
SiLK	2.65	2.3	54	–	2.1
Parylene-N	2.58	2.9	55–100+	425 (melt)	30
Parylene-F	2.18	4.9	33	–	0.8
HSQ	2.8–3.0	7.1[a]	20.5	–	×

[a]Biaxial modulus.
×, Not measured; –, none observed.

Thermal conductivity is another important material property and a high value is desirable to minimize Joule heating, which poses a reliability concern for high-density interconnect structures. Table 3.7 summarizes the thermal conductivity data obtained by the 3ω and photothermal technique in our lab. The values of thermal conductivity of all candidate materials tested so far are significantly lower than for TEOS. Many polymers have thermal conductivity of about 0.2 W m^{-1}K^{-1} and heat transport seems to be best in the dense and crosslinked polymers. The thermal conductivity for the OSGs and porous materials scale to a first approximation with their density. However, the thermal conductivity decreases much faster than the density at high porosity, with the thermal conductivity being lower by a factor of 20 as compared to TEOS for 77% porosity. The porosity effect on thermal conductivity for organosilicate films will be discussed further in a later section.

3.4.2 Structure property relations

3.4.2.1 Polymers

The low value of dielectric constant of fluorinated organic materials like PTFE is due to the consequent use of molecular bonds with lowest polarizability (from the top of Table 3.1). PTFE, which consists of singly bonded carbon chains saturated with fluorine atoms, has one of the lowest κ values (~1.9) of any non-porous material. One drawback of PTFE is that the flexible and uncrosslinked chain structure limits the thermomechanical stability of the material. For example, one PTFE material evaluated in our laboratory was found to have a low yield stress (12 MPa), low elastic modulus (0.5 GPa), low softening temperature (~250°C), and high CTE (>100 ppm °C^{-1}).

Table 3.7 Thermal conductivities for several low dielectric constant materials

Material	Dielectric constant	Thermal conductivity ($W m^{-1} k^{-1}$)
TEOS	4.0	1.26
	POLYMERS	
PMDA-ODA	3.2	0.22
BPDA-PDA	3.12	0.21
PTFE-based	2.15	0.19
BCB	2.65	0.24
OSG		
13%	2.69	0.34
28%	2.64	0.20
30%	2.60	0.21
	POROUS MSQ	
Matrix I	2.82	0.30
	2.36	0.22
	2.20	0.17
Matrix II	2.23	0.22
Matrix III	2.39	0.26
Matrix IV	2.41	0.19

A second issue for PTFE, which is a concern for all fluorine-containing materials, is the potential release of fluorine atoms that can cause corrosion of metals or other reliability problems in the interconnect structure.

Better thermomechanical properties compared to PTFE can be obtained by incorporating a stiffer polymer chain or by crosslinking the chains. Classic examples of stiff-chain polymers are the aromatic polyimides, which have a rigid backbone due to the aryl and imide rings incorporated into the chain. This can raise the modulus to 8–10 GPa and the T_g to 350–400°C [34]. However, the rigid chain structure causes the polyimide chains to align preferentially parallel to the substrate, especially when deposited as thin films, which results in anisotropic material properties [81–87]. The thermomechanical properties are likewise anisotropic. For instance, the CTE of thin films of rigid polyimides is often $\leqslant 10\,ppm\,°C^{-1}$ in the plane of the film, but can be more than 10 times larger in the out-of-plane direction [87].

The spin-on poly-aryl-ether (PAE) materials result from attempts to balance the dielectric and thermomechanical properties of the material. The aryl rings in these materials provide better thermomechanical properties than PTFE and the flexible aryl linkages allow bending of the chains that results in a more isotropic material than PIs. PAEs typically have a κ value of 2.8–2.9,

while typical values for the modulus and CTE are 2.0 GPa and 50–60 ppm °C^{-1}, respectively. Resistance to thermal decomposition can be quite good for PAEs; weight losses of only ~2% over 8 h at 425°C has been observed in TGA experiments. One drawback of uncrosslinked PAEs is that they have a relatively low T_g of ~275°C. In order to raise the T_g, reactive functional groups can be incorporated along the backbone, which allows for crosslinking of the film during cure. Experiments conducted in our laboratory have shown that crosslinking of PAEs can increase the T_g to over 450°C. The effects of crosslinking on T_g are shown in the stress curves of Fig. 3.13. Unfortunately, crosslinking can also lead to a corresponding increase in the κ value if the crosslinking is not optimized. Therefore, careful control of the crosslinking chemistry is necessary to improve the material stability without sacrificing the dielectric properties.

Because it is difficult to obtain high T_g values in uncrosslinked polymers, efforts have been made to use polymers that crosslink into a three dimensional network upon curing. Two spin-on examples of these organic thermosets are the bis(benzocyclobutenes) (BCB) [88, 89] and SiLK™ thermosets [5, 88] produced by Dow Chemical, both of which are highly aromatic. The thermomechanical properties of these films (E = 2–3 GPa, CTE ~ 60 ppm °C^{-1}) are comparable to the PAEs, but they have a somewhat improved κ of 2.65. In the case of BCB, the low-κ value results partly from the incorporation of relatively non-polarizable aliphatic rings in addition to the aromatic rings. The large number of rings and crosslinking makes these materials quite rigid, so that they do not show a T_g below 450°C [90], although the relatively weak Si–C bond in BCB results in thermal decomposition of this material above 350°C. The thermal stability of SiLK™ is significantly better, as the material shows very low thermal weight loss (~2% over 8 h at 425°C) and good interfacial adhesion, raising the potential of this material for successful integration into the interconnect structure.

3.4.2.2 Silsesquioxanes

Since mechanical and thermal stability is difficult to obtain using purely organic materials, there has been much interest in inorganic or inorganic/organic hybrid materials. The strategy behind the silica based materials is to use the much stronger and more rigid SiO_2 network as a starting point, and to lower the κ value by reducing the density through the incorporation of organic chemical substituents or voids into the film. The silsesquioxanes are one such class of hybrid OSGs. Thin films of OSG can be deposited by a CVD process using methylsilane and an oxidizing agent or by a spin-on process using silsesquioxanes, then often called spin-on glasses (SOGs). In the silsesquioxanes each Si atom is bonded to one terminating group such as hydrogen, methyl or phenyl, resulting in a nominal stoichiometry $SiO_{1.5}R_{0.5}$. Both the crosslinking density and material density are reduced due to these terminating groups. The organic content in the films can be varied by the CVD process conditions or by the curing conditions after spin-on. The dielectric constant of these materials is in the range of 2.5–3.0. The reduction in κ from that

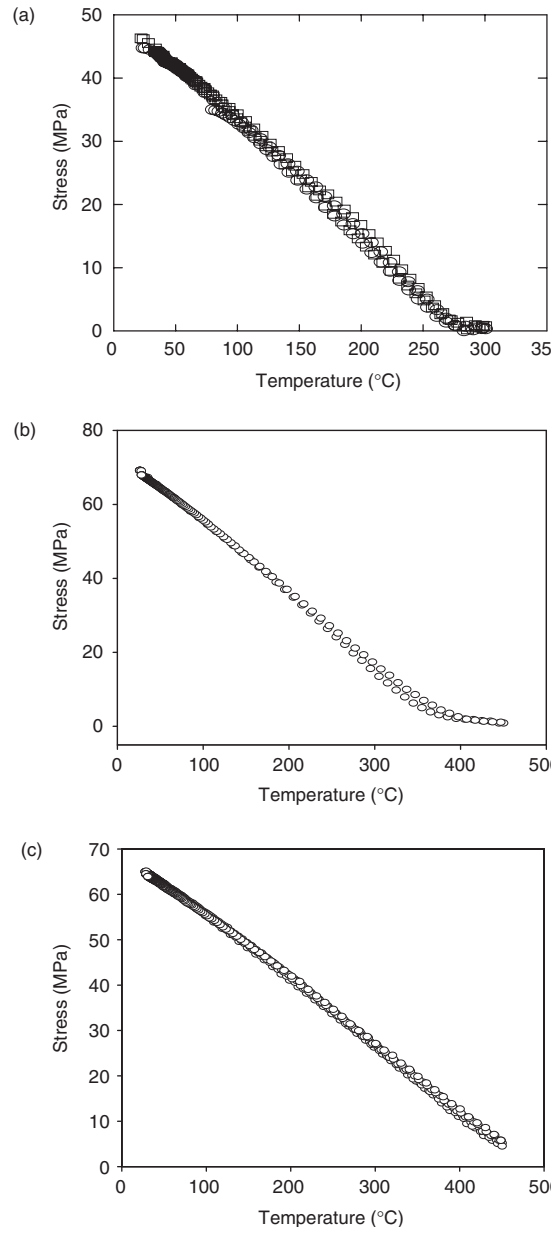

Fig. 3.13 Thermal stress measurement of (a) uncrosslinked, (b) partially crosslinked, and (c) fully crosslinked PAE film, showing an increase in the T_g from 275 to $>450\,°C$. A corresponding rise in κ from ~2.9 to 3.1–3.2 was observed for these films.

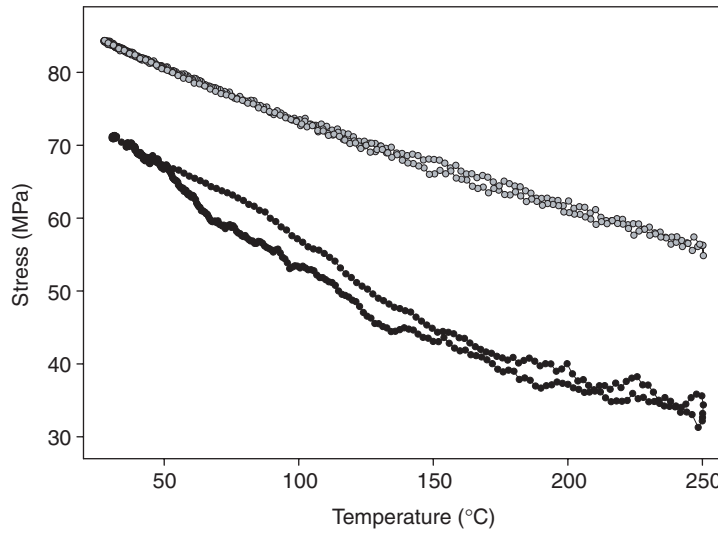

Fig. 3.14 Thermal stress measurements for two different OSGs on Si. The lower curve is more noisy because it was obtained from a film on a 700 μm thick substrate, after extending the light path to 6 m.

of SiO_2 is thought to be mainly due to the reduction in density. For example, the density of hydrogen silsesquioxane (HSQ) ($k = 2.8$–3.0) can be about one-third less ($1.4\,g\,cm^{-3}$) [91, 92] than that of TEOS (2.2–$2.4\,g\,cm^{-3}$).

The mechanical properties of the materials are generally superior to most organic polymers. For instance, our laboratory has determined a biaxial modulus of 7.1 GPa and CTE of $20.5\,ppm\,°C^{-1}$ for HSQ. The latter value is in good agreement with X-ray reflectivity measurement [68]. Black Diamond, a CVD film from Applied Materials (version April '99) analyzed in our lab showed FTIR spectra similar to those of a HSQ/MSQ hybrid. The material had a carbon content of 13%. It should be noted that the carbon contents for the OSG's reported here were measured by XPS and therefore do not account for the hydrogen present in the films. Typical for these materials are stress vs. temperature curves which bend towards smaller slopes at elevated temperatures, as shown in Fig. 3.14. The CTE for this version of Black Diamond was $23\,ppm\,°C^{-1}$ and the biaxial modulus was 7.7 GPa at temperatures below 100°C. Above 100°C the CTE is $22\,ppm\,°C^{-1}$ and the biaxial modulus dropped to 6.1 GPa. As the oxide network provides the rigidity of the structure, the mechanical properties decay with increasing organic content. Results from bending beam experiments on OSGs, with systematically varied carbon contents but otherwise similar process conditions are shown in Fig. 3.15. The data show a clear trend towards larger negative products of $E \cdot \Delta\alpha$ with increasing carbon content. The negative sign of $E \cdot \Delta\alpha$ is due to CTEs larger than silicon, the increasing absolute numbers show an increasing tendency to build up thermal stresses. Assuming that the biaxial modulus does not

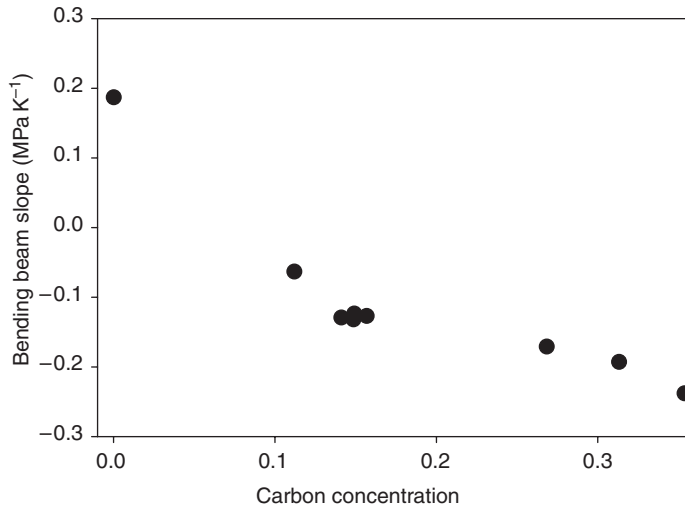

Fig. 3.15 Slopes ($E{\cdot}\Delta\alpha$) of stresses vs. temperature for OSGs as function of carbon content (excluding H). TEOS is shown at 0% for comparison.

increase with carbon content, the data show an increase of CTE with carbon content. Since the modulus of the material most likely decreases when the Si–O bonds, which provide the rigidity of the structure, are replaced by more and more organic groups, the decrease in modulus will occur together with increasing CTE. This indicates a tradeoff between a lower dielectric constant, which can be achieved by increasing the number of organic groups and the thermomechanical properties of these materials.

Many types of SOGs experience a large amount of shrinkage during curing that leads to high tensile stresses that can crack the films. This often limits the maximum thickness of these films to only a few thousand angstroms. The methyl silsesquioxanes (MSQ) undergo much less shrinkage, are less prone to cracking, and therefore can be prepared about 1 μm thick [93].

Resistance to thermal decomposition for silsesquioxanes is generally better than that of most organic films due to the increased stability of the silica network. For example, AlliedSignal has reported no outgassing in TDMS experiments conducted on an MSQ film at 450°C [93]. However, HSQ is susceptible to oxidation at temperatures over 350°C, which produces a denser, higher κ film having a reduced number of Si–H bonds [91, 94]. Oxidation can also form terminating –OH groups that bind water. Oxidation appears to be less of a concern for OSGs with a higher content of carbon, due to the better stability of the Si–C bond relative to Si–H. Still, OSG films are prone to oxidation, leading to a small increase in weight in TGA experiments when traces of oxygen are present. Oxidation usually leads to a decrease in the number of Si–H bonds as seen in FTIR and to a larger dielectric constant, as the material becomes more oxide like. As a result, OSG films are often cured in an inert environment and capped with oxide.

3.4.2.3 Microporous materials

Since very few dense materials have a κ less than 2.5, there has been much interest in fabricating porous materials in order to reach ultra low-κ values ($\leqslant 2.0$). Most of these materials are not as well developed as the fully dense dielectrics. Nevertheless, a wide variety of porous materials have been produced to date, and some initial integration studies have been done [60]. Thin porous films are generally made in one of two ways; either through direct construction of a porous network, or indirectly by depositing a composite film, a component of which is later removed. The first type of material is often produced by a gel process in solution [95–97] and includes the aerogel and xerogel porous silica films, which have traditionally been dried either supercritically [98] or by evaporation [99]. Preventing collapse of the porous network due to capillary forces during drying is key for these films.

There are several possibilities using the indirect method [100]. For example, one can incorporate a surfactant [101] or dendritic structure [97] as a thermally degradable template, or porogen, build what will become the porous film around this template. Subsequent heating leads to porogen decomposition and diffusion out of the matrix. Under optimum processing conditions, a porous network results in where the pore size directly correlates with the porogen morphology. This approach is applicable to a wide range of materials, both inorganic and organic, and to a range of porogen structures. For example, porous silsesquioxanes, such as DendriGlass, are based on the blending of organosilicates, such as phenylsilsesquioxane, with a polyeric porogen [103, 104].

There are a number of reliability concerns that are particularly prominent for porous ILDs. One concern is the mechanical strength, since films with voids will undoubtedly be weaker than their fully dense analogs. Another set of potential problems involves the size and distribution of the pores in these materials. It is critical to the reliability that these parameters be carefully controlled. For instance, if pores are too large, feature sizes and shapes will not be well defined during integration. Also, if the pores percolate together to form channels, the material may have a low breakdown voltage and mechanical strength and prone to absorption of process chemicals.

As mentioned above, an important reliability concern for porous materials is their mechanical strength. Studies of highly porous bulk aerogel materials show that the Young's modulus scales with at least the second or third power of the density [105, 106]. This suggests that the mechanical strength of ILD films will deteriorate very quickly as voids are introduced. At our laboratory recently the material properties of porous MSQ films processed at IBM were investigated using the porogen-dendrite method. Properties studied include the dielectric constant using C–V measurement, the thermal conductivity using the 3ω technique and the thermal stress behavior using the substrate curvature technique [106]. The porosity ranges from 0 to 50%, which provides an opportunity to study the effects due to a transition in pore morphology from closed-cell to interconnect open-cell structure at the percolation limit. Results are summarized in Fig. 3.16. The dielectric constant decreases with increase in porosity, following closely

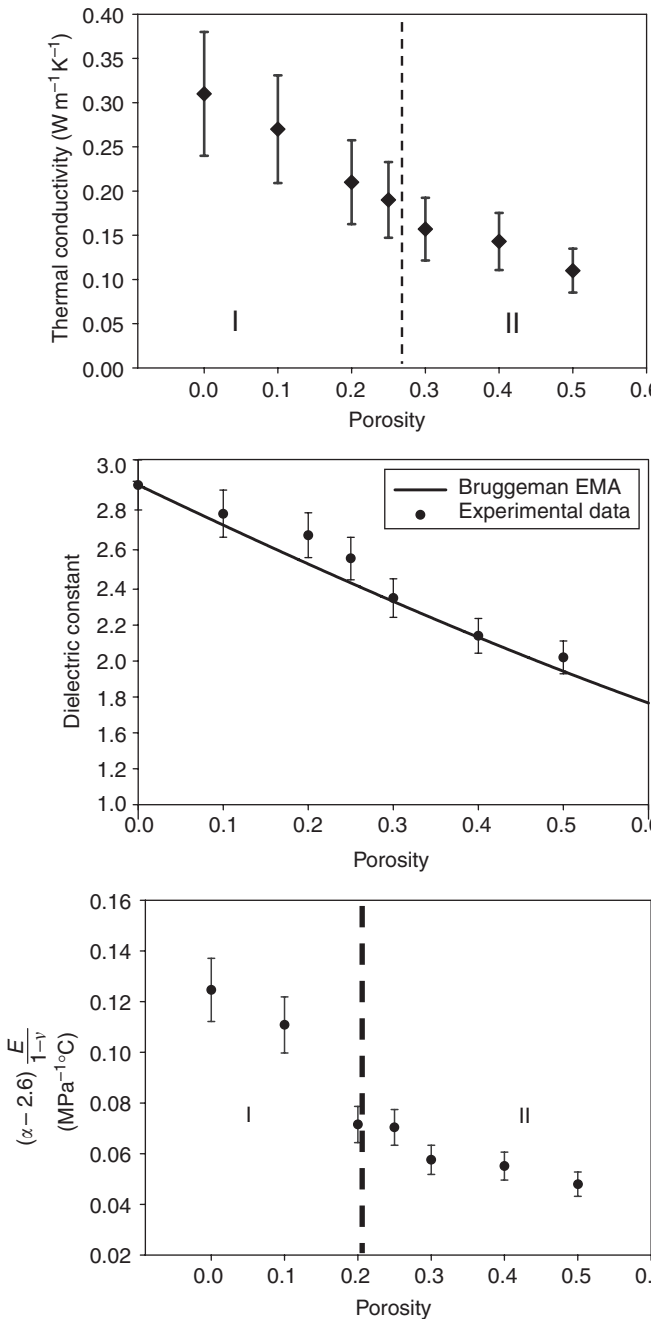

Fig. 3.16 Porosity dependence of material properties of porous MSQ films: (a) dielectric constant (curve shows the Bruggeman EMA); (b) thermal conductivity; and (c) thermal stress. In (c), the slope of thermal stress vs. temperature is shown, where 2.6 ppm °C^{-1} is the CTE of the silicon substrate and $E(1-\nu)^{-1}$ is the biaxial modulus. The transition from region I to region II due to percolation is clearly observed.

the Bruggeman's effective medium approximation (EMA). The effect of percolation on κ is not clearly observed although a small break in κ may exist at 25% where percolation is expected. Similarly, the thermal conductivity decreases with increasing porosity, reducing from $0.35\,W\,m^{-1}K^{-1}$ for the fully dense material to $0.12\ W\,m^{-1}K^{-1}$ with 50% porosity. Again, the percolation effect is not clearly observed. At the bottom of Fig. 3.16, the slope extracted from the stress-temperature curve, $E(1-\nu)^{-1}\ (\alpha - 2.6)$ MPa °C^{-1} (2.6 ppm °C^{-1} is the CTE of the Si substrate), is plotted vs. porosity. In contrast, this thermomechanical property shows a clear effect due to percolation with a drop from 0.11 to about 0.07 MPa °C^{-1} at 20% porosity. For low porosity material, the thermal expansion is close to that of the matrix material. Therefore, the decrease in the slope reflects a significant drop in the elastic modulus of the material when it changes from a closed-cell to an open-cell structure. This may have a significant impact on the reliability of Cu/low-*k* interconnect and that has yet to be investigated.

The thermal conductivity data for various porous materials, given in Table 3.7 are plotted against their dielectric constant in Fig. 3.17. For porous MSQ and silica films, the thermal conductivity seems to follow a similar linear relationship with the dielectric constant. Based on the Bruggeman's EMA, the dielectric constant scales approximately linearly for small percentages of porosity, or to the average density of the matrix material. The linear correlation observed suggests that the thermal conductivity is also related to the density of the matrix material, which is the oxide skeleton for porous MSQ and silica. As lower density is the main mechanism to lower the dielectric constant of these materials, there is a fundamental tradeoff between a low dielectric constant and thermal conductivity. The sharp drop in the thermal conductivity for higher

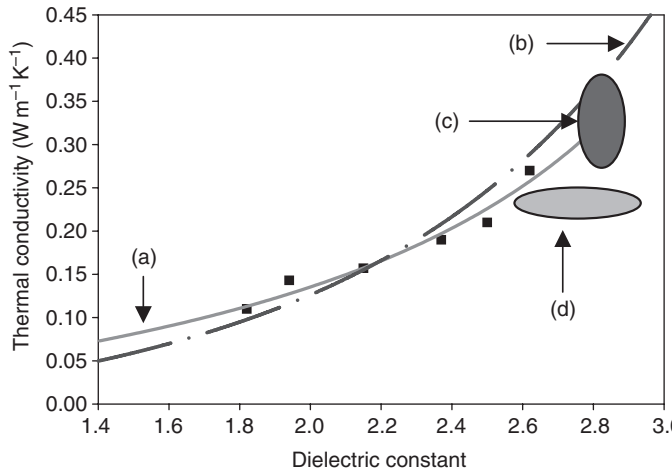

Fig. 3.17 Correlation of thermal conductivity and dielectric constant for low-κ materials; symbol (■) represents the experimental data for porous MSQ films; curve (a) is for porous MSQ film and curve (b) for porous silica films; oval (c) includes various fully dense OSG materials and (d) includes various fully dense low-κ polymers.

percentage of porosity as observed for the xerogels indicates that there are other mechanisms further reduce the thermal conductivity. In general, a carefully tailored matrix material and a proper pore structure, preferably one with closed cell structure, are important for optimizing the properties of porous low dielectric constant materials. Clearly, a great deal of work will be required to correlate the structures with the thermal and mechanical properties.

3.5 Summary

Low-κ dielectrics have to meet stringent requirements in material properties in order to be successfully integrated. A particular difficult challenge for material development is to obtain a combination of low dielectric constant with good thermal and mechanical properties. The basic difficulty is that the strong chemical bonds that impart structural stability are the most polarizable, thus yield a high dielectric constant. There are a variety of characterization techniques available for thin film characterization and several of them which allow for on-wafer characterization have been discussed in detail in this chapter. Several promising candidate materials with κ of 2.7–3.0 have been developed and integrated into Cu damascene interconnects.

The next phase development of porous materials with $\kappa < 2.5$ seems more challenging since the incorporation of porosity degrades further the thermal and mechanical properties. The scaling of layer thickness with device dimensions presents challenges for the characterization metrology itself. Several methods have been developed to characterize the structure and properties of thin porous films but much work remains to be done to understand how the porosity affects the macroscopic properties of the films, particularly the thermomechanical properties. The porosity, pore structure, surface area and surface chemistry on the pore walls all affect the dielectric constant and the mechanical strength and uptake of moisture or other solvents. Results from characterization of porous MSQ films show that the dielectric constant follows the Bruggeman's EMA and the correlation with the thermal conductivity suggests that both properties scale with the average density of the material. However, data from the slope of the stress–temperature curve show a significant drop in the thermomechanical property beyond the percolation when pores become interconnected. These observations suggest that the amount of porosity should be minimized and with pores preferably in closed cell form. Thus there is a definite advantage of using starting materials with a lower κ value and to limit the pore percolation in developing porous dielectrics. With the current intense effort in integrating Cu and porous low-κ interconnects, the material properties, particularly the thermomechanical properties, will have significant impact on yield and reliability. A great deal of work will be required on metrology, characterization and reliability study of porous low-κ materials to ensure successful integration of future Cu/low-κ interconnects.

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Interlayer Dielectrics for Semiconductor Technologies
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Chapter 4
Compatibilities of dielectric films

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Abstract

Interface reliability has become a primary focus of advanced semiconductor development as dielectric materials transition from oxides and nitrides to polymers and carbides. Packaging reliability, transistor performance, RC delay, electromigration, and stress migration resistance all have dependencies on interface properties. Process and environmentally induced damage are shown to be critical contributors to the properties of interfaces formed between dielectrics and metals, semiconductors, and other dielectrics. Adhesion promoters, plasma pre-cleans, wet pre-cleans, queue times, design rule changes, low downforce polishing, and resist stripping changes have all been employed to improve the compatibility of emerging dielectrics with other materials and with process, performance and reliability requirements.

4.1 Introduction

Due, in part, to geometrical scaling and the scaling of Young's modulus, material compatibility has become a central focus of semiconductor development in order to manipulate (i.e. engineer) interface properties to achieve required electromigration resistance, package reliability, RC delay, and transistor performance. When assessing the compatibility of different materials, adhesion, mismatch of thermal expansion coefficient (TCE), interface composition, and interface roughness are amongst the commonly compared metrics.

Performance and reliability depend on the properties of interfaces between dielectrics and metals, dielectrics and semiconductors, and interfaces between different dielectric materials. Silicon roughening and trapped charges at the interface of gate dielectric and silicon have been one of the most extensively studied examples of the importance of interface engineering. The proliferation of low-density low-dielectric-constant materials has exposed severe reliability issues that surface long before the device is packaged. The interface between copper interconnects and dielectric diffusion barriers has been demonstrated to be critical for electromigration performance of advanced semiconductor devices.

Interface adhesion depends on chemical bonding across the interface and stresses in the films adjacent to the interface. Poor adhesion can be improved by (a) modifying interfacial chemistry (e.g. surface treatments, adhesion promoters), (b) changing the stresses in the structure, and (c) modifying stress singularities associated with the structural design [1].

This chapter includes an overview of key interfaces and interactions between dielectrics and metals, dielectrics and semiconductors, and between different dielectrics for advanced semiconductor technologies. An overview of each of these interfaces is presented for porous and dense dielectrics, organic and silicon-based materials.

Due to the advancements in analysis techniques, interfaces are better understood and can be engineered more directly. Comparisons of different methods for detecting interactions by chemical analysis, imaging, and adhesion testing are presented.

The correlation of interface properties on unpatterned substrates to patterned product wafers is discussed, including the influence of etch and resist strip damage, tiling, slotting, moisture absorption, and thermal cycling. Modeling is presented as a method to predict interface reliability and the impact of material changes and interface modifications. The impact of dielectric interface properties on performance and reliability issues such as chemical–mechanical polishing (CMP) compatibility, packaging reliability, as well as transistor performance, RC delay, and electromigration (EM) resistance, is also addressed.

4.2 Interfaces between dielectrics

The interlayer dielectric (ILD) shares common interfaces with several other dielectrics in inlaid integrations. As shown in Fig. 4.1, the lower ILD interface is formed between the ILD and dielectric barrier, and the upper ILD interface can be formed with an anti-reflective coating (ARC), a capping layer, hardmask, etch stop, or dielectric barrier. The term ‘dielectric barrier’ is being used to describe a dielectric layer that functions as a copper diffusion barrier. As described in Chapters 5–9, ILD candidates consist of dense and porous versions of silicon dioxide, fluorine-doped silicon dioxide, silicon oxycarbides, and polymers. Some integrations have been described using multiple ILD materials in a given stack, resulting in additional dielectric interfaces [2]. Emerging low-κ materials commonly exhibit integration challenges associated with low elastic moduli and TCE mismatch, resulting in high film tensile stress and poor adhesion [3, 98].

This section will describe the properties of different dielectric interfaces, emphasizing how porous materials behave differently from dense dielectrics, and how silica-based materials differ from polymeric films. Some of these interfaces are present in the manufactured chip, and other interfaces are present only during segments of chip manufacturing and are eliminated during subsequent subtractive processing (e.g. etch, CMP – chemical mechanical polishing). The examples in this section are restricted to inlaid metal integrations, using copper as the interconnect metal.

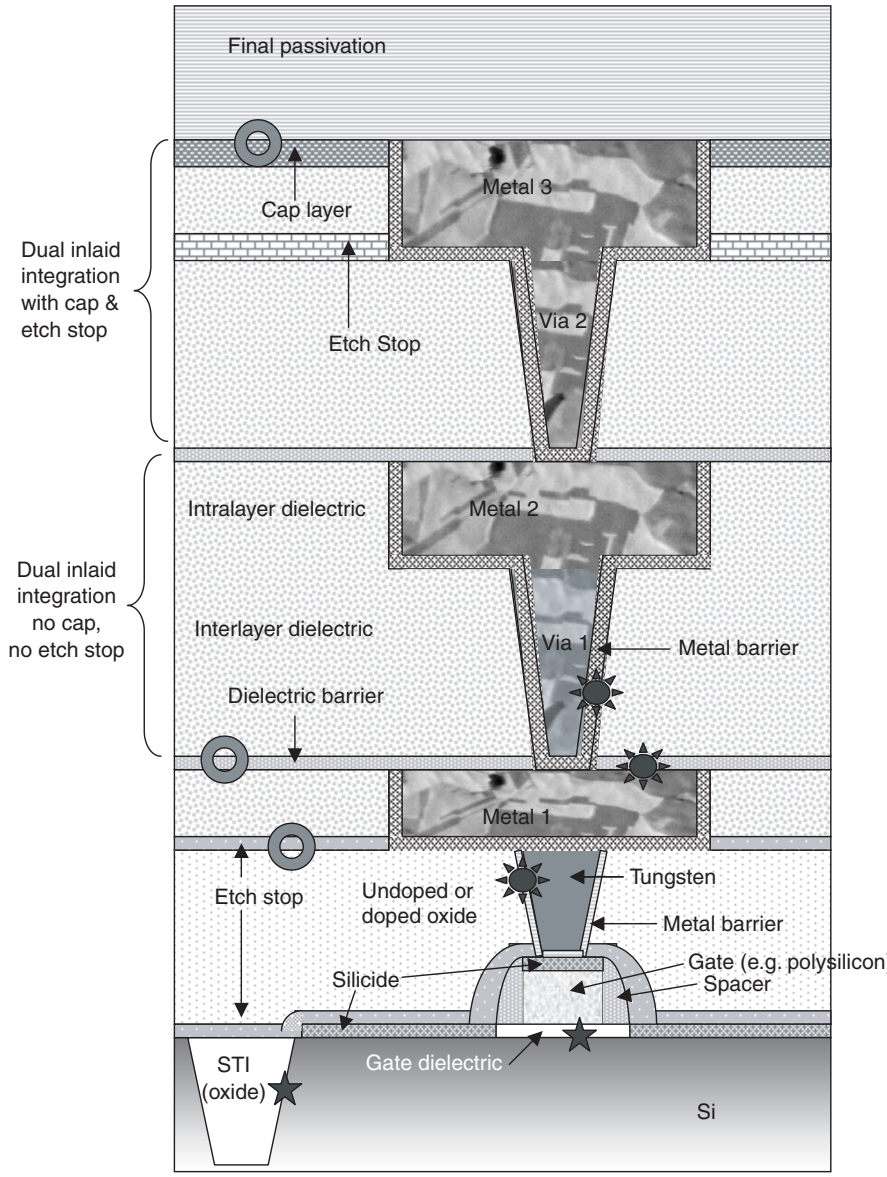

Fig. 4.1 Drawing of semiconductor device. ◎, Denotes interfaces between dielectric materials; ✷, denotes interfaces between metals and dielectrics; ★, denotes interfaces between dielectrics and semiconductors.

For low-κ dielectrics, interfaces to capping layers generally have different properties as compared to underlying layers, and this section is organized to reflect the differences between underlying and overlying interfaces of low-κ dielectrics.

4.2.1 Interfaces between ILD and underlying dielectrics (e.g. dielectric barriers)

Silicon nitride and silicon carbide, deposited using plasma enhanced chemical vapor deposition (PECVD), are the most commonly used dielectric barriers to copper diffusion. Silicon carbide films are replacing nitrides as dielectric barriers, etch stops, hardmasks, and capping layers due to lower dielectric constants ($\kappa \sim 3$–5 for $SiC_xN_yH_z$ versus 6–9 for SiN_xH_y) and improved etch selectivity with respect to many low-κ dielectric films. Interfaces formed between the ILD and SiN or SiC (e.g. SiOF/SiN) are described for various ILD materials.

4.2.1.1 Interfaces between silicon-based dielectrics and underlying dielectrics

Unlike polymers, silicon-based ILDs benefit from more similar chemical composition to conventional dielectric barriers. Fluorinated silicate glass (FSG) dielectrics were introduced to replace standard SiO_2 with a lower dielectric constant material. Although many mechanical properties are similar between the doped and undoped glasses, the potential mobility of fluorine can result in interface properties quite different from standard SiO_2.

Fluorine from FSG films segregates to interfaces with Si_3N_4, TaN, and Ta [4]. If the concentration of free fluorine is too high, fluorine pileup at these interfaces can lead to void formation and delamination. This fluorine mobility is enhanced by exposure of FSG to moisture and thermal cycling. FSG deposited using SiH_4 as the silicon source has been shown to be more susceptible to fluorine mobility than TEOS-based FSG. Although there have been reports of poor adhesion between FSGs and overlying SiN [5] due to fluorine segregation, there have been no reports of adhesion failures of the FSG to an underlying SiN. This may be due to the potential for moisture absorption at the polished FSG surface between CMP and SiN deposition process steps, whereas there is typically less moisture exposure at the underlying FSG/SiN interface.

Donaton *et al.* [6] observed no adhesion failures between low-κ SiOC films and SiC dielectric barrier films.

4.2.1.2 Interfaces between porous dielectrics and underlying dielectrics

As a result of the reduced elastic moduli of porous dielectrics, cohesive strength of the porous material is commonly weaker than the adhesion strength at the underlying interface. Cohesive failures are associated with fracture and crack propagation within the bulk of the film as compared to crack propagation along an interface for adhesive failures.

Porous SiO_2 films have been found to fail tape test for adhesion to underlying dense SiO_2 [7]. The presence of an interface failure suggests that the cohesive strength of the porous SiO_2

exceeds the adhesive strength to the underlying substrate. The use of adhesion promoters and/or pre-cleans may be required to provide adequate adhesion between porous SiO_2 and underlying dielectrics

Adhesion promoters are commonly used to enhance adhesion between spin-on porous polymers and underlying dielectric barriers or etch stops. Porous polymers, such as the porous SiLK material, have shown cohesive failures during adhesion testing to underlying Si, SiC, and SiO_2. The cohesive failures occurred with a measured fracture toughness of 0.36 MPa $m^{1/2}$ using the modified edge liftoff technique (m-ELT) [12, 25]. By improving the interfacial adhesion, the cohesive strength became the dominant failure mode. This result for porous SiLK differs from the failure mode of the dense SiLK, described in Section 4.2.1.3.

When cohesive and adhesive strengths are comparable, a mixture of failure modes may be observed, with failure modes changing depending on the testing method. Integration of a porous organosilicate glass (OSG) material, with an elastic modulus of ~0.36 GPa, resulted in delamination during CMP at the interface with the OSG and underlying SiN film. However, tape test of the same interface suggested a cohesive failure, near the SiN interface [9].

The presence of cohesive failures are a function of low modulus and also interface adhesive strengths exceeding the cohesive strength. For the case of OSG films, failures are not typically observed for higher modulus films.

4.2.1.3 Interfaces between low-κ polymers and underlying dielectrics

Spin-on organic ILDs commonly employ adhesion promoters prior to spin-coating the ILD in order to enhance adhesion to the underlying dielectric. In the absence of an adhesion promoter, adhesion of organic polymers to underlying oxide is poor and subject to thermally induced degradation [10, 106].

Adhesion promoters typically have a silanol end group to facilitate bonding to SiO_2 and either an amino- or vinyl-based functional end group to adhere to the polymer overlayer [3]. The formation of strong covalent bonds across the SiO_2/polymer interface results in improved adhesion strength. Polymer interfaces with vinyl-based adhesion promoters have been found to be stronger than with the amino-based adhesion promoter for the polymer benzocyclobutene (BCB). The superiority of the amino-based adhesion promoter may be due to more effective incorporation of the double bond of the vinyl group into the BCB polymer network. Adhesion promoters have also been incorporated into the bulk of the polymer [11].

For SiLK, an organosiloxane formulation is commonly used for the adhesion promoter. During a cure, the adhesion promoter bonds to both the SiLK polymer and underlying inorganic dielectrics, as long as the underlying layers have at least one monolayer of a strongly bound oxide [12]. During adhesion measurements of SiLK to underlying Si, SiO_2, Si_3N_4, TiN, and Al, no cohesive failures were observed; only adhesion failure at the interface with fracture toughness of 0.32–0.35 MPa $m^{1/2}$, measured using the m-ELT technique.

Even when an adhesion promoter is used, the adhesion of a polymer to the dielectric barrier can be compromised. Wet cleaning agents (e.g. HF) can diffuse through the low-κ material to attack the siloxane bonding of the adhesion promoter, thereby compromising the adhesion strength between the polymer and the underlying dielectric [13].

4.2.2 Interfaces between ILD and overlying dielectrics (e.g. antireflection coatings, hardmasks, capping layers, dielectric barriers)

Capping layers on ILD materials can assist patterning by functioning as antireflection coating (ARC) layers, hardmasks, and barriers to ILD damage from CMP and photoresist strip. When no cap is used (or if the cap is removed by CMP), then the dielectric barrier associated with the via ILD stack is deposited directly on top of the ILD, as shown in Fig. 4.2. The interface between low-κ materials and capping layers is commonly the interface most likely to delaminate during CMP, particularly for porous low-κ dielectrics.

When a dielectric barrier from the subsequent via stack covers the ILD layer, it is important to note that the dielectric barrier is simultaneously deposited over the underlying dielectric and Cu. As a result, any surface treatments employed must satisfy interface requirements of the dielectric barrier to both Cu and ILD, without inducing increases in ILD dielectric constant. The interface between Cu and dielectric barrier will be discussed further in Section 4.3.1.

As with the underlying dielectric barriers described in Section 4.2.1, dielectric capping layers are typically dense PECVD films, although spin-on etch stop and capping layers are being developed by chemical suppliers. Etch stop layers placed between the via and trench dielectric

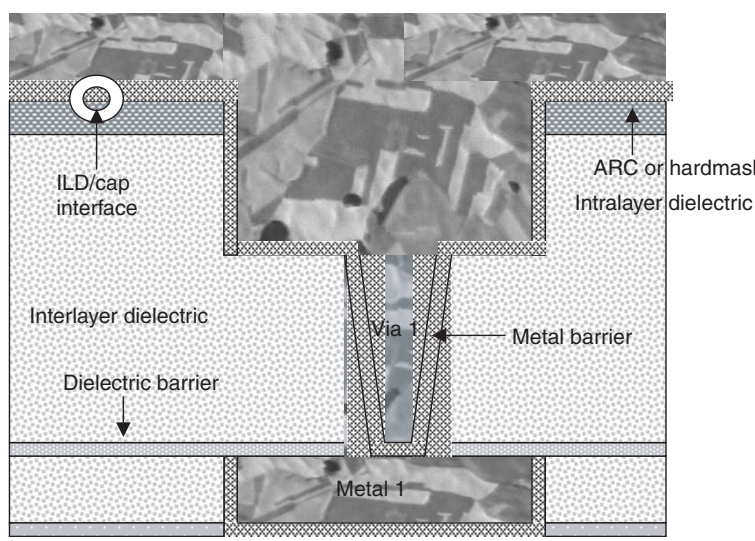

Fig. 4.2 Drawing of dual inlaid trench and via prior to CMP.

films are used to control the trench depth as a result of a significantly slower etch rate relative to the overlying trench ILD, as will be addressed in greater detail in Chapter 12. The plasma from the overlying layer deposition can result in a change in chemical, electrical, and mechanical properties of the underlying ILD.

4.2.2.1 Interfaces between silicon-based dielectrics and overlying dielectrics

The mobility of fluorine in FSG can lead to delamination of silicon nitride from FSG during thermal cycling [2]. The interface integrity of FSG films to subsequently deposited layers depends, in part, on moisture exposure prior to capping. FSG layers exposed to CMP and ambient moisture absorption prior to encapsulation are susceptible to fluorine migration to interfaces. Additionally, several authors have reported that the poor stability of the FSG/SiN interface is specific to FSG formed with SiH_4/SiF_4 precursors, while no analogous instability is observed for $TEOS/SiF_4$-based FSG films. The disparity has been attributed to the presence of more unbound and unstable fluorine in the FSG-based films [14, 15].

Martin *et al*. [16] reported that the FSG/SiN defectivity depends on (a) the time the wafer is exposed in the ambient environment, (b) the fluorine concentration in the FSG film, and (c) the FSG thickness, with thicker films more susceptible to delamination. They found that FSG can be stabilized by using an undoped cap, minimizing the time in ambient, or using dry N_2 storage.

Furasawa *et al*. [17] reported that unlike polymers and porous silicon-based low-κ materials, SiOC does not require a cap explicitly for CMP. They found that the presence of Si–C–Si bonds provides mechanical stability during CMP, and that oxide caps are required on the more fragile organosilicates with methyl-terminated Si–O–Si networks.

Even if caps are not required for OSG films to withstand CMP, they may still be used for patterning purposes (e.g. ARC, hardmasks). Peters [18] reported that SiC hardmasks have greater adhesion to SiOC than SiN caps. Wrschka *et al*. [19] suggested that a silane-based SiO_2 hardmask adheres weakly to SiOC, based on CMP erosion performance. Exposure of the SiOC-type low-κ materials to reactive plasmas during cap deposition may result in surface modifications, such as carbon removal and an increase in dielectric constant. Baklanov *et al*. [20] found that silica organic low-κ materials are stable in hydrogen plasmas, in contrast to organic low-κ materials that are attacked by hydrogen plasmas.

4.2.2.2 Interfaces of porous dielectrics and overlying dielectrics

Porous materials, in particular, require a capping layer to withstand chemical mechanical polishing (CMP). Porous polymer low-κ dielectrics also require a cap so that photoresist can be stripped without damaging the dielectric [21, 97]. Depending on the integration used, this cap may also be functioning as a hardmask and/or ARC layer.

For porous films, the plasma associated with cap layer deposition is expected to result in a thicker damaged region, as compared to dense ILD films. The ‘damage’ is manifested as

changes to chemical, electrical, and mechanical properties of the low-κ dielectric. Donaton *et al.* [22] found that oxidation of HSQ and silica from oxide cap deposition results in poor resistance to moisture absorption due to the formation of silanol.

Porous SiO_2 films are commonly post-treated to form a hydrophobic pore surface using hexamethyldisilazane (HMDS) or methyltriacetoxysilane (MTAS) [23]. This solvent exchange reaction will be discussed further in Chapter 5. In addition to reducing leakage current, the post-treatment results in a lower dielectric constant and improved stability with respect to moisture uptake [7]. Carbon loss in the porous SiO_2 during cap deposition depends, in part, on the temperature and thickness of the cap layer. Case *et al.* [23] found that a Si_3N_4 film deposited at 300 °C resulted in less carbon removal than a film deposited at 400 °C; however, the 300 °C film was a poor moisture barrier. Additionally, a 30-nm Si_3N_4 film resulted in less carbon loss than a 100-nm Si_3N_4 film.

The required thickness for a cap layer differs between porous and dense dielectrics. Iacopi *et al.* [24] found that a 30-nm layer of SiC is required to form a continuous cap to seal porous low-κ materials, as compared with thinner cap for non-porous low-κ films. For porous versions of SiLK, cohesive failures were obtained during adhesion testing of various capping layers (e.g. SiC, SiO_2, TaN) to porous SiLK [25].

Porous OSG films were shown to exhibit good CMP compatibility only with SiCN caps (corresponding to a fracture toughness of ~0.12 MPa $m^{1/2}$), while delamination was observed for SiO_2 and SiN caps [26]. The use of non-oxidizing plasmas in the cap deposition may be important for maintaining the chemical and mechanical properties of the OSG surface to supply adequate adhesion.

Spin-on etch stops and hardmasks are being developed by chemical suppliers. Such materials could eliminate the plasma damage issues associated with the PECVD materials, with potentially lower dielectric constants.

4.2.2.3 Interfaces between low-κ polymers and overlying dielectrics

The weakest adhesion in a low-κ polymer integration is typically found at the interface of the polymer and oxide cap [27]. An oxide cap layer can be completely delaminated from porous materials during CMP, even when low downforce is used [28]. The delamination may be associated with poor adhesion, surface contamination, or cohesive failure of low-κ film.

Adhesion between SiLK and hardmask has been enhanced by depositing a thin silicon-rich oxide prior to depositing a PECVD oxide hard mask [10]. The improved adhesion may be due to an increase in dangling bonds on the hardmask. Waeterloos *et al.* [8] measured the optimized adhesion strength of SiO_2 cap to SiLK to be ~ 0.3 MPa $m^{1/2}$ and of SiC to SiLK to be ~ 0.4 MPa $m^{1/2}$. They found that the gas stabilization steps for SiO_2 deposition were critical to optimizing adhesion to SiLK because if the surface of SiLK was oxidized prior to hardmask deposition, then poor adhesion and subsequent mechanical failures were observed during integration.

Long plasma exposure on polyimide can destroy molecular structure leading to worse cohesion within the upper regions of the film. Essentially, the adhesion failure occurs between bulk polyimide and damaged polyimide [29].

Spin-on and low-κ hard masks and etch stops are being developed. Waeterloos *et al.* [12] described the use of a spin-on material as etch stop/buried hardmask. Such spin-on layers eliminate all of the consequences of plasma damage associated with PECVD cap layers. A spin-on organo-siloxane film, used as a buried hardmask, does not require an adhesion promoter to the underlying inter-level dielectric, and the overlying intra-layer dielectric does not require an adhesion promoter when deposited on top of this buried spin-on hardmask. Few details have been published regarding the composition of these spin-on hardmasks and etch stop layers.

4.2.3 Interfaces between dielectrics and photoresist

Resist poisoning has been observed for many low-κ dielectrics and highlights the requirement for dielectric materials to be compatible with photoresist. Resist poisoning is the neutralization of the photogenerated acids in chemically amplified photoresist by amine-based by-products. As a result, resist dissolution is prevented during the development step in poisoned regions [18, 30]. The amine source may be the low-κ film directly. Porous materials without as-deposited nitrogen content may be an indirect source of amines when exposure to nitrogen-containing plasmas and subsequent reaction with hydrogen produces amines that diffuse into the low-κ film. The trapped amines can diffuse out from the film to react with exposed photoresist. A smaller pore size for a given porosity is preferred for minimizing poisoning effects [18, 30].

Hardmasks can effectively prevent direct contact between deep ultraviolet (DUV) resist and low-κ, but only on the top surface. For a via first, trench last (VFTL) integration, the key is to prevent resist and chemicals from penetrating via sidewalls in order to effectively pattern the trench layer without via poisoning [18]. Figure 4.3 shows the resist/dielectric interface prior to trench patterning in a VFTL integration.

Utilization of a trench first, via last (TFVL) dual hardmask integration eliminates poisoning problems by eliminating the possibility for resist to come in contact with the low-κ ILD [31]. This integration also facilitates patterning re-work without the possibility of damaging the low-κ. Via poisoning and various integrations will be addressed in further detail in Chapter 10.

4.3 Interfaces between dielectrics and conductors

4.3.1 Interfaces between copper and dielectric barriers

The interface between Cu and the dielectric barrier has been shown to be critical for both package reliability [32] and electromigration resistance [33]. Many reports have been published describing the native oxide formation on Cu and subsequent removal with thermal treatments

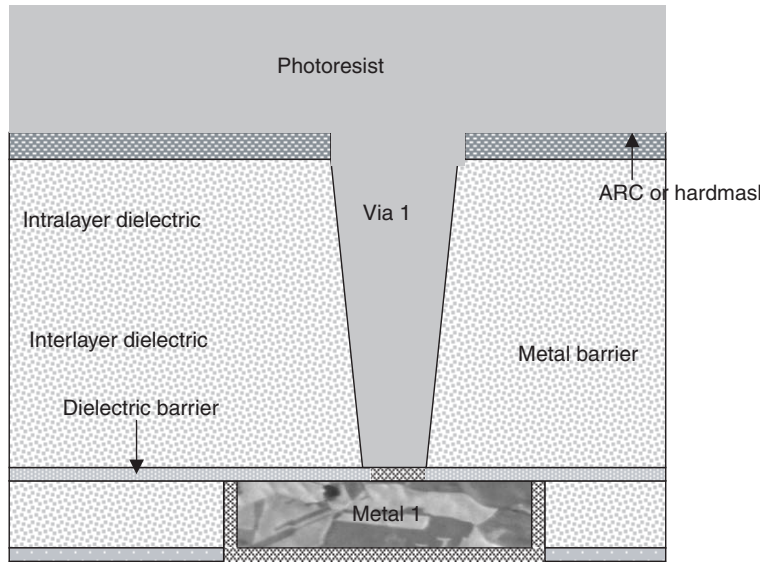

Fig. 4.3 Drawing of etched via prior to trench patterning for a VFTL integration.

and an assortment of plasma treatments. As noted in Section 4.2.2, all of these treatments must also be compatible with the underlying dielectric, in addition to the Cu.

4.3.1.1 Formation and removal of oxides and residuals on copper

Copper oxides readily form on a copper surface exposed to ambient air or deionized water [34]. Copper forms Cu_2O, CuO, $Cu(OH)_2$, $CuCO_3$, with Cu_2O as the dominant residue in a clean room ambient [20].

Many authors have reported methods to remove the native oxide, passivate the Cu surface by forming a copper hydride, and form a copper silicide to prevent Cu oxidation [35]. They showed that CO_2 and water will desorb thermally, and that a reducing plasma at temperatures $>300°C$ will reduce Cu oxide [20]. A metastable Cu hydride can form when hydrogen atoms are present in the gas phase. Hydrogen, ammonia, and N_2/H_2 plasmas have all been described for their ability to reduce copper oxide [20, 30, 36].

Decomposition of Cu hydroxide and Cu carbonate results in desorption of H_2O and CO_2 as shown in Eq. (1). The Cu surface is then mainly Cu_2O and CuO [20]. Copper oxide can then be reduced by hydrogen to yield pure Cu, as per Eq. (2).

$$CuCO_3 \rightarrow CuO + CO_2; \qquad Cu\,(OH)_2 \rightarrow CuO + H_2O_{(ads)} \tag{1}$$

$$CuO + 2H \rightarrow Cu + H_2O \tag{2}$$

Wet cleaning the copper with HNO_3 or HF provides some improvement, but is inadequate as these chemistries cannot remove adsorbed water or prevent re-adsorption of ambient species [35, 37].

In addition to native oxide, CMP residues also affects the integrity of the interface between copper and dielectric barriers. The use of corrosion inhibitors, such as benzotriazole (BTA), during CMP processing will impact the composition at the copper/dielectric barrier interface, and potentially impact the reliability of that interface. Further discussion of the contribution from CMP is included in Section 4.5.4.2.

A deleterious by-product of native oxide removal in the dielectric barrier deposition chamber is that desorbed oxygen-containing species from the Cu surface can accelerate decomposition of silane in the gas phase, resulting in a thin oxide deposition during silicon nitride deposition. A clean Cu surface can also suppress the catalytic decomposition of silane during the dielectric barrier deposition [35, 37].

4.3.1.2 Impact of copper alloys on interface with dielectric barriers

Alloying the copper has been another method employed to improve adhesion between copper and dielectric barriers. CuMg alloys improve adhesion with two mechanisms. (a) CuMg forms a self-passivating barrier that inhibits Cu oxidation and (b) upon anneal, Mg migrates to the surface and segregates along grain boundaries and is highly reactive with surface contaminants such as oxygen to form MgO [38].

The ability of Cu alloys to inhibit Cu oxidation was also studies by Li *et al*. [39]. They found Cu alloys formed with Ti, Pd, Cr, Al all to be effective in inhibiting copper oxidation.

4.3.1.3 Hillock formation on the copper surface

Given the temperatures of $>300°C$ associated with dielectric barrier deposition, when plasma pre-treatments are employed for Cu oxide reduction, the Cu microstructure is altered. The thermal cycling associated with deposition temperature plasma treatments can result in recrystallization of the copper, grain boundary grooving, and roughening, including copper hillock formation. Hillocks form to relieve compressive stress induced by thermal expansion mismatch [40]. Hillock formation and growth is confined to the time that copper is at temperatures above 300°C prior to the dielectric barrier deposition. Once the Cu has been encapsulated, hillock growth ceases.

With SiN Cu passivation layers, the density and size of the Cu hillocks grow rapidly as treatment conditions get more severe and treatment times are increased, and this poses a limitation on the treatment conditions that can practically be implemented [41]. The lower deposition temperature of SiCN (300–350°C) as compared to SiN (400°C), results in a reduction of Cu hillock density.

For an extreme case of hillock growth, adjacent lines can be shorted, causing device failure [40]. However, the more common impact of hillocks is the flooding of defect metrology scans with nuisance defects, which will be discussed in Section 4.6.4.

4.3.1.4 Impact of Cu/dielectric barrier interface on reliability

Removal of copper oxide has been found to improve both Cu/SiN- and Cu/SiC-based barrier adhesion. The impact of adhesion at the Cu/dielectric barrier interface on packaging reliability is presented in Section 4.6.1.2. Slotting is also presented as a contributor to reliability at this interface in Section 4.5.4.3. The impact of the chemical impurities at the Cu/dielectric barrier interface on electromigration resistance is discussed in Section 4.6.3.

As low-κ spin-on dielectric barriers are developed, a large challenge will be to identify a method to clean the copper surface so that the interface reliability is not compromised by the room temperature/solvent intensive processing of spin-coating.

4.3.2 Interfaces between ILD and metal barrier

The interface between ILD and metal barrier is amongst the most complex interface to study due to surface modifications incurred during integration. Degas and pre-cleans steps typically precede the metal barrier. When considering the interface between ILD and metal barrier, one must consider what, if any, damage has been incurred by the low-κ material during etch, ash, wet cleans, degas, sputter pre-cleans, and damage from the barrier deposition itself. Additionally, the amount of moisture absorbed, thermal cycling, and pattern density can be important components to the ILD/barrier interface properties, depending on the susceptibility of the ILD material used. Porous ILD layers provide an additional challenge related to the difficulty to deposit a continuous barrier along a porous sidewall [99, 102, 104].

Figure 4.4 shows an etched dual inlaid structure prior to barrier deposition, illustrating the potentially damaged surfaces of the low-κ dielectric.

Degas and plasma pre-clean steps, commonly used prior to barrier deposition, can improve barrier/ILD adhesion by chemically modifying the dielectric surface. When this method of surface modification is employed, it must not induce resputtering of the underlying Cu to the via sidewalls due to potential leakage.

The influence of various integration aspects (e.g. etch, resist strip, via clean, moisture, etc.) on this interface will be discussed in Section 4.5.4.

4.3.2.1 Interfaces between silicon-based dielectrics and conductive barriers

The most commonly used sputtered copper barriers, Ta and TaN, exhibit adequate adhesion to silicon dioxide. There is a temperature-dependent reduction of SiO_2 and Ta oxide formation that occur at the interface of Ta/SiO_2, thereby improving adhesion [42]. A bilayer of TaN/Ta has been proposed as the optimal barrier for SiO_2 since TaN has better adhesion to SiO_2 and Ta has better adhesion to Cu [5].

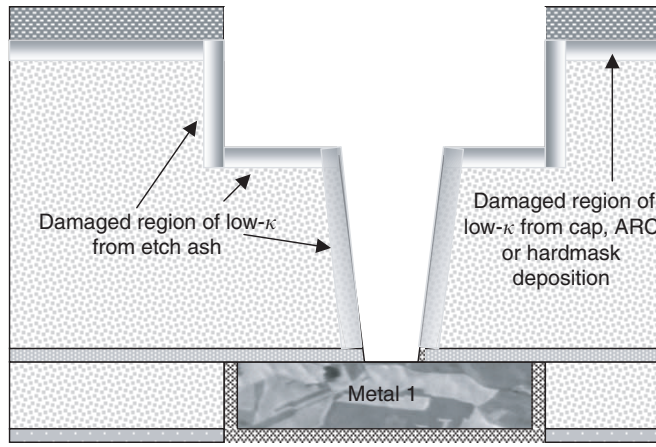

Fig. 4.4 Drawing of dual inlaid metal and via after etch and photoresist strip, showing regions where low-κ surface has been altered.

Several so-called 'barrier-less' integrations have been introduced with SiO_2. One such approach employs a Cu alloy to form a 'zero-width' barrier. For the Cu–Al alloy, Wang *et al*. [43] found that the Al segregates to the metal–oxide interface to promote an interfacial reaction at the alloy/SiO_2 interface. Although preliminary investigations of many of these barrier-less methods have focused on standard oxide ILD materials, they could be enabling approaches for delaying the imminent limitation on interconnect linewidth scaling and for addressing the inherent challenges of forming a continuous barrier on porous dielectrics.

The stability of fluorine-doped oxides depends on the fluorine content and bonding type. Even fluorine, which is well bound in the SiO_2 matrix as-deposited, can react with water to produce free fluorine [30] and react with Ta at elevated temperatures to form a readily delaminated TaF_x interface [44].

Reactive pre-cleans can be used to chemically modify the SiOF surface in order to either deplete F from the surface, or form an interfacial layer with Ta, which is resistant to TaF_x formation [45]. The use of a TaN/Ta bilayer was described by Edelstein *et al*. [5] as providing the adhesive benefits of TaN/FSG and Ta/Cu simultaneously. TaN is less reactive with free fluorine than Ta, and hence, exhibits greater stability of adhesion properties.

Adhesion of Ta-based barriers to SiOC materials has shown no adhesion degradation with moisture uptake or thermal cycling.

4.3.2.2 Interfaces between porous dielectrics and conductive barriers

The first challenge of barrier compatibility with porous dielectrics is the formation of a continuous layer that effectively blocks copper diffusion. Additionally, wet chemical and plasma via cleaning may cause more damage in a porous film due to increased diffusion length [30]. Porous films exhibit porosity dependent susceptibility to irreversible deformation and swelling.

Standard barrier thicknesses used on dense materials may be insufficient to prevent Cu diffusion into porous films [12, 25]. Iacopi *et al*. [46] found that the barrier thickness necessary to form a continuous seal on a porous dielectric depends on both pore size distribution and composition of porous material. They found that more than 30 nm of a PVD barrier is required when deposited directly on a porous material. However, if a 10-nm SiC spacer is first deposited, then 10 nm of PVD barrier provides a sufficient seal.

In addition to required barrier thickness, barrier composition, and thus, resistivity, has also been observed to change when deposited on a porous dielectric. Schulz *et al*. [7] found that the resistivity of sputtered TaN increases when deposited on porous oxide as compared to standard PECVD oxide. The increase is attributable to increased oxygen and carbon in the TaN, and Ta carbide and Ta oxide formation at the interface. The carbon source in the porous oxide is the methyl groups present due to the HMDS-based hydrophobization treatment the low-κ. The oxygen source is assumed to be weakly bound surface oxygen released from the porous oxide surface during the barrier sputter deposition. The authors found no carbon or oxygen reaction with TaN when a PECVD SiO_2 cap is used on the porous oxide. No nitrogen penetration into the porous oxide was detected for TaN capping. During adhesion testing of the barriers to the porous oxide, the porous films delaminated from underlying oxide.

The use of an oxide or carbide PECVD liner results in a reduction in required barrier thickness, and elimination of chemical reactions between the porous low-κ and the barrier. This could prove to be an important method for addressing some of the integration challenges associated with porous dielectrics, if the liner can be thin enough to minimize capacitance impact.

4.3.2.3 Interfaces between low-κ polymers and conductive barriers

Polymers have different bonding properties to metallic barriers as compared to silicon-based dielectrics. Additionally, the impact of integration damage at the polymer surface differs from Si-based materials. Spin-on organic films are very resistant to most wet clean chemistries, but bowing of the via profile has been observed for plasma-based via cleaning of organic ILD films [18].

The interface bonding between metals and polymers is determined by the unfilled d-orbitals of the metal, according to Chang *et al*. [47]. As such, it is expected that refractory metals such as Ti or TiN have a higher bonding energy than metals such as Cu, which have few or no unfilled d-orbitals available for bonding interactions. It is predicted that the bonding mechanisms for Ti(N), Ta(N), and WxN will all be similar.

Scherban *et al*. [48] observed that spin-on polymer dielectrics generally adhere better to barrier films than carbon-doped oxides and that PVD barriers generally adhere better than CVD barrier to low-κ dielectrics. They also found that barrier pre-treatments can significantly modulate adhesion of CVD barriers to polymers. The adhesion of CVD TiNSi to a spin-on polymer is greatest when no pre-clean is used, with severe degradation in adhesion observed

when an Ar pre-clean is used. The aggressive ion bombardment associated with Ar sputter pre-cleans may damage the cross-link structure of the polymer.

As with the fluorine-doped oxides, reactive pre-cleans can also be used to modify the polymer surface to enhance bonding to metal barriers. Treating the polymer surface with O_2 and N_2 plasmas results in improved adhesion by creating new functional groups on the surface [49]. The breakage of C–C or C–H bonding on a polymer surface and formation of the functional groups, C–N, C=N, C=O–N by a nitrogen plasma and C=O in oxygen plasmas facilitate strong bonding between the barrier and the modified polymer surface. Adhesion is stronger to the N_2- plasma-treated polymer due to Ti–N bonding as compared to Ti–O bonding at the surface of the O_2-plasma-treated polymer.

In addition to surface modification, plasma pre-cleans can also be used to remove etch residues. Hydrogen plasmas remove carbon and fluorine containing residues from the plasma etching of polymers [20]. However, if the hydrogen-based reactive pre-clean is applied at high temperatures following wafer degas, the polymer may be attacked and sidewalls recessed.

4.3.3 Interfaces between metal barrier and hardmask or CMP cap

Figure 4.2 shows that when a capping layer is used for a given integration and is not completely removed during etch/ash, then an interface will be formed between the capping layer and the subsequently deposited metal barrier. As with the ILD/photoresist interface, the interface between the metal barrier and dielectric capping layers is present during fabrication, but is not present in the final device, as the conductive barrier must be removed from the hardmask surface during CMP in order to avoid leakage between electrically isolated metal lines.

Little has been published about adhesion to this interface, using either conventional PECVD capping layers or the spin-on capping layers currently being developed. Given the temporary nature of this interface, it need not withstand repeated thermal cycling or package reliability. In terms of mechanical reliability, this interface must only withstand CMP.

4.4 Interfaces between dielectrics and semiconductors

In CMOS transistor or 'front-end' processing, two critical dielectric/semiconductor interfaces are the oxide/Si interface in shallow trench isolation (STI) structures and the gate dielectric/Si interface. In both cases, the physical and chemical properties of the interface can have a significant impact upon electrical performance and/or reliability of the device.

For isolation trench filling, SiO_2 is the dielectric fill material commonly used, and is deposited through various techniques, including thermal low-pressure chemical vapor deposition (LPCVD), atmospheric and sub-atmospheric CVD (APCVD, SACVD), conventional plasma-enhanced CVD (PECVD), or high-density plasma (HDP) CVD. The dielectric/Si interface can

be affected by thermal cycles prevalent in front-end processing, and the quality of the interface affects electrical isolation effectiveness.

As CMOS technology scaling has continued to follow Moore's law, one of the by-products has been continued aggressive scaling of the gate dielectric thickness for improved device speed and performance. However, as the gate oxide continues to be thinned, gate leakage current due to direct tunneling becomes an ever-increasing component of the overall gate leakage. For example, for SiO_2 gate dielectric below 3.5 nm, every 0.4–0.5 nm reduction in oxide thickness results in a gate leakage current increase of 100×. This has driven an evolution from pure SiO_2 being used as the gate dielectric to nitrided-oxides, and soon to higher dielectric constant (higher κ) materials such as metal oxides and silicates, which are discussed in detail in Chapter 8. The selection and integration of these new high-κ gate dielectrics are largely impacted and limited by the interfacial properties of these materials with Si.

4.4.1 Shallow trench isolation fill dielectric/semiconductor interfaces

While shallow trench isolation (STI) has proven capable of improved isolation performance and scalability compared to traditional local oxidation of silicon (LOCOS) isolation, the combination of etch, fill, and chemical–mechanical polishing adds complexity to the process. For successful integration of an STI approach, careful consideration must be given to understanding the interfaces between the dielectric fill material and the surrounding Si.

Since the trench etch introduces crystallographic damage into the Si, post-etch treatments such as sidewall oxidation, or trench liner oxidation, are used to eliminate trap-assisted junction leakage. In addition, the trench liner oxidation removes plasma damage from the trench etch and provides proper edge rounding of the active corners [50–55].

As described by Chatterjee *et al.* [56] deposited oxides used for STI trench fill such as LPCVD TEOS, SACVD O3-TEOS, and spin-on glass such as hydrogen silsesquioxane (HSQ) generally etch much faster than the thermally grown side-wall liner oxides. During subsequent pre-gate HF cleans, this can result in field oxide loss and possible exposure of trench corners directly to poly-gates. Densification anneals (typically above 800°C) in oxidizing ambients can serve to match trench fill and trench liner oxide etch rates, but also induce stresses that increase diode leakage [57]. Furthermore, densification in H_2O produces the Kooi effect, in which gate oxide thinning occurs near transistor edges, causing significant degradation in gate oxide integrity. Therefore, a trench fill densification step in an inert ambient is typically used to better match etch rates between LPCVD- and SACVD-deposited and grown oxides [58]. This densification step may not be required in HDP-CVD trench fill oxides. Figure 4.5 shows an example of trenches filled with HDP-CVD oxide where there is no delineation between fill and liner oxides.

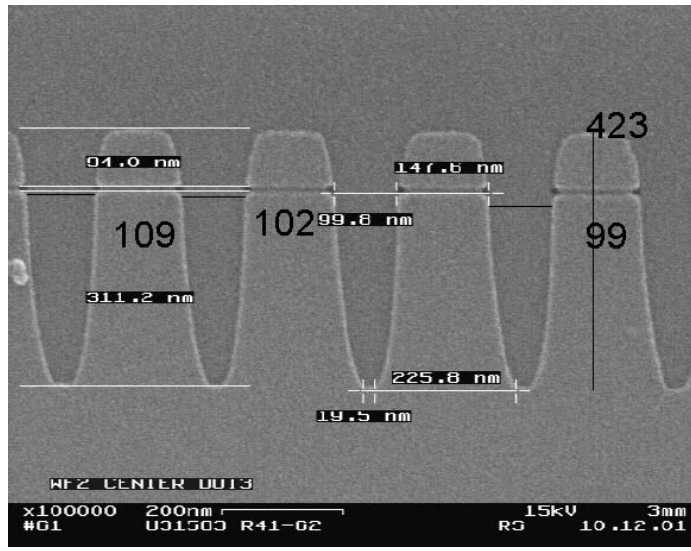

Fig. 4.5 STI structures using high-density plasma CVD oxide fill showing no delineation between trench oxide liner and fill.

4.4.2 Gate dielectric/semiconductor interfaces

There are four primary causes of non-ideal MOS behavior in an SiO_2/Si system: fixed oxide charge (Q_f), oxide trapped charge (Q_{ot}), mobil charge (Q_m), and interface-trapped charge (Q_{it}). Fixed oxide charges are located in the SiO_2 layer very near to the SiO_2/Si interface, and result from dangling bonds off excess Si atoms in SiO_2. Fixed oxide charges cause flatband and threshold voltage shifts, which can be reduced by high-temperature post-oxidation thermal annealing. Oxide-trapped charges are believed to be due to H and OH bonds trapped in the oxide, and lead to oxide breakdown and threshold voltage instability. Trapped oxide charges in SiO_2 can be reduced by the incorporation of nitrogen into the oxide either during or after the oxidation process. Mobile charges are generally due to ionic contaminants such as sodium or potassium in the SiO_2, and cause flatband voltage instabilities. Exposure to a chlorine-containing chemistry can reduce the mobile charge. As its name suggests, the interface-trapped charge is the only one of the four that is present directly at the SiO_2/Si interface, and is the result of process- or radiation-induced structural defects from dangling Si bonds or impurities at the interface. Interface-trapped charges degrade the transconductance and sub-threshold swing of CMOS devices. In the SiO_2/Si system, the effects of interface-trapped charges can be reduced by terminating dangling bonds via hydrogen-containing anneals [59].

To minimize the generation of interfacial defects prior to thermal oxidation of Si or deposition of a high-κ gate dielectric, the wafer surface should be as pristine as possible, and free from particles, organic contamination (e.g. resists, oils), inorganic contamination (e.g. metals), native oxide, and surface roughness [60]. For several decades now, the industry has utilized cleans based on the original RCA cleaning process developed by Kern and Poutiner [61]. The 'standard clean-1' (SC-1) consists of an NH_4OH:H_2O_2:H_2O solution, and removes particles by either dissolution, oxidation and dissolution, lift-off, or electrical repulsion between the wafer surface and the particles. The 'standard clean-2' (SC-2) consists of an HCl:H_2O_2:H_2O solution that is effective in removing metallic contaminants by forming soluble complexes.

Native oxide on the Si substrate prior to gate dielectric growth or deposition is undesirable as it tends to be non-stoichiometric and may contain impurities. HF-last or modified HF-last cleans containing isopropyl alcohol or H_2O_2 are effective at removing native oxide and leaving a hydrogen-terminated surface prior to gate dielectric formation.

Surface roughness at the gate dielectric/silicon interface can cause multiple performance and reliability issues, including degradation of channel mobility, drive current, oxide breakdown field, and charge-to-breakdown. For the 100-nm technology node, it is estimated that the surface roughness can be no greater than 0.1 nm, and for the 70-nm node, the roughness should be less than 0.08 nm. Roughness can be caused by NH_4OH, or etch component, of the SC-1 clean. The effect can be reduced by adjusting either composition of the etchant, the temperature of the cleaning bath, or the overall cleaning time, but these factors must be balanced against the cleaning efficiency of the process. More recently, Heyns *et al.* [62] have developed a clean that effectively separates the oxidizing and etching components of the cleaning process to provide a self-limiting chemical oxide growth followed by an HF-based oxide removal and drying step that maintains improved surface smoothness compared to the traditional RCA clean.

To date, CMOS technology has thrived largely due to the relative ease of formation of a high-quality oxide on Si. Continued scaling of the SiO_2 gate oxide thickness results in higher drive currents and operating speeds while reducing short channel effects. However, conventional oxide scaling will ultimately be limited by factors such as direct tunneling and stress-induced leakage currents, inability to block diffusion of dopant and impurity atoms, and high interface state generation under electrical and radiation stresses. Oxynitrides allow for some extendibility in thickness scaling by offering lower interface state generation, stress-induced leakage currents, and trapped charges, while improving resistance to dopant diffusion. For the projected gate leakage requirements for future low-power and high-performance devices, however, a change to higher-κ gate dielectrics will be required. Since the physical thickness of a high-κ gate dielectric compared to its equivalent oxide thickness (EOT) in SiO_2 is directly proportional to their dielectric constant ratios, high-κ dielectrics provide longer physical tunneling distances compared to SiO_2 for the same EOT. This will allow for further gate dielectric scaling without exceeding gate leakage requirements. With the shift towards deposited high-κ gate dielectrics, engineering the interface or interfaces between gate dielectric and Si are significantly more complex.

Some of the early high-κ gate dielectric work with TiO_2, Ta_2O_5, and barium strontium titanate (BST) showed that because these materials were thermally unstable with the Si substrate, an additional barrier layer would be required to prevent interfacial reactions. Specifically, in the cases of TiO_2 and Ta_2O_5, which had been previously used as capacitor dielectrics in memory devices, oxygen vacancies were typically present in as-deposited films, which prompted the need for post-deposition oxygen anneals to improve the gate dielectric quality. As a result of those anneals, the bottom and top surfaces of the high-κ gate dielectric became oxidized, leading to an undesired increase in the electrical oxide thickness that negated much of the benefit of going to a high-κ dielectric [63–66].

ZrO_2 and HfO_2 are considered two promising high-κ gate dielectric candidates since they are thought to be thermodynamically stable in contact with Si. In their pure oxide forms, both have shown that a significant interfacial SiO_2 layer forms between the high-κ material and the Si substrate after post-deposition anneals, and that carrier mobilities are ultimately degraded [67, 68] (Tseng *et al*., to be published). Figure 4.6 show a cross-sectional TEM of a gatestack with HfO_2 gate dielectric, which clearly shows significant interfacial layer growth after post-deposition anneal.

Zr- and Hf-based silicates have also been examined with respect to their interfaces with Si. Wilk and coworkers [69, 70] have observed that $ZrSi_xO_y$ films annealed at 800°C for 30 min in nitrogen show no appreciable interfacial oxide layer formed between the gate dielectric and the Si substrate, and that carrier mobility is also higher than that for pure ZrO_2.

For high-κ gate dielectric materials, the challenges for integration are clearly not just in achieving the desired bulk dielectric film properties. Engineering the interfaces between the gate dielectric and the Si substrate as well as possibly between the gate dielectric and the gate

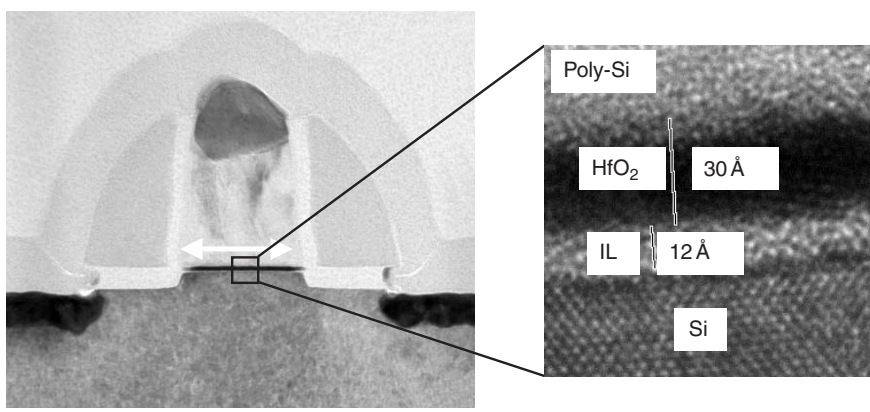

Fig. 4.6 Cross-sectional TEM of gatestack with HfO_2 gate dielectric showing significant interfacial layer resulting from post-deposition anneal.

electrode (whether it be polysilicon or a metal gate) are issues critical to the success of high-κ gate dielectric integration that were not present in the SiO_2/Si system.

4.5 How to look for interactions

A variety of analytical techniques have been used to characterize dielectric interfaces. Techniques to measure the chemical and mechanical properties of interfaces have advanced to accommodate the requirements associated with scaling of device geometries and low-κ moduli. Advancements in compositional analysis, adhesion measurements, and atomic scale imaging are critical components to understanding and optimizing the abundant interfaces that dominate the performance and reliability of the most advanced semiconductor devices. This section will discuss the applicability of various analytical techniques to interface characterization. Some of these techniques will be described in greater detail in Chapter 12.

4.5.1 Interface composition analysis

Common tools for determining interface composition include X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), and time-of-flight secondary ion mass spectrometry (ToF-SIMS). Each of these techniques provides surface and depth profile compositional information, and require standards to determine sensitivity factors for converting signal intensity or peak area into atomic concentration.

Roughness at an interface will result in a compromised depth resolution and depending on the ratio of surface roughness to interface thickness, may make it difficult or impossible to definitively distinguish the composition at the interface from the composition of the surrounding bulk films. Analysis of a buried interface using XPS, AES, or ToF-SIMS requires sputtering a crater through the subsequently formed films. This sputtering adds roughness to the crater and thereby adds another source of compromised depth resolution at the interface.

XPS has been widely used to detect reactions across interfaces by the measured shifts in binding energy that occurs when an element in the bulk reacts to form new compounds at the interface. Evaluation of copper oxide reduction [20, 36] and dielectric surface modifications by plasmas [29, 49] have employed XPS to detect such binding energy shifts.

ToF-SIMS has greater sensitivity to trace levels than XPS or AES. This technique has been used to show diffusion across interfaces, as well as reactions at the interface. XPS, AES, and ToF-SIMS have all been used to determine the locus of failure following adhesion testing.

Rutherford backscattering (RBS) can provide depth profile information without artifacts associated with sputtering used in AES, XPS, and ToF-SIMS depth profiles. However, RBS is not sensitive to light elements, and due to depth resolution limitations, is most appropriate for detecting the creation of broad ($>$200-Å thick) interfacial layers. Similar to AES, XPS, and ToF-SIMS, interface roughness cannot be distinguished from interface diffusion.

4.5.2 Interface imaging analysis

Standard imaging techniques such as scanning electron microscopy (SEM), transmission electron microscopy (TEM), and focused ion beam (FIB) methods require limitations for sample preparation and beam conditions on some low-κ materials in order to prevent damage to low-κ materials. Etched profiles may appear distorted if the low-κ films incur shrinkage during sample preparation and imaging. Interface imaging necessarily requires very high magnifications ($>100\,000\times$) to reveal subtle interactions.

Novel techniques are emerging for imaging low-κ materials due to both the beam-damage artifacts of conventional imaging techniques and the need to identify methods to reveal interface-specific issues. Focus on new techniques is expected to grow to satisfy failure analysis and in-line metrology needs to evaluate emerging materials and complicated interfaces with ever-increasing resolution requirements.

4.5.2.1 Scanning electron miscroscopy for interface imaging

While SEM is effective in showing interface effects of >200 Å, resolution limitations prevent the use of SEM to detect monolayer-type reactions at the interface. Beam damage of low-κ materials is a concern with SEM. An indirect benefit of this damage is that the beam damage affects the bulk of the low-κ material differently from regions of the dielectric modified by other process steps (e.g. etch, resist strip). As such, SEM is an effective tool to show if a low-κ material has been altered by etch/ash along a sidewall.

4.5.2.2 Transmission electron microscopy for interface imaging

Imaging with TEM has been a particularly enabling method for interface analysis. While techniques such as atomic force microscopy AFM can be used to measure roughness on a surface, TEM is amongst the best methods to obtain high-resolution evaluation of interface roughness. However, the sampling size is very small ($<10\,\mu$m) and may not be representative of the entire wafer.

Gate dielectric thickness measurement is one of the most critical applications for TEM, with no viable alternative for a calibrated physical measurement. TEM has also been used to show Cu diffusion through barriers, and penetration through ILD layers. Complex interfaces can be characterized to show multilayers [71] when other techniques may yield more ambiguous results due to spatial resolution limits.

4.5.2.3 Nanoscale elastic imaging and electric force microscopy for interface imaging

Shekhawat *et al*. [72, 73] have introduced a technique, nanoscale elastic imaging, in which an ultrasonic force microscope (UFM) is configured from an atomic force microscope (AFM).

The output of the nanoscale elastic imaging is a map of mechanical rigidity across the sample with a spatial resolution of ≤ 10 nm. This technique has been used to scan inlaid metals after polishing to reveal an increase in elastic modulus of a polymer along the sidewall of the metal trench.

Gross *et al*. [74] described the use of electric force microscopy (EFM). A variant of scanning probe microscopy (SPM), the EFM technique provides a map of dielectric constant. With a spatial resolution of 50 nm, this technique can be used to detect local variations in dielectric constant, such as at low-κ surfaces adjacent to etched trenches.

4.5.3 Adhesion measurement techniques

Adhesion is a complex quantity that is affected by numerous factors. It is the sum of all interatomic interactions at the interface. Adhesion can be considered as the work required to completely separate two films along the common interface. Experimentally measured adhesion (i.e. practical adhesion) depends on fundamental adhesion in addition to external contributors (e.g. intrinsic stress, defectivity, grain size, etc.) and is a function of the technique used [27].

Delamination starts at a flaw. Particle contamination, minute delamination due to surface cleanliness, or a stress singularity associated with the integration architecture can all function as flaws [1].

Today, there are over 300 methods for measuring practical adhesion [75]; each technique exploiting different properties of the measured materials, and each having its own set of benefits, artifacts, and drawbacks. In this section, several adhesion measurement techniques most commonly used for assessing dielectric interfaces are described and compared. Most quantitative measurements for measuring adhesion require unpatterned wafers or large unpatterned regions on patterned wafers. Identifying the locus of failure is a critical component to all adhesion testing techniques. The previously described surface analysis techniques can be used for this purpose. The correlation of adhesion performance of unpatterned test structures to that of functioning devices will be addressed in Sections 4.5.4 and 4.5.5.

4.5.3.1 Tape pull methods

4.5.3.1.1 Scotch tape test

The use of tape tests for adhesion dates back to 1935. It is a qualitative method to measure adhesion with the outcome being (a) film completely removed from the substrate, (b) film not removed at all, (c) film is partly removed or removed in localized patches. The great advantage of this method is the ease of measurement, and has been shown as a useful tool for quickly screening interfaces for poor adhesion. An interface that fails the scotch tape test is unlikely to endure the stresses involved in CMP.

4.5.3.1.2 Quantitative peel test

Quantitative peel tests involve peeling a thin film off the substrate by applying a backing material to the film and holding onto the backing material while peeling the film. Peeling is performed with a fixed lift angle, rate, and film width. The load required to remove the film is measured during the peeling, with results expressed as force per length (e.g. N/cm). Crack initiation is the difficult part, requiring either a release layer deposited as part of the stack, or scratching the film prior to peel.

4.5.3.2 Stud pull tests

Stud pull tests employ a nail-shaped stud bonded to a surface and subsequently pulled from the surface under controlled conditions [76]. This test produces a large scatter in measured pull strength due to a broad range of impurities or defects along the interface at which crack growth starts, and thus requires multiple tests for each sample. For very strong interface adhesion, the epoxy, used to adhere the stud to the sample, is expected to fail first. The pull strength is measured in MPa, and standard deviation is also reported.

4.5.3.3 Scratch tests

The scratch test consists of scratching the surface thereby deforming the coating–substrate interface, with either an increasing or constant load. The critical load can be determined by acoustic emission or by the sudden variation of the normal, tangential, or lateral force applied to the sample [77]. The mechanical resistance of the interface is characterized by the critical load, which is defined as the minimum load at which coating damage can be observed.

During testing, the shear stress is transmitted elastically through the coating, across the interface, and into the substrate that undergoes elastic–plastic deformation [78]. The correlation between measured critical load and the actual adhesion strength is not well understood due to the many contributors to the shear stress distribution in the sample from the test itself.

4.5.3.4 Four-point bend

The four-point bending test involves preparing samples in strips, glued together with epoxy. A pre-crack notch is created in the top Si strip to produce a localized high-stress region where delamination initiation is desired. Instruments record applied load and displacement of the pins [103]. Strain energy release rate G_c depends on silicon elastic modulus, Poisson's ratio, strip geometry, and apparatus geometry. P is the load that generates a stable crack growth at the weakest interface of the stack [44]. The advantages of the four-point bend method are that it is reproducible and provides a quantitative measure of interface adhesion energy [48].

Bending beam methods can also be used to measure fatigue, which is the debond growth rate as a function of applied strain energy release rate under static and cyclic loading

conditions [3]. Fatigue loading can accelerate debond growth rates and decrease thresholds for subcritical debonding relative to static loading conditions.

4.5.3.5 Nanoindentation

Nanoindentation has been used to measure a variety of mechanical properties. It has been used for adhesion measurements where the mechanical energy release rate, or practical work of adhesion, is calculated based on the delamination size. Adhesion strength (i.e. fracture toughness) is derived from the continuous load–displacement profile and an independently measured geometrical scale parameter, which results from the crack length or delamination radius from the indentation [79, 107].

4.5.3.6 Modified edge liftoff (m-ELT)

The m-ELT test uses a deposited film on a rigid substrate (e.g. silicon) with a thick backing layer (e.g. epoxy). The backing layer has a known stress–temperature profile and higher fracture toughness than the test material, and must have excellent adhesion to the deposited material. The wafer is diced and cooled until debonding occurs. The residual stress and fracture toughness are calculated based on the temperature at which debonding occurred [80].

4.5.3.7 Comparison of adhesion techniques

Table 4.1 includes a comparison of different techniques for adhesion testing. Sample preparation, measured quantity, and technique-specific limitations are included.

4.5.4 Correlating interfacial properties of unpatterned wafers to complex device architecture

As mentioned in the previous section, current quantitative adhesion measurement techniques require unpatterned stacks. As such, it is common to deposit unpatterned test structures to measure adhesion in order to predict the interface integrity on the actual device. Measurements on unpatterned substrates can range from overly favorable or overly unfavorable relative to reliability on functional devices, depending on which, if any, integration-related surface modifications such as etch, resist strip, CMP, cleans, moisture absorption, and pattern density are considered. Finite element modeling (FEM) and fracture mechanics can also be utilized to predict interface reliability for patterned structures when only mechanical properties of unpatterned stacks are known.

4.5.4.1 Role of etch, resist strip, and clean damage in altering sidewall ILD properties

The combination of etching and resist stripping can leave residues and can additionally cause changes in composition, rigidity, dielectric constant, and stability of low-κ dielectrics on

Table 4.1 Comparison of various adhesion measurement techniques

Technique	What is measured	Sample preparation and testing complexity	Quantitative or qualitative	Limitations
Scotch tape test	Pass/fail	No sample prep.	Qualitative: comparative use only	Appropriate for 'poor' adhesion only
Stud pull	Pull force (MPa)	Attach studs with epoxy	Quantitative for adhesion weaker than epoxy, large sigma	Cohesive strength of epoxy defines measurable upper limit
Scratch test	Critical load	No sample prep.	Quantitative	Many test artifacts contribute to critical load
Four-point bend	Strain energy release rate G_c (J/m^2)	Dice strips, join with epoxy	Quantitative for adhesion weaker than epoxy	Cohesive strength of epoxy defines measurable upper limit
Nanoindentation	Fracture toughness	Deposit superlayer	Quantitative	Artifacts related to superlayer contribute to fracture toughness
m-ELT	Fracture toughness K_{1C} MPam$^{1/2}$)	Apply epoxy, controlled cooling, Inspection for delamination	Quantitative	Crack path shape can vary

patterned surfaces. The modifications to the low-κ dielectric surface, as shown in Fig. 4.4, clearly impact the low-κ/barrier interface reliability, and can furthermore, impact chip performance.

Many investigations of the adhesion of barriers to low-κ dielectrics neglect the altering effects of the etch, resist strip, and clean steps. The following sections address how the etch, resist strip, and clean affects Si-based, porous, and polymeric materials, and the subsequent impact of those surface modifications on the barrier interface.

4.5.4.1.1 Impact of etch, resist strip, and clean on silicon-based dielectrics

As described in Section 4.2.2.1, OSG materials have been found to be susceptible to oxidation from exposure to oxygen plasmas and basic aqueous solutions [13]. With aggressive chemistries, carbon of the low-κ is consumed, and polar groups such as silanol (Si–OH) are formed. Less aggressive plasma conditions may transform the surface of an OSG film into a dense SiO_2 layer with few polar groups.

Severe shrinkage and bowing with a 250-nm damaged region was seen for SiOC trenches when using a high-temperature/high-pressure O_2 plasma for photoresist strip [6]. The bowing and undercut was reduced when using a low-temperature/low-pressure N_2/O_2 strip process instead.

4.5.4.1.2 Impact of etch, resist strip, and clean on porous dielectrics

It is expected that etch, resist strip, and wet cleans can each cause severe modifications of etch profiles and porous film compositions by either rapid diffusion of plasma species and wet chemicals through the porous microstructure, or by reaction with the low-κ material.

Etch and ash damage can be manifested as a change in dielectric constant. For a porous OSG film, Lin *et al*. [81] measured a dielectric constant of ~2.7 following a reducing NH_3 ash versus a dielectric constant of 2.2 for an oxidizing N_2/O_2 ash. Iacopi *et al*. [24] found no harmful impact when using a water-based strip process for post-etch cleaning of XLK. The authors suggested that the rinse–dry and degas processes are critical determinants of the impact of wet treatments.

The use of oxygen in the OSG etch causes severe bowing of the trench profile and an increase of dielectric constant to >4, compared to etching with a reducing chemistry [31, 97]. Very few clean chemicals have been identified as compatible with porous OSG films.

4.5.4.1.3 Impact of etch, resist strip, and clean on low-κ polymers

Etching of polymers such as SiLK have not shown the severe surface modifications described for OSG films. However, polymers have shown varying reactivity to solvents and clean chemistries.

For integration of SiLK with a hardmask, photoresist strip occurs concurrently with etching due to the similarities in composition between photoresist and SiLK [82]. However, a chemical treatment (e.g. hydroxylamine based) may still be required to remove residual resist and polymers. Nomura *et al*. [82] suggest that thermosetting polymers, such as SiLK, are less vulnerable to attack by plasma and chemicals as compared to thermoplastic polymers that have no cross-linking structure and exhibit low resistance against polar solvents. Passemard *et al*. [13] found that when polymers absorb solvents, they do not readily react, and the absorbed solvents can be readily removed by drying at 150°C in N_2.

Passemard *et al*. [13] found that an ozone treatment will form a ketone group on the polymer surface, sulfuric acid will transform ether groups (R–O–R′) into polar termination

(R–OH). As reported in Section 4.2.1.3, the authors also found that HF can penetrate an organic polymer and attack the siloxane bonding of the adhesion promoter, resulting in delamination from the underlying substrate. Additionally, hydroxylamine clean chemistries were found to interact with Cu and subsequently delaminate with SiLK.

4.5.4.2 Effect of CMP chemistries on interface properties

As mentioned in Section 4.2.1, impurities at the interface between Cu and dielectric barrier impact both adhesion and electromigration resistance. Although most studies have focussed on growth and removal of native oxide, residuals from CMP may be of equal or greater importance for interface reliability.

Hymes *et al*. [35] described the use of benzotriazole (BTA) in the final stages of CMP in order to passivate the Cu against oxidation. Although adsorbed BTA can be removed by thermal cycling, remaining residuals will alter the Cu/dielectric barrier interface, and potentially impact the nucleation of the PECVD-based dielectric barriers. As with etch damage, the CMP steps are frequently absent in published studies of Cu surface effects and subsequent interface reliability.

4.5.4.3 Effect of pattern density, slotting, and tiling in adhesion

Tiling and slotting is another important predictor of interface reliability that is frequently omitted from interface studies. Delamination of low-κ dielectrics during CMP is pattern dependent, with peeling most prevalent in open field areas [71]. Likewise, CMP of blanket stacks show failure when no failures are observed on patterned stacks [28]. For a given range of elastic moduli, CMP tests on unpatterned stacks will delaminate, when the same stacks integrated in patterned structures do not delaminate [26]. Goldblatt *et al*. [21] described the use of a 'sea of vias' beneath bonding pads to effectively provide a local increase in pattern density to improve packaging reliability when SiLK is used as the low-κ dielectric.

In addition to the benefits of metal islands in a field of dielectric (i.e. tiling), the presence of dielectric islands in a field of metal (i.e. slotting) can also beneficial. Figure 4.7 shows delamination of a probe pad with no slotting at the Ta/FSG interface. This same interface subjected to the same moisture and thermal cycling shows no delamination on slotted probe pads. Slotting can also benefit reliability of the Cu/dielectric barrier interface.

Benefits of slotting or tiling depend on which interface is weakest. If the weakest interface is between dielectric layers (e.g. interface between low-κ dielectric and cap), then tiling will decrease the surface area of that weak interface thereby improving reliability. However, slotting would increase the surface area of the weak interface and subsequently decrease reliability. If the weakest interface includes a metal interface (e.g. interface between metal barrier and low-κ), then slotting will improve overall reliability and tiling will compromise the interface integrity.

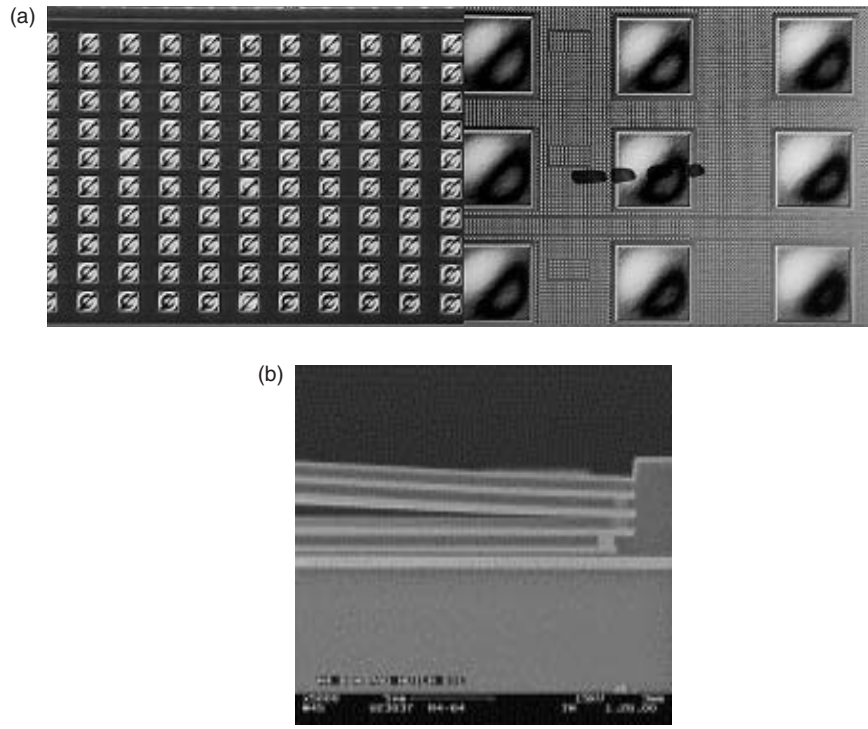

Fig. 4.7(a) Top-down image of delamination in unslotted probe pads. (b) SEM cross-sectional image of delamination at the Ta/FSG interface in an unslotted probe pad.

These results are not surprising given the higher intrinsic stress for a blanket sheet as compared to small segments of material. As such, assuming all interface damage and moisture absorption are the same for unpatterned and patterned structures test structures, adhesion measurements and CMP performance are expected to be worse for the unpatterned test structures. This adhesion behavior of unpatterned versus patterned structures can also be explained by modeling work showing an increase in crack driving force with increasing crack length, as shown in Fig. 4.8 [83]. The presence of slots or tiles effectively limits the maximum crack length thereby minimizing the crack driving force.

The natural outcome of this difference between patterned and unpatterned substrates is to define a minimum pattern density and tiling/slotting algorithm to minimize susceptibility to delamination. As will be described in Section 4.5.5, modeling can be used to predict pattern density effects on interface delamination.

4.5.4.4 Impact of moisture and thermal cycling on interface properties

Moisture absorption can turn a strong interface weak and convert a low-κ material into a not-so-low-κ material. Heat resistance is necessary to prevent degradation during the interconnect

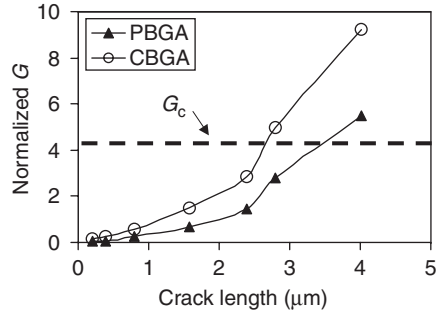

Fig. 4.8 Crack driving force versus crack length at the low-κ/passivation interface.

fabrication process (e.g. Cu anneal, low-κ curing, etc.). Moisture resistance is necessary for long-term reliability after packaging. The degree to which interfaces are impacted by moisture absorption differs amongst dielectrics, depending on composition and porosity. Spin-on dielectrics are typically stable with thermal cycling, as they are cured at high temperatures. However, porous films can readily absorb moisture. Fluorinated materials have shown the most dramatic changes with moisture.

Bound fluorine in FSG becomes mobile with moisture absorption, and migrates to interfaces upon thermal cycling [44]. As such, FSG/Ta and FSG/SiN adhesion is both moisture and heat dependent. Lanckmans *et al.* [27] reported that SiLK and FLARE show no adhesion degradation with temperature cycles. However, Song *et al.* [10] showed that adhesion of SiLK to an oxide underlayer was degraded with anneals of $\geq 400°C$.

Porous oxide films with Si dangling bonds can easily absorb moisture, and passivation of the dangling bonds with hydrogen or methyl groups reduces moisture absorption in these films [84]. OSG and SiOC have been shown to be stable with respect to moisture and heat stress [85]. The presence of Si–CH_3 and Si–CH_n–Si bonds is the source of stability. However, samples degrade with heating above 400°C, and Si–H decomposes with moisture as per Eqs (3) and (4):

$$Si–H + H_2O \rightarrow Si–OH + H_2 \quad (3)$$

$$2Si–OH \rightarrow Si–O–Si + H_2O \quad (4)$$

Oxidation of HSQ and silica, caused by oxide cap deposition, results in reduced stability to moisture absorption and subsequent increase in dielectric constant due to the formation of silanol [22].

In a study on fatigue, Snodgrass *et al.* [3] purported that subcritical debonding may be caused by corrosion of strained bonds at the debond tip due to environmental moisture. Therefore, increased humidity allows debonding to propagate with considerably lower applied driving forces.

Moisture absorption may occur from the fab ambient. As such, the presence or absence of capping layers above low-κ dielectrics and the moisture barrier properties of those materials will influence the stability of the low-κ with respect to moisture. For materials highly susceptible to moisture-induced damage, queue times may be needed to minimize the time that etched or polished dielectrics are exposed to fab ambient [16]. Most lifetime testing involves high-humidity testing (e.g. autoclave).

The impact of thermal cycling on interface adhesion may depend on whether the materials were exposed to relevant etch/strip damage and moisture absorption prior to thermal cycling. For example, FSG/Ta is stable with thermal cycling if the FSG has not been subjected to moisture absorption, whereas the FSG/Ta fails the tape test if moisture absorption precedes thermal cycling.

Lifetime testing includes both temperature cycling and moisture exposure to simulate long-term environmental impact on device reliability. As such, the packaged die must be able to withstand any interface stress incurred from the moisture and thermal stressing. Pathways for moisture in a packaged die must also be considered to address the lifetime reliability of advanced semiconductor devices.

4.5.4.5 The die edge and other pathways for moisture in a packaged die

Even with the most effective moisture barriers in the dielectric stack, ultimately the edge of the die provides one of the most direct pathways for moisture introduction to the chip. The scribed edge of a die is shown in Fig. 4.9. Severe deformation is observed, along with interface delamination extending into the chip. Elaborate edge seals have been utilized to block diffusion, but may not be able to block severe delamination originating at the die edge. Originally implemented to prevent sodium penetration, edge seals on advanced devices are required to seal the die from moisture penetration as well.

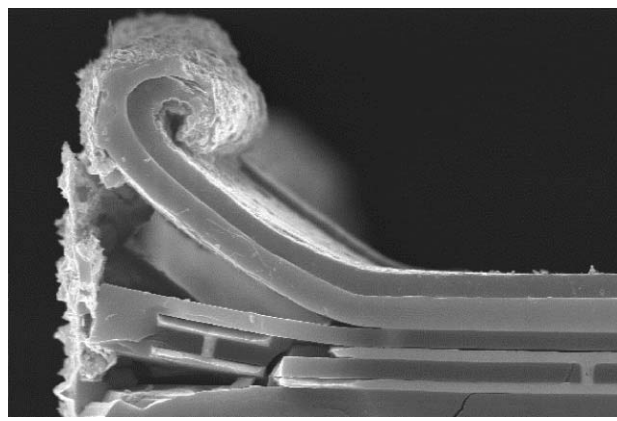

Fig. 4.9 SEM cross-sectional image of the scribed edge of a die.

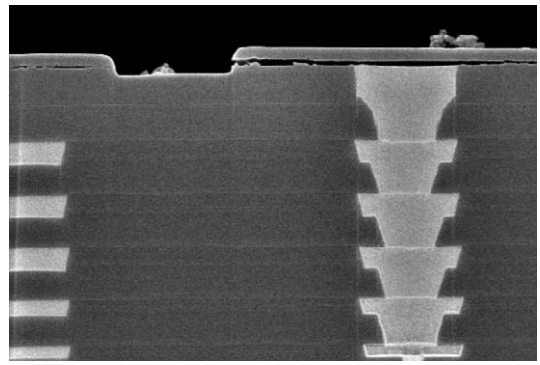

Fig. 4.10 SEM cross-sectional image of delamination at the interface of SiN and FSG at the terminal metal level.

Additional pathways for moisture exist where there is an uncapped opening in the final passivation. Such openings may occur at edge seals and fuse openings in addition to the die edge. Figure. 4.10 shows delamination at the interface of FSG/SiN following extended autoclave exposure.

4.5.4.6 The impact of the geometry of metal levels

Interface reliability is impacted by the number of metal levels in the device, and the location of the interface being studied. For example, an interface between a polymer and its oxide cap at last metal will have a different susceptibility to delamination than a polymer/oxide interface at the first metal level. Furthermore, the difference between the interface integrity of first and last metal, depends on how many levels are in between. This topic is largely confined to modeling evaluation, although some work has been reported on interface reliability of unpatterned multilayer dielectric stacks.

Predictive modeling has shown (a) that crack driving force decreases from last metal to the first metal level, (b) that an eight-level stack will have a higher crack driving force at upper layers compares to a four-level stack, and (c) the crack driving force at lower levels is higher for a four-level stack than for an eight-level stack [86]. These results are plotted in Fig. 4.11. In an eight-level stack, there is a higher number of softer layers to serve as stress buffers to the lower levels as compared to a four-level stack.

Using finite element modeling, Lee *et al*. [87] found that potential failures increase as the total number of Al interconnect layers increases. The lower metal lines are under higher stresses for the case of Al interconnects with gap-filled dielectrics. Metal stress increases as width is reduced, leading to a higher probability for voiding and cracking in the metal lines.

The height of the metal line can also influence adhesion at various interfaces. For Cu interconnects, TaN/SiO_2 interface fracture energy was shown to increase dramatically with Cu thickness due to plasticity contributions [88].

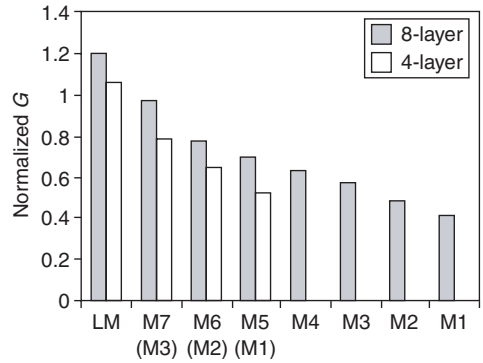

Fig. 4.11 Modeling results of crack driving force at the low-κ/passivation interface for a four-level stack versus an eight-level stack.

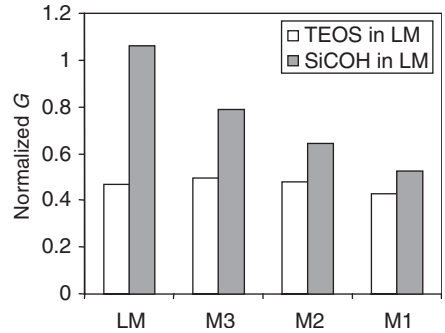

Fig. 4.12 Modeling results of the influence of final ILD on crack driving force at lower levels comparing TEOS and SiCOH as final ILD.

4.5.4.7 The impact of dielectric at last metal

Goldblatt *et al.* [21] reported on the use of a USG/FSG stack at terminal metal levels when SiLK is used at lower levels. As described previously, Fig. 4.9 shows delamination between the final ILD layer (FSG) and final passivation. Changing the terminal ILD layer to a material less susceptible to moisture-induced delamination eliminates the failure mechanisms shown in the figure.

The choice of dielectric at the final ILD layer not only affects reliability at that level, but also impacts interface integrity at lower levels, as related to the dissipation of packaging stresses through the stack. Reliability of an interface at the first metal level depends not only on the total number of metal levels (as described in Section 4.5.4.6), but also on which materials are used at those upper layers. This is illustrated in Fig. 4.12 in which the impact of the last metal dielectric on the crack driving force at the low-κ/passivation interface at lower levels is shown [86].

4.5.5 Predicting interface properties using modeling

The current state-of-the-art for adhesion measurements requires unpatterned stacks for measurement. Detailed stress distribution profiles cannot be experimentally measured for complex devices. Modeling can be used to predict various stress-related failure mechanisms associated with complex interconnect geometries (e.g. metal aspect ration, number of metal levels, tiling density, slotting density, etc.) based on the properties of unpatterned film stacks and predict how these stresses change during processing. Finite element modeling and fracture mechanics approaches have been used to predict interface reliability for complex structures.

4.5.5.1 Finite element modeling

FEM modeling is used to determine the local stress distribution and evolution during manufacturing for complex multilayer structures [87]. This modeling method utilizes a plane strain formulation to predict wafer curvature in directions parallel and perpendicular to the lines, resulting from both patterning and thermal cycling [89].

Modeling fracture resistance of interface in multilayer structures involves including dissimilar elastic properties, metal layer thickness, yield properties, interface properties, and loading mode mixity. This mixed mode loading refers to the presence of multiple stress modes (e.g. tensile and shear stress) at the debond crack [90]. Studies show that ductile layer deformation properties, cohesive parameters, elastic layer thickness between the debonding interface and the ductile layer, and the phase angle of loading have the most significant effect on interface fracture resistance [88].

The continuing trends towards high-aspect-ratio metal lines and multilayer structures yields an increase in thermo-mechanical stress and an increasing probability of stress-related failure mechanisms [91]. FEM methods have been employed to evaluate the impact of repeated thermal cycling of upper metal levels on stress evolution in the lower level metals [105].

FEM does not employ information on interface adhesion in the modeling and as such cannot be used to predict delamination. Additionally, modeled stress using FEM depends on the mesh density used in the model, with highly refined mesh giving increasingly higher stress [83].

4.5.5.2 Fracture mechanics approach

Fracture mechanics is used to (a) experimentally measure fracture resistance of a material under monotonic and cyclic loadings and (b) assess structural integrity using these data. It utilizes experimentally measured quantities to correlate macroscopic geometry and loads to microscopic fracture processes. Unlike the thermal mechanical approach of finite element approaches, fracture mechanics includes the experimentally measured adhesion and mechanical properties of the materials used.

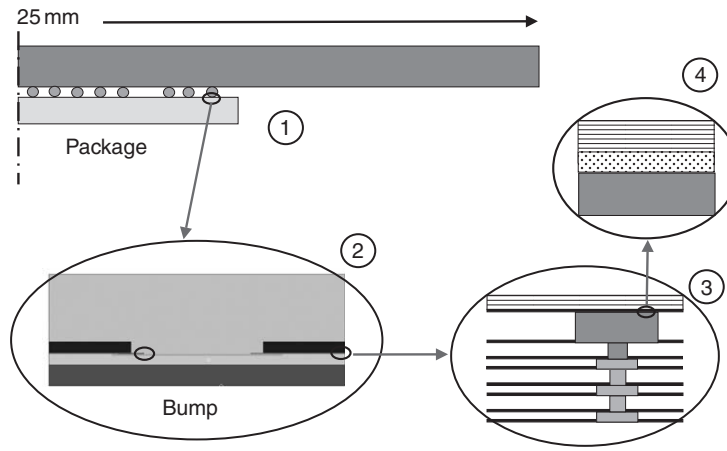

Fig. 4.13 Schematic diagram of the multi-level multi-scale submodeling technique used to evaluate the impact of the global packaging process on the local die-level structures.

Good correlation between the fracture mechanics model of the dependence of interface toughness on Al–Cu thickness and experimental measurements has been seen [92]. Fracture mechanics has been used to study adhesion failures, the role of plasticity in toughness, and crack growth resistance in ductile materials. Fracture mechanics approaches are also useful to predict the resistance of multilayer structures to mechanical failures during packaging.

Perhaps the most powerful method to predict interface failure is to couple FEM with fracture mechanics. In a method described by Mercado *et al*. [83] to investigate the impact of flip-chip packaging stresses on low-κ dielectric structures, a multi-level, multi-scale submodeling technique was used, as schematically depicted in Fig. 4.13. This technique provides the ability to incorporate the global models with the local die-level structures. By using fracture mechanics to predict delamination, it is possible to incorporate experimentally measured interface toughness and eliminate the dependence on modeling mesh density.

4.6 Impact of interfaces on performance and reliability

Interfaces have a clear impact on mechanical reliability, with delamination as the most visible outcome. Transistor performance, backend RC delay, EM resistance, and yield enhancement effectiveness are also impacted by the compatibility of dielectrics with other materials. In this section, the impact of dielectric interfaces on various components of performance and reliability will be discussed. Further discussion of the impacts of dielectrics on reliability will be included in Chapter 12.

4.6.1 Impact of interfaces on mechanical reliability

Mechanical reliability failures can occur during device fabrication (e.g. capping layer delaminating from porous low-κ during CMP) or packaging (e.g. wirebond stresses result in delamination of a Ta/FSG interface in the chip). There is essentially an internal stress budget that each interface and low-κ materials can endure. Exceeding this budget during CMP or packaging will produce either adhesive or cohesive failures, depending on which is the weaker force for a given material integration.

4.6.1.1 Impact of interfaces on CMP

In addition to films-based work to strengthen the cohesion and adhesion of films, process modifications are being developed to minimize the stresses associated with CMP processing. Preventing delamination of dielectric films has been a focus of advanced CMP process and equipment development. Downforce and platen speed have been found to be important parameters for modulating delamination [43].

Again, porous films are more susceptible to this failure mode due to the low mechanical strength of the porous materials relative to the downward and shear stresses applied [28]. Additionally, low-κ damage (e.g. chemical modification of surface or penetration of process gases into the low-κ) from cap deposition creates another weak interface between the intact low-κ and damaged low-κ dielectric. Cohesive failures may also occur during CMP of porous films.

Scherban *et al*. [48] found that the adhesion between capping layer and low-κ must exceed 5 J/m^2 (as measured by four-point bend) in order to withstand CMP processing intact. Interface integrity determines downforce limits for CMP, and delamination susceptibility impacts defectivity from CMP. The probe pad delamination shown in Fig. 4.7 would certainly lead to incompatibility with CMP processing. Further discussions of CMP related interface failures are included in Chapter 12.

4.6.1.2 Impact of interfaces on package reliability

Both wirebond and C4 packaging methods involve thermal and mechanical stresses on the die. Additionally, the packaging and assembly processes result in new interfaces potentially exposed to moisture, as described in Section 4.5.4.5 Even if the interfaces are strong enough to withstand CMP, package stresses may still produce interface related failures.

Braeckelmann *et al*. [32] found that the interface between the last metal Cu and final passivation delaminates during the C4 die pull test. Figure 4.14 shows the C4 BUMP delamination from the bond pad at the Cu/SiN interface. The authors further showed that this failure mechanism is eliminated when the interface adhesion is improved (e.g. CuMg alloy is used instead of Cu).

Wirebonding of die with FSG at final ILD has been shown to be susceptible to delamination at the interface between the *inter*layer FSG and overlying metal barrier in the bond pad,

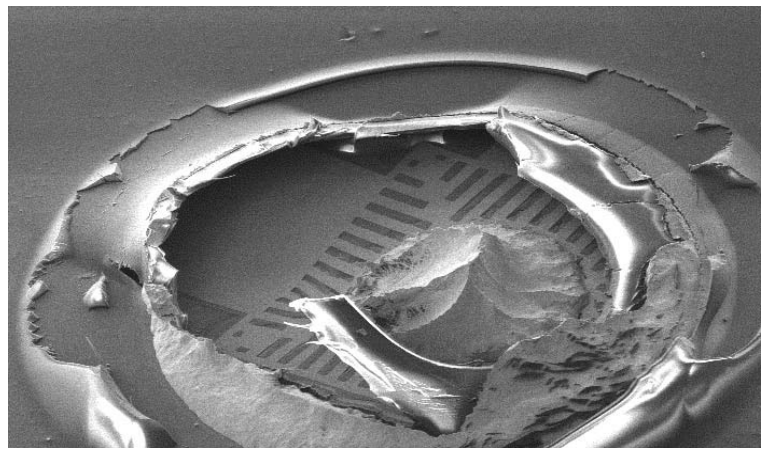

Fig. 4.14 FIB image of C4 BUMP die pull failures showing that the final passivation has delaminated from the Cu at the terminal metal level.

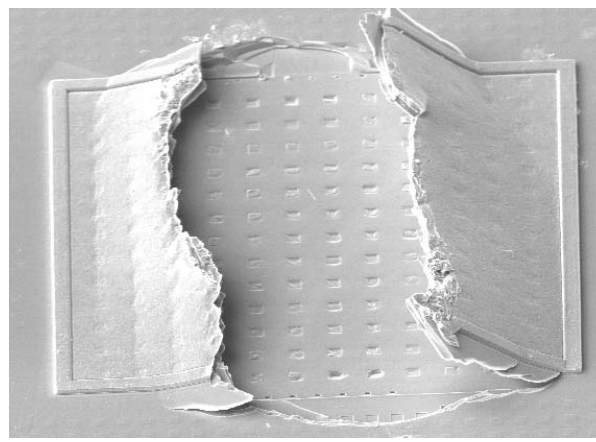

Fig. 4.15 Delamination along FSG/barrier interface upon wirebonding, when FSG is used as final ILD.

depending on wirebonding conditions, as shown in Fig. 4.15 [86]. Wirebonding with other low-κ materials at final ILD have also shown interface reliability issues depending on die attach and wirebond conditions. The use of standard SiO_2 in final levels eliminates such wirebonding failures.

Changing pattern density has been used to address package reliability issues associated with low-κ polymer integration. Goldblatt *et al*. [21] implemented a 'sea of vias' as reinforcement beneath the terminal metal pads to provide adequate mechanical reliability to withstand wirebond stresses when SiLK is used as the ILD. The authors additionally used a USG/FSG instead of a low-κ stack at upper levels, where fuses reside.

4.6.2 *Impact of interfaces on RC delay*

For logic devices in particular, clock frequency is a critical metric for success in the marketplace. For backend-limited devices, RC delay dominates the overall chip speed. As such, minimizing dielectric constant is essential. Increases in ILD dielectric constant, and in turn, capacitance, due to etch, photoresist strip, CMP, and moisture uptake (as described in Section 4.5.4) can result in the reduction or elimination of all of the capacitance benefits that the low-κ ILD was intended to provide. Even without damaging the low-κ material, capping layers, inserted as hardmasks or to protect porous materials from CMP, will also increase the effective capacitance. Damaged surfaces that result in localized increases in dielectric constant will have the greatest RC impact on minimum pitch structures, with negligible RC increase for large pitches.

Dielectric interfaces can impact the resistance component of RC delay as well. If barrier metals react with the underlying low-κ material, the resistance of the barrier may increase, thereby increasing the line resistance [7]. As described in Section 4.3.2.2, barrier thickness may need to be increased in order to seal porous materials from Cu diffusion. Any increase in barrier thickness will have significant impact on the resistance of fine-pitch structures. Additionally, delamination of capping layers during CMP impacts dishing/erosion performance and subsequent resistance distribution. A more detailed discussion of integration-related damage to low-κ dielectrics and the associated increase in dielectric constant is included in Chapter 12.

4.6.3 *Impact of interfaces on EM performance*

The fast diffusion path leading to electromigration failure in Cu interconnects is along the interface between Cu and the dielectric barrier [33, 93, 94, 100, 101]. In terms of copper interconnects, there have been no thorough studies published on how changes in the Cu/passivation interface (e.g. Cu oxide removal, CMP residue removal, passivation with hydrogen) affect EM performance.

Martin *et al*. [41] found that the use of a pretreatment prior to depositing the dielectric barrier SiCN modifies the Cu/SiCN interface, leading to excellent adhesion and reduced CuO at the Cu/SiCN interface. As shown in Fig. 4.16, the SiCN split with the pretreatment substantially outperforms the SiN, with higher median time to failure (MTTF) and higher activation energy.

Electromigration resistance in Al interconnects can also be modulated by the choice of dielectric encapsulating the metal line, with a compliant polymer coupled with a thin SiO_2 film having longer lifetimes than a rigid thick SiO_2, and unpassivated lines having the shortest lifetimes [95].

Tsai *et al*. [96] observed electromigration failure to occur due to copper extrusion along the SiOC/SiN interface. They proposed that elimination of this failure mechanism requires improved adhesion between SiN and SiOC.

Electromigration testing typically includes measurements at temperatures above 300°C for activation energy calculations. As a result, interfaces need to be stable and not introduce failure

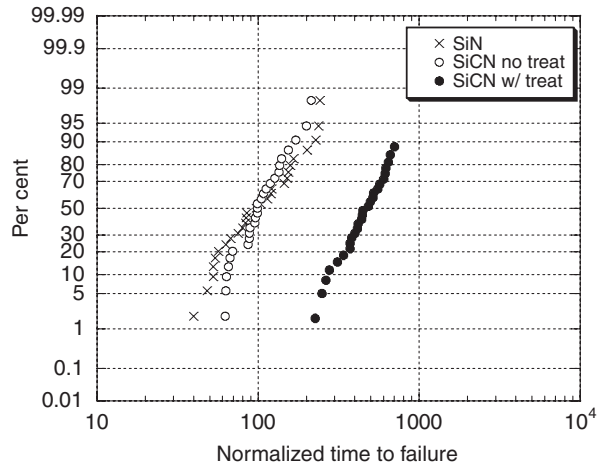

Fig. 4.16 Electromigration performance of SiCN as a function of pre-treatment used.

mechanisms unique to elevated temperatures testing. A more detailed discussion of dielectric reliability is included in Chapter 12.

4.6.4 Impact of interfaces on yield enhancement capability

As described in Section 4.3.1, Cu hillocks form when polished Cu is exposed to high temperatures prior to deposition of the dielectric barrier. Hillock formation is influenced by stress, thermal history, surface condition, grain size, and orientation of the copper.

While typical hillocks have not been shown to impact yield or reliability directly, they are classified as nuisance defects by many defect metrology tools. The signal swamping caused by a high density of hillocks requires the sensitivity of the defect metrology to be reduced, thereby reducing the probability that a real yield limiting defect will be detected.

4.7 Conclusions

Dielectric compatibilities have been described for a variety of materials in a variety of integrations. The distinctions between interface properties of porous and dense dielectrics, organic and silicon-based dielectrics have been discussed with respect to interfaces formed with dielectric barriers, capping layers, etch stop layers, and conductive barriers. Various techniques used to characterize interface composition and adhesion were described and compared. The complexities involved in inferring interface reliability in real devices, from properties measured on un-patterned substrates were addressed. Modeling was described as a method to extrapolate interface reliability based on measured quantities.

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Chapter 5
Silicon-based dielectrics

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Abstract

Silicon-based dielectrics are the most widely used materials in the semiconductor industry. These include oxides (both doped and undoped), nitrides, oxynitrides, and carbides. Their applications span from the front-end device isolation steps to the back-end interconnect steps. This is due to their compatibility to the silicon substrate. In this chapter, we mainly focus on the deposited silicon-based dielectric films, and do not include the thermally grown silicon oxide or nitride films. The deposition techniques of Si-based dielectrics include both thermal and plasma assisted CVD. Their resultant film properties, including both mechanical and electrical properties, and their consequent applications in the semiconductor fabrication process are extensively discussed.

5.1 Introduction

During integrated circuit fabrication, dielectric layers are used for both active and passive functions. The active dielectrics are those used for charge storage in the transistor and capacitor, as well as those used for isolation between adjacent transistors and the metal lines. The passive dielectrics are those used in antireflection coating, dielectric diffusion barriers and caps, etch stops layer as well as passivation layers. Various chemical vapor deposition (CVD) techniques are used to deposit these films. They can be divided into thermal- and plasma-assisted CVD processes. Thermal CVD process include low-pressure CVD (LPCVD), atmospheric (AP) and sub-atmospheric (SA) CVD, while plasma-assisted CVD includes conventional low-density plasma-enhanced CVD (PECVD) and high-density plasma CVD (HDPCVD). This chapter describes the current methods used for depositing silicon-based dielectrics, their deposition chemistry, their resulting material properties, and their applications in semiconductor microfabrication.

5.2 Deposition techniques

5.2.1 Thermal chemical vapor deposition process

5.2.1.1 Low-pressure chemical vapor deposition

This technique is also refers to as thermal CVD, due to its high-temperature process. The dielectric deposition is typically carried out in a tube furnace. A vertical furnace is commonly used today, although the industry has moved towards a single-wafer reactor as shown in Fig. 5.1.

The vertical furnace typically consist of a quartz tube, heated by a three-zone heater, with gas introduced from the bottom of the tube and exhausted on top. The wafers are held and stacked vertically on a quartz boat across the length of the tube. Typical operating pressure range between approximately 200 mTorr and 2 Torr.

Individual gases are introduced into the chamber through a shower head and mixed inside the chamber, the wafer sits on top of a resistive heater, and at the bottom a nitrogen purge is introduced to prevent reactant gas and particle buildup in the lift pin area, which is used to lift the wafer for transport. Typical operating pressure ranges between 10 and 200 mTorr. High-temperature silicon oxide and nitride films, which are typically used in the front-end process for the fabrication of the transistor and capacitor device layers, are most commonly deposited by these techniques.

Silane and ammonia are typically used to deposit silicon nitride (Si_3N_4) film at temperatures between 700 and 800°C, although dichlorosilane is more commonly used today. The chemical reactions are:

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$$

Si_3N_4 deposited by conventional high-temperature LPCVD techniques is typically stoichiometric, has good uniformity and film quality. The LPCVD Si_3N_4 film is typically denser that plasma-deposited Si_3N_4 and has lower H content.

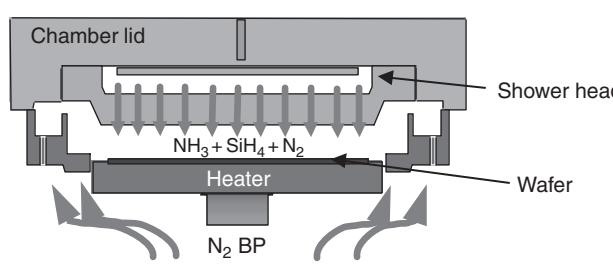


Fig. 5.1 A single-wafer LPCVD reactor.

The key advantages of a single-wafer reactor process compared to that of a batch furnace are: (a) lower thermal budget, which becomes more important with device shrinks; (b) uses non-chlorine chemistry for thermal nitride deposition, that is, SiH_4 chemistry is used in a single-wafer reactor while dichlorosilane is typically used for furnace processes, this could cause the incorporation of unwanted Cl into the film, which may react with polysilicon and cause film cracking; and (c) better particle performance, which affects device yield. Some of the disadvantages observed with the film deposited from a single-wafer reactor compared to the furnace are: (a) higher H content, which may affect charge storage properties; (b) film uniformity across the wafer; and (c) pattern loading effect.

Some of the applications for these high-temperature oxide and nitride films include chemical mechanical polish (CMP) stopping layer for shallow trench isolation, oxide hard mask for deep trench etch in DRAM capacitor, sidewall spacer for capacitor isolation in DRAM devices, as well as for salicide formation in logic devices. These will be illustrated in Section 5.4.

5.2.1.2 Atmospheric (APCVD) and sub-atmospheric chemical vapor deposition (SACVD)

APCVD and SACVD are commonly used to deposit undoped silicate glass (USG), phosphosilicate glass (PSG), and borophosphosilicate glass (BPSG) at a temperature range of 400–600°C. Both APCVD and SACVD reactors require an ozonator that generates ozone (O_3) to react with tetraethyl-orthosilicate (TEOS), forming SiO_2. The structure of TEOS is shown in Fig. 5.2. The TEOS:O_3 chemistry offers excellent gap-filling capability for the USG, PSG, and BPSG applications.

Trimethylphosphite (TMP) or triethylphosphate (TEPO) has been used as precursor for phosphorus dopant whereas trimethylborate (TMB) or triethylborate (TEB) has been used as precursor for boron dopant.

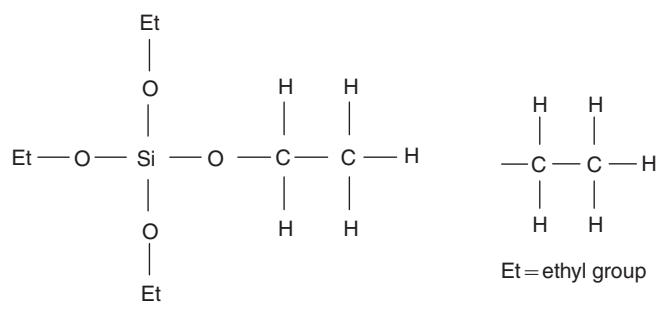


Fig. 5.2 Structure of TEOS.

In a typical atmospheric reactor, wafers lie on top of a horizontal heater with reactive gases flowing over the substrates at atmospheric pressure, that is, 760 Torr. In an APCVD batch reactor, multiple wafers rest on top of a large 'pancake' heater and are processed at the same time. In a continuous reactor, wafers are transported through the reactor on a conveyer belt. Inert gas curtains around the outer edge of the reactor are used to contain the reactive gases.

The typical hardware for SACVD is similar to that of a single-wafer LPCVD reactor discussed above. The operating pressure of the SACVD process ranges from 20 to as high as 600 Torr; hence, 'Sub-atmospheric'.

SACVD is generally preferred over APCVD for PMD applications since it offers better particle performance without using high-flow inert gas curtains and higher productivity, allowing a larger number of wafers to be processed in the reactor before a wet clean is needed.

5.2.2 Plasma-assisted chemical vapor deposition

5.2.2.1 Plasma-enhanced chemical vapor deposition

After the first metal layer has been deposited, conventional LPCVD processes, which are typically of higher temperatures (i.e. > 450°C), can no longer be used because they will melt the metal, cause hillocks or electromigration problems. Any subsequent deposition must be done at low temperature (less than 450°C). In order to accomplish this, an electrically charged gas, called plasma, is used to provide the energy for the deposition reaction. The plasma density of PECVD is typically low. A typical single-wafer PECVD reactor is shown in Fig. 5.3.

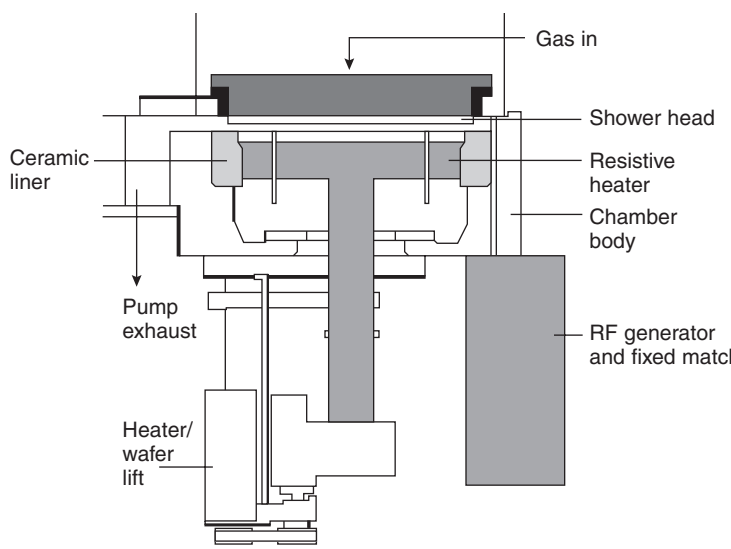


Fig. 5.3 A typical PECVD chamber.

This chamber is also called a 'cold wall' reactor since the chamber body is usually maintained between 60 and 70°C. The substrate is placed on a heater made of either aluminum or ceramic and heated to a temperature of around 400°C. The heater and the chamber wall are grounded electrically whereas the showerhead is the powered electrode. The process pressure is relatively low, in the 0.5–15 Torr range. After the gas flows and the pressure is stabilized, radio-frequency (RF) energy is applied to the chamber to generate a plasma, ionizing the reactive gases. One of the advantages of plasma-enhanced deposition is that the wafer temperature can be maintained relatively low. Conventional LPCVD processes usually require temperatures substantially higher and are not suitable for certain substrate materials such as aluminum or copper. Typically, RF at 13.56 MHz is used for generating the plasma, although in some cases mixed frequencies of 13.56 MHz and 450 kHz are used to control film stress and other film properties.

5.2.2.1.1 Oxides

5.2.2.1.1.1 Undoped silicon dioxide and fluorosilicate glass

Two common precursors used to form PECVD USG and FSG are silane (SiH_4) and TEOS.

SiH_4 USG is formed by the reaction of SiH_4 with nitrous oxide (N_2O) over a substrate temperature of ~400°C in the presence of plasma. Since SiH_4 and N_2O are fairly reactive, only a low RF power (~300 W) is needed to sustain the plasma. On the other hand, since the reaction is in the flow-limited regime, sufficiently high SiH_4 flows and pressure (in the Torr range) are necessary to achieve a high deposition rate. Silicon tetrafluoride, SiF_4, is used as the precursor for fluorine in the FSG deposition.

TEOS is a liquid precursor that has been used for high-temperature oxide deposition in furnaces since the 1960s. [1, 2]. TEOS oxide has been known to have more conformal step coverage than SiH_4 oxide even over high aspect ratio structures [3]. The challenge is to deposit TEOS-based USG at a low enough temperature so that the film can be used as an inter-metal dielectric.

Starting at the 0.18 μm and below technology node, the gap fill requirement for aluminum interconnect has become too stringent for conventional PECVD techniques, even with TEOS USG, to achieve satisfactory results. Hence, device manufacturers have shifted to a different gap fill technology called HDPCVD, which will be discussed later in the chapter. PECVD TEOS films are then used as capping layers over the HDPCVD films, where the step coverage requirements are much less stringent. SiF_4 is also used as the fluorine precursor for TEOS FSG.

5.2.2.1.1.2 Carbon-doped oxide

Carbon-doped oxide (CDO), also known as organosilicate glass (OSG) or silicon oxicarbide (SiOC), can be deposited in a parallel-plate PECVD chamber. Various precursors have been used to deposit CDO films, including methylsilane, dimethylsilane, trimethylsilane (TMS) [4], and tetramethylsilane (4MS). Precursors with more methyl groups are capable of incorporating more carbon into the film, though the compounds are more difficult to dissociate. Therefore, 4MS, a liquid precursor, in general, deposits at a lower rate than that of TMS, which is a gas.

Other precursors such as tetramethylcyclotetrasiloxane (TOMCATS), octamethylcyclotetrasiloxane (OMCTS) [5], dimethyldimethoxysilane (DMDSO) [6] have also been demonstrated in CVD of CDO films.

TMS and O_2 chemistry has been the most widely accepted method for depositing CDO film thus far due to the industry familiariarity with the precursors and its simple gas-delivery system. TMS and O_2 are typically introduced into the chamber through separate gas lines, with or without carrier gases, in order to prevent any pre-mature reaction before they reach the chamber. Deposition temperature is usually kept below 400°C, preferably at around 350°C, since the dielectric is used between metal layers.

5.2.2.1.2 Nitrides (SiN)

Plasma-deposited silicon nitride has been widely used in microelectronic device fabrication for years. The applications include final passivation layer, diffusion barriers against mobile ions, and moisture barriers. Recently, silicon nitride film applications have been extended to advanced dual damascene processing, such as copper diffusion barrier and middle etch stop due to the film's excellent barrier properties against copper and the high etch selectivity to low-κ dielectric films.

Copper oxidizes readily in air. Therefore, before silicon nitride is deposited over copper, the native copper oxide must be removed first. A plasma treatment consisting of a hydrogen containing a gas such as ammonia (NH_3) is typically used to reduce the copper oxide to metallic copper in PECVD chambers [7].

The reaction of ammonia gas with copper oxide is as follows:

NH_3 + Plasma = NH_2 + H
CuO + H = CuOH intermediate step
CuOH + H = Cu + H_2O

After the CuO removal step, SiH_4 is introduced to the chamber to react with ammonia, forming silicon nitride. It has been found that copper will start reacting with SiH_4 at temperature as low as 200°C. After CuO has been removed, if copper is exposed to an environment with high concentration of silane, copper silicide will be formed. It is known whether uncontrolled copper silicide formation on the copper surface increase the resistivity of copper inter-connections and degrades the adhesion of barrier layer. Very often, people refer copper silicide to as 'green' or 'black' copper.

5.2.2.1.3 Oxynitrides (SiON)

A typical single-wafer PECVD reactor with a 400°C heater is used for SiON deposition. A gas mixture of SiH_4 and nitrous oxide (N_2O) is introduced into the process chamber before high-frequency RF power is applied.

In addition to SiH_4 and N_2O, sometimes helium or nitrogen can be added to the reaction for various reasons. In the pressure and spacing regime the PECVD SiON process operates, helium requires a lower breakdown voltage than nitrogen [8]. Since helium is easier to breakdown, it helps to stabilize the plasma during deposition.

After SiON deposition, the film surface is treated by either capping the film with a very thin layer of silicon oxide or striking an oxygen-containing plasma to oxidize the SiON surface. The purpose of the treatment step is to prevent any interaction between the SiON film and the photoresist, causing 'poisoning' problems. Detailed discussion on poisoning will be covered in Section 5.4.

5.2.2.1.4 Silicon carbide

Silicon carbide is typically deposited in a parallel-plate PECVD reactor at around 300–400°C. Sometimes, the same chamber can be used for CDO deposition also. Since silicon carbide is also deposited over copper, a copper oxide removal step similar to that used for silicon nitride is also required prior to silicon carbide deposition. A similar chemistry involving ammonia and/or hydrogen is also used to reduce the native copper oxide.

TMS and 4MS are common precursors for depositing silicon carbide. Sometimes, helium and ammonia gases are added during the process to stabilize the plasma and improve the hardness of the film. However, using ammonia also incorporates nitrogen in the film, resulting in higher dielectric constant (~5) and resisting poisoning issues with 193-nm lithography than the film without nitrogen. Therefore, silicon carbide films for low-κ applications are also known as SiCH or SiCHN, depending on whether the precursors contain nitrogen or not. To further ensure good adhesion of SiCH to CDO, helium plasma treatment is sometimes performed on the wafer after film deposition.

5.2.2.2 High-density plasma chemical vapor deposition

Starting at the 0.18 μm and below technology node, the aspect ratio for gap fill requirement has become more and more challenging for PE TEOS USG to fulfill. Device manufacturers have shifted to a different gap fill technology called HDPCVD, which utilizes a new concept of depositing and sputtering at the same time to successfully fill the high aspect ratio gaps. (Fig. 5.4)

The key difference between an HDPCVD chamber (Fig. 5.5) and a conventional CVD chamber is that it simultaneously deposits and sputters in the same chamber. High-density plasma generates more ions and gives more directional deposition. It also yields higher sputtering rates.

Therefore, an HDPCVD chamber is designed with these objectives in mind. Key hardware components of the chamber include a turbo pump, RF power delivery (source and bias), gas distribution, monopolar or bipolar electrostatic chuck (ESC), and helium cooling.

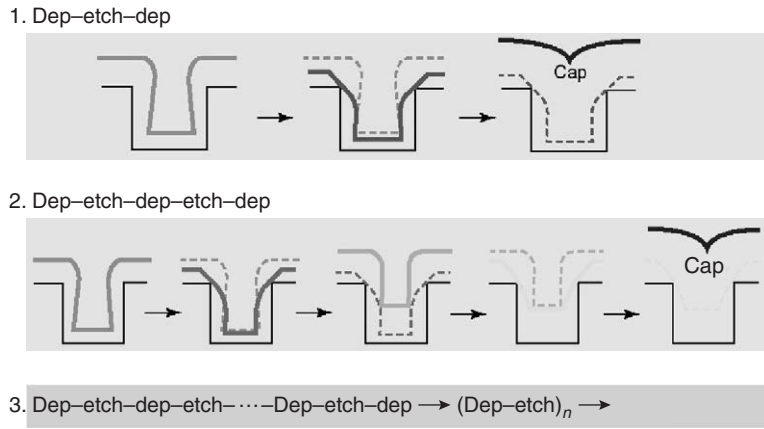


Fig. 5.4 Dep/etch concept of HDPCVD.

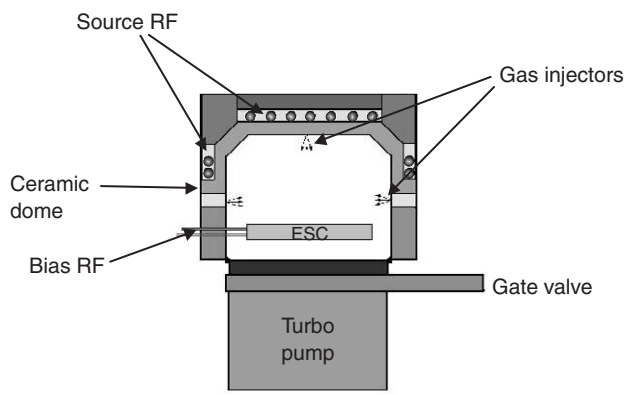


Fig. 5.5 Schematic of an HDPCVD chamber.

The dome and process kit components are made of ceramic mainly due to the requirements of low mobile ion contamination. In addition, the dome has to be made of dielectric material in order to allow the coils to couple into the chamber for high-density plasma generation. The turbo pump enables the chamber to operate in the 2–10 mTorr range. Low pressure is necessary to lengthen the mean free paths of the ions that are responsible for high sputter etch rates.

The bias RF generator delivers capacitively coupled energy to the ESC for sputtering whereas the source RF delivers inductively coupled power to the chamber through the coils and the dome and provide directional deposition.

Gases are delivered to the chamber through injectors that are distributed around the dome to provide uniform and symmetrical gas dispersion. Silane and oxygen are introduced separately into the chamber to prevent any undesirable upstream reaction. Argon is used to enhance the sputtering component. The ESC holds the wafer to allow helium backside cooling without mechanical clamping. Helium cooling is critical since wafer temperature could reach

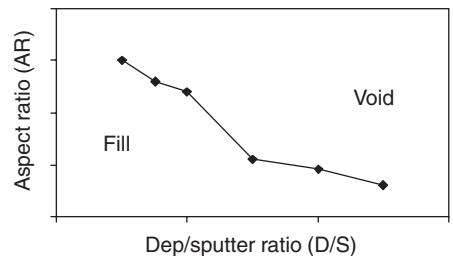


Fig. 5.6 Gap fill window as a function of D/S ratio and aspect ratio.

over 400°C during deposition and it is essential to conduct heat away from the wafer to avoid damage to the devices. Electrostatic chuck clamping is preferred over mechanical clamping since it provides much better particle performance.

Since HDPCVD is a combination of deposition and sputtering at the same time, proper deposition to etch ratio is required in order to achieve optimal results. Too much deposition and too little sputtering will generate cusping of deposited oxide, resulting in poor gapfilling and formation of voids. Too much sputtering relative to deposition can result in corner-cutting in the underlying film, either in the metal or the anti-reflective coating layer on top of the metal, which in some cases can cause leakage currents and device failure. Therefore, a balance between deposition and sputtering has to be established. The ratio between the two rates is called the D/S ratio, which has to be adjusted depending on the underlying topography and aspect ratio of the gap. The effect of different D/S ratios is shown in Fig. 5.6. In general, the higher the aspect ratio, the lower the D/S ratio required to fill the gap void free.

Sputtering is the result of ions bombarding the surface. As ions accelerate to the substrate, any collisions that occur will cause energy to be lost due to elastic/inelastic collisions. By minimizing the chamber pressure, the mean free path between collisions is increased and, therefore, minimal energy is lost. In addition, argon, which is a heavy ion, is used in HDP to enhance the sputtering rate.

HDPCVD can also be used to deposit FSG and PSG. Similar to PECVD, SiF_4 and PH_3 are used as precursors for fluorine and phosphorus, respectively.

5.3 Properties of Si-based dielectrics

5.3.1 Oxides

5.3.1.1 Undoped silicate glass

All three deposition methods, that is, PECVD, HDPCVD, and SACVD, can be used to form USG. However, some properties of the resulting USG films could be very different, depending on which deposition technique is used.

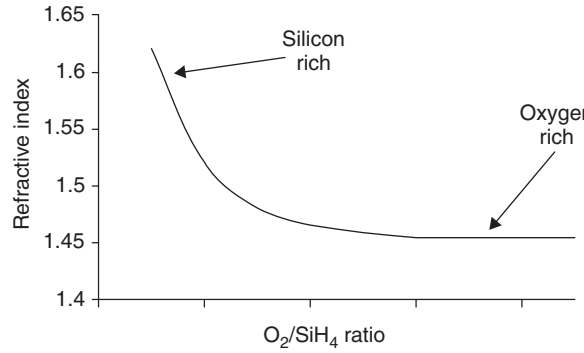


Fig. 5.7 Refractive index as a function of O_2/SiH_4 ratio.

The dielectric constant of CVD USG films is around 4.0 ± 0.2 whereas the refractive index (RI) is typically at 1.46 ± 0.005. However, silicon-rich films with refractive index of 1.5 can be achieved by lowering the flow ratio of the silicon precursor such as SiH_4 to the oxygen precursor such as N_2O. On the other hand, a perfectly stoichiometric film with an RI of 1.46 can also be achieved by adjusting the flow ratio (Fig. 5.7).

Fourier transform infrared (FTIR) spectra of a stoichiometric oxide film and a Si-rich oxide film show no Si–H peak at $2250\,cm^{-1}$ and a significant Si–H peak, indicating that Si dangling bonds might be present in the Si-rich film. These dangling bonds are highly polarizable and therefore are responsible for the high refractive index.

The film stress is typically compressive for HDP and PECVD oxide, in the range of $1–2 \times 10^9$ dyn/cm^2 while that for SACVD USG films is usually tensile. Both the HDP and PECVD oxide films demonstrate minimal changes after thermal anneal whereas SACVD oxides shrink and densify after thermal treatment.

Wet etch rate of CVD films in a buffer oxide etch solution is commonly used to measure relatively how dense the oxide films are when compared to thermally grown oxides. Although HDP, PECVD, and SACVD oxides are not as dense as thermally grown oxides, the wet etch rate ratio (WERR) of CVD oxides to thermal oxides is still less than 2.

Deposition rates vary in great degrees depending on which deposition technique is used. Over 1 μm/min deposition rate is readily achievable for PECVD oxides whereas up to 5000 Å/min is more likely found in HDP- and SACVD oxides.

Absence of metallic contamination is extremely critical when HDP- and SACVD oxides are used in the front-end applications. Since HDPCVD chambers perform gap fill by depositing and sputtering simultaneously, the chamber is more susceptible to metallic contamination. Therefore, the process kit in the HDPCVD chamber is typically made of ceramic in order to achieve a metallic contamination level below 5×10^{10} atoms/cm^3. Since the SACVD process is strictly a thermal one, low metallic contamination can easily be accomplished.

5.3.1.2 Fluorosilicate glass

Fluorine ions are very electronegative. When fluorine is bonded to the Si–O structure, electrons from the Si–O bond are drawn towards the electronegative fluorine side. This electron shift weakens the Si–O bonds and makes the entire oxide structure less polarizable, resulting in a lower dielectric constant. However, weakening of the Si–O bonds also reduces the hardness and mechanical strength of the FSG film. Furthermore, the hydrophilic nature of fluorine tends to increase the moisture absorption of the oxides. After the film has been exposed to a wet environment such as CMP, formation of hydrofluoric acid (HF) could possibly corrode the adjacent metals and cause adhesion problems. The maximum amount of stable fluorine incorporation is about a 6–8% for the inter-metal dielectric application. Regardless of the fluorine content, process optimization is required in order to achieve stable FSG films. The flow ratio of SiF_4 to silicon precursor has the strongest effect on the amount of fluorine in the resulting FSG film. Increasing SiF_4 flow decreases refractive index, and increases fluorine concentration. The relative fluorine concentration can be determined by the ratio of the peak heights of Si–F at ~937 cm^{-1} and Si–O at ~1081 cm^{-1} using FTIR spectroscopy as shown in Fig. 5.8.

Thermal Desorption Mass Spectroscopy (TDS) analysis can be used to study properties of FSG films (Fig. 5.9). When the film is heated to 800°C, any unstable species will start desorbing out of the film and species such as fluorine (F), water (H_2O), hydrogen (H_2), and hydrogen

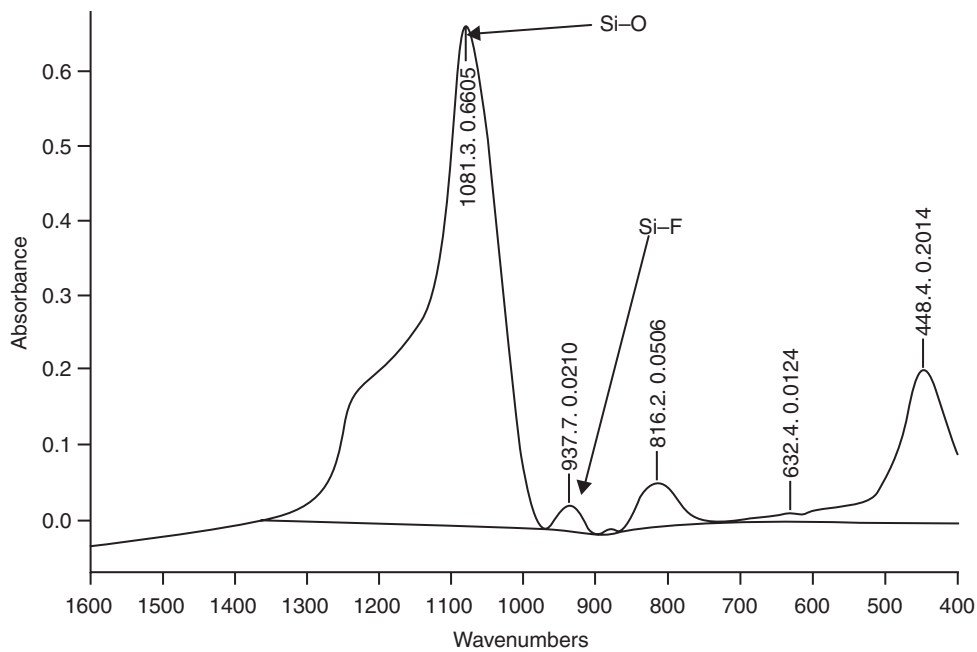


Fig. 5.8 FTIR of FSG film.

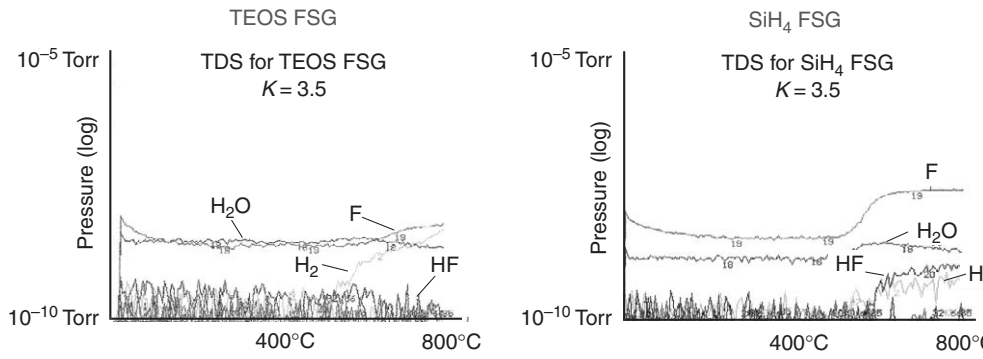


Fig. 5.9 FSG film stability analysis by thermal desorption spectroscopy.

fluoride (HF) can be detected using mass spectroscopy. The silane FSG (right) shows that F, HF, and H_2O start to out-gas at 500°C whereas the TEOS-based FSG (left) shows no F, HF, or H_2O evolution up to temperatures of 800°C (Fig. 5.9).

5.3.1.3 Phosphorus silicate glass

PSG has good gettering properties that remove metallic contaminants such as mobile ions from the devices so that no potential damage occurs. Typical phosphorus dopant concentrations range from 2 to 9 wt%. PSG films with phosphorus concentrations higher than 6% are usually less stable and more hygroscopic, potentially reacting with moisture in air and forming phosphoric acid. The peak height of the FTIR absorption band at $1330\,cm^{-1}$ (P=O) can be used to quantify the phosphorus amount. In general, higher dopant concentration results in higher deposition rate and higher wet etch rate. SACVD PSG films tend to be less stable and need to be densified at high temperature in order to convert the unstable P_2O_3 to P_2O_5 completely.

5.3.1.4 Borophosphosilicate glass

Boron concentrations in BPSG range from 2 to 6 wt% whereas phosphorus concentrations range from 2 to 9 wt%. Properties of BPSG, deposited with the SACVD method are sensitive to TEOS flow and deposition temperature, as shown in the Table 5.1.

Since the operating regime of SACVD is TEOS flow limited, increasing TEOS flow will increase deposition rate but at the same time lower the dopant to TEOS flow ratio, therefore lowering the resulting boron and phosphorus concentration in the film. Higher deposition temperature yields a denser film with more dopant incorporation.

BPSG films have as-deposited tensile stress at less than $1 \times 10^{10}\,dyn/cm^2$. Since the step coverage of as-deposited BPSG is not sufficient to fill the gap, the film has to be thermally

Table 5.1 Effect of TEOS flow and temperature on deposition rate and dopant concentrations

Parameter	Deposition rate	B%	P%
TEOS flow ↑	↑	↓	↓
Temperature ↑	↓	↑	↑

Table 5.2 FTIR absorption bonds in BPSG

Bond	Wavenumber (cm^{-1})
P=O	1330
Si–O	1050
B–O	930, 1350

annealed either in a furnace or a rapid thermal processing (RTP) chamber to flow the glass. Annealing the film also densifies it and makes it shrink.

Boron oxides have two FTIR absorption bands, that is, the B–O bond at 1350 cm^{-1} and the Si–O–B bond at 930 cm^{-1}. Determining the boron concentration is straightforward, that is, by evaluating the peak at 930 cm^{-1}. However, measuring the phosphorus concentration in BPSG is more tricky since the P=O peak at 1330 cm^{-1} overlaps with the B–O peak at 1350 cm^{-1} and the two peaks must be deconvoluted. The different absorption bands in BPSG are summarized in Table 5.2.

5.3.1.5 Carbon doped oxide

CDO, also known as SiOC and organosilicate glass (OSG) has a dielectric constant, κ value, between 2.2 and 3.0. The lower κ value is achieved by introducing porosity to the films through the incorporation of methyl groups. CDO films have a composition of $Si_wC_xO_yH_z$ with about 10–25% of the silicon atoms substituted with organic groups [9]. However, these methyl groups also affect other physical, thermal, and chemical properties of the CDO films [10].

Although CDO films are not as good as silicon dioxide films, they have many of the beneficial thermal and mechanical properties of silicon oxide. Table 5.3 shows a comparison of the properties between CDO and oxide.

CDO is a mixture of pores and the solid phase. Since pores are made of air with a dielectric constant of 1, the presence of pores in a solid material can lower the effective dielectric constant. Measurement of porosity allows one to understand the correlation between pores and the solid phase and therefore the dielectric constant.

The dielectric constant, κ, of the CDO film can be derived as

$$\kappa = (1 - \mathrm{P})\kappa_0 + P\kappa_{\mathrm{air}} = \kappa_0 - (\kappa_0 - \kappa_{\mathrm{air}})P$$

Table 5.3. Flim properties' comparison between CDO and SiO_2

Mechanical properties	CDO	PECVD SiO_2
Dielectric constant	< 3.0	4.2
Refractive index	< 1.42	1.46
Stress	Tensile	Compressive
Hardness	< 2.0 GPa	7–9 GPa
Young's modulus	<10 GPa	70–80 GPa
Mass density	< 1.4 g/cm^3	2.2 g/cm^3
Thermal conductivity	< 0.4 W/mC	~1 W/mC
Coefficient of thermal expansion	< 10 ppm/°C	< 1 ppm/°C

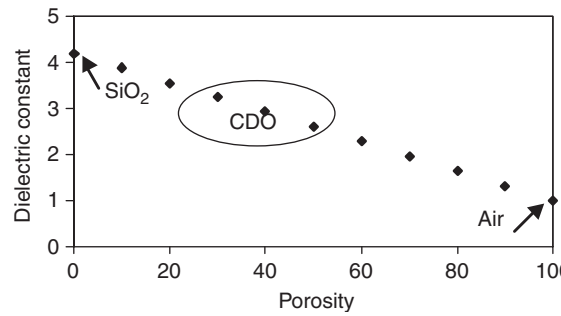


Fig. 5.10 A plot of dielectric constant as a function of porosity.

where κ_0 is the dielectric constant of SiO_2 at a value of 4.2 and P is the porosity. Since $\kappa_{air} = 1$,

$$\kappa = \kappa_0 - (\kappa_0 - 1)\, P$$

Porosity can be calculated according to the following formula: $P = 1 - D/D_0$, since D, the density of CDO film and D_0, the density of the oxide can be calculated by measuring the mass of the film using a microbalance and thickness of the film using a stylus.

A plot of κ versus P is shown in Fig. 5.10. Empirical results show that if CDO has a porosity of about 40%, the equivalent κ value should be around 2.9, which agrees with the actual measured κ value by a mercury probe.

As the device geometry continues to shrink, spacing between metal lines becomes narrower and it becomes even more critical for the dielectric material to conduct heat away from the metal lines, especially on the top metal layers. CDO materials have good thermal conductivity, allowing heat to be dissipated effectively. Since the coefficient of thermal expansion (CTE) of CDO is similar to that of copper, it will help prevent cracking and peeling due to thermal mismatch between the dielectric and copper. Some low-κ materials, such as organic spin on dielectrics, have very low thermal conductivity and high CTE, making the material difficult to

integrate into the device scheme. Figure 5.11 shows the similarities and differences between USG, CDO, and spin-on type materials.

If the CDO film is to be used on all the metal layers throughout the device, the mechanical strength of the film has to be able to withstand cracking resistance tests, the abrasive chemical mechanical polish, and pressure from the final packaging processes. Since CDO films have a substantial amount of pores, they also have lower hardness and modulus of elasticity. However, when compared to spin-on type of materials, CDO films are as least an order of magnitude stronger. Figure 5.12 shows the comparison.

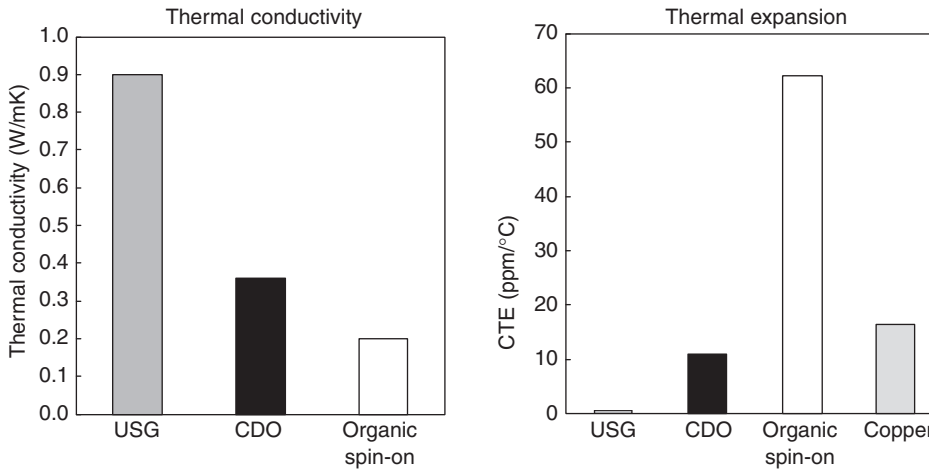


Fig. 5.11 Comparison of thermal properties between USG, CDO, and organic spin-on materials.

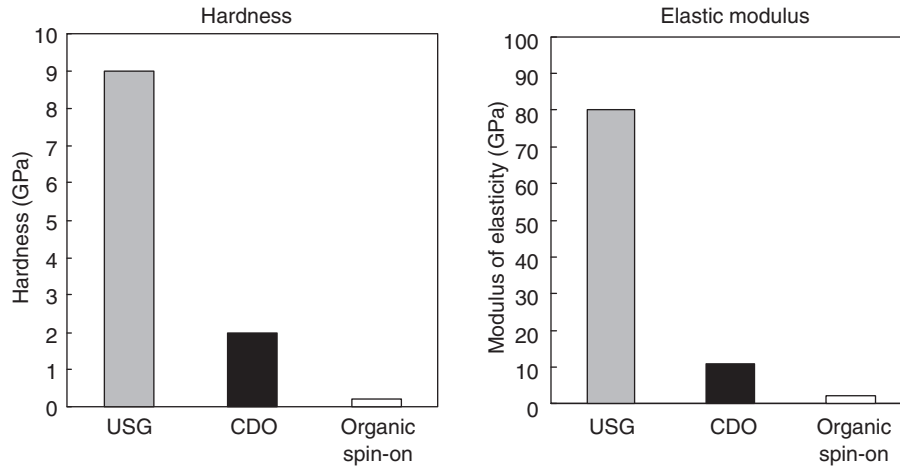


Fig. 5.12 Comparison of mechnical properties between USG, CDO, and organic spin-on materials.

5.3.2 Nitrides (SiN)

Silicon nitride films have been known for their moisture barrier properties and the high resistance to fluorine etch chemistries, compared to silicon oxides. Recently, SiN films have also been found to be excellent candidates for copper diffusion barriers and etch stop layers in dual damascene applications.

A good copper diffusion barrier should have minimal O_2 content (less than 2 at%). This is because nitride films with higher oxygen content are known to be more leaky electrically and chemically. The RI of the nitride film is a good indicator of the oxygen content in the film. The RI of a stoichiometric SiN film is around 2.0–2.1. When more oxygen is present in the film, the RI decreases since pure SiO_2 has a value of 1.46. Figure 5.13 gives the comparison of the RI versus O_2 content for a nitride film, measured by the X-ray photoelectron spectroscopy (XPS) technique. While very low RI would make a poor diffusion barrier, very high RI indicates that the film is silicon rich; and it is well known that copper can diffuse through a silicon-rich nitride film very easily.

The nitride reaction is expressed as

$$SiH_4 + NH_3 + N_2 \Rightarrow Si_xN_yH_z$$

where *x, y*, and *z* are determined by different process parameters and hardware configurations. If only N_2 or no NH_3 is used in the process, very low hydrogen content can be obtained. There are still some hydrogen in the film since SiH_4 is still a source of hydrogen. When a high NH_3/N_2 flow ratio is used, up to 25% hydrogen can be incorporated into the film.

N–H bonds are stable and hence are difficult to break. Therefore, low hydrogen content can be achieved by hardware that breaks down the ammonia molecules completely so that only a minimal amount of hydrogen is left bonded to the nitrogen atoms.

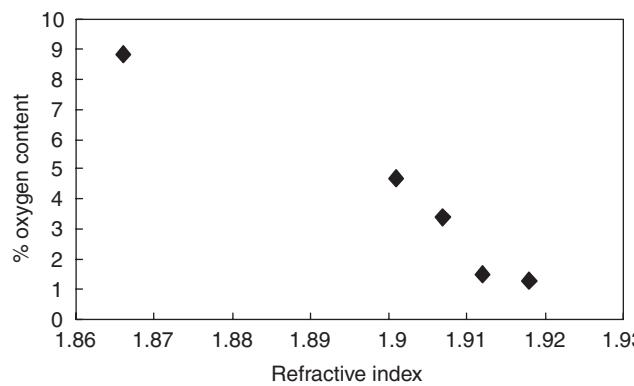


Fig. 5.13 A plot of correlation between oxygen content and refractive index of silicon nitride films.

Silicon nitride can also be deposited using HDPCVD with silane, nitrogen, and argon chemistry. The resulting film has very low hydrogen content also. However, since the cost of operating HDP is much higher than that of PECVD, HDP is not a popular method of producing silicon nitride films.

Hydrogen can be measured using techniques like nuclear reaction analysis (NRA), Rutherford backscattering spectroscopy (RBS), and hydrogen forward scattering (HFS). However, these methods are time consuming and expensive and therefore FTIR is the more economical method for measuring hydrogen content. Hydrogen is bonded to both Si and N forming Si–H and N–H bonds, respectively. N–H bonds are more stable than Si–H bonds due to the larger bond strengths, that is, 388 kJ/mol for N–H and 318 kJ/mol for Si–H. Therefore, it is undesirable to have Si–H bonds in the film since they can break loose during thermal anneal and form free hydrogen that causes problems. FTIR analysis can qualitatively measure the hydrogen content and at the same time distinguish the difference between hydrogen that is bonded to Si or N. A comparison between different nitride films with different reactor configurations and chemistries using FTIR is shown in Fig. 5.14. PE SiN A is deposited using no NH_3 and therefore has the minimum Si–H bonding whereas the other PE SiN films with high NH_3 flows have more significant Si–H bonds. HDP SiN also has very low hydrogen content.

Hydrogen content is the most important factor causing adhesion issues between SiN and FSG. Fluorine in the FSG tends to react with hydrogen in the nitride forming HF. One way to reduce the problem is to use an FSG with stable fluorine. Another way is to use a nitride film with very low hydrogen content. Of course, the best combination would be to use both.

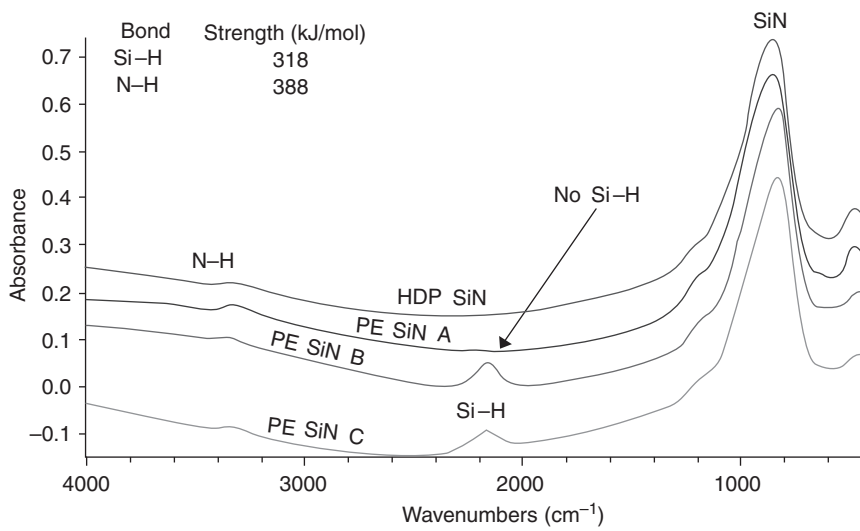


Fig. 5.14 FTIR spectra of silicon nitride films with different hydrogen content.

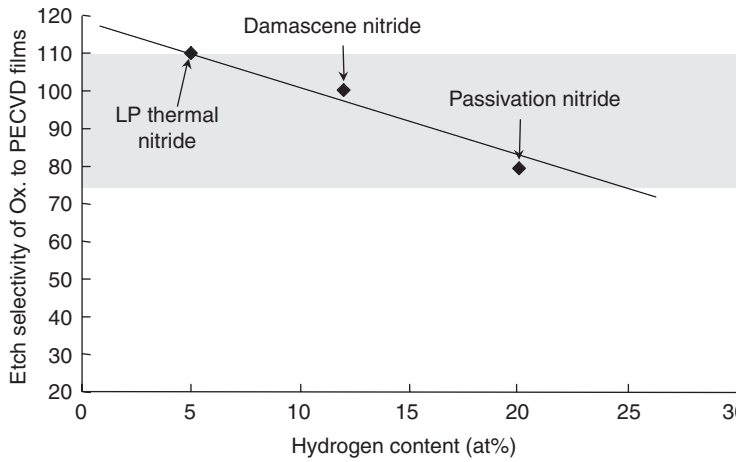


Fig. 5.15 A plot of etch selectivity as a function of hydrogen content in silicon nitride films.

Interestingly, the hydrogen content in the nitride film not only affects FSG adhesion, it also impacts the etch selectivity. Selectivity is defined as the etch rate of oxide to SiN. In order for SiN to function as a good etch stop, the selectivity has to be high. Figure 5.15 shows that films with lower hydrogen content provide higher selectivity.

5.3.3 Oxynitrides (SiON)

Antireflection coatings are used to minimize the amount of incident light that gets reflected back from the substrate. This effect is achieved by controlling the optical properties of the ARCs, namely the refractive index (n), the thickness (t), and the extinction coefficient (k). The absorption coefficient is directly proportional to k and inversely proportional to the wavelength of light. Silicon oxynitride films are commonly used for this application since the films' n and k values can be easily tuned to minimize reflections.

In addition to SiH_4 and N_2O, sometimes helium or nitrogen can be added to the reaction for various reasons. Since helium is easier to breakdown, it helps to stabilize the plasma during deposition and therefore allows tighter and more uniform control of the RI, extinction coefficient, and the thickness values. Since ARC layers are not removed after the patterning process in some integration schemes, it is critical that the film remains stable throughout all the subsequent processing steps.

By varying the SiH_4 to N_2O flow ratio, a wide range of n and k values can be achieved for 248- and 193-nm stepper wavelengths as shown in Fig. 5.16. Polysilicon is more reflective than aluminum and therefore requires a higher extinction coefficient to achieve the same minimal reflectivity. As the stepper wavelength decreases, the reflection for a given substrate increases and, therefore, a higher extinction coefficient is also needed as shown in Fig. 5.16.

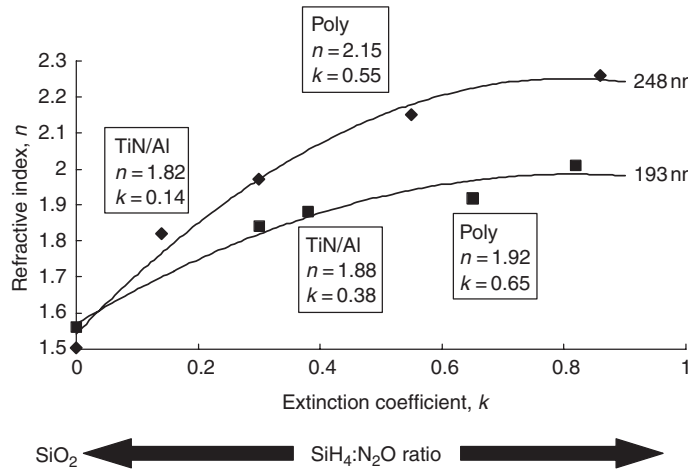


Fig. 5.16 A wide range of n and k values can be tuned by changing the SiH_4 to N_2O ratio.

Table 5.4. Effect of reactive gas flows on deposition rate, n and k values

	Deposition rate (A/min)	Refractive index (n)	Extinction coefficient (k)
SiH_4 flow ↑	↑	↑	↑
N_2O flow ↑	↓	↓	↓

At a high N_2O to SiH_4 ratio, the film composition consists of more oxygen than nitrogen and therefore results in a lower refractive index and extinction coefficient, similar to the properties of silicon dioxide. As the SiH_4 flow increases, the film becomes more silicon rich and the film properties gradually approach that of silicon, with high n and k values. The typical effects of different process parameters on deposition rate, RI, and extinction coefficients are shown in Table 5.4.

5.3.4 Silicon carbide (SiCH)

In order to use silicon carbide fo low-κ applications, the dielectric constant needs to be low and the film needs to be electrically insulating. Conventional silicon carbide (SiC) has a dielectric constant of 7 and an RI of 2.2, similar to that of silicon nitride. It is also more electrically leaky due to conduction through the silicon atoms. Since silicon atoms are larger in size than carbon, they are more electronically polarizable than carbon, more specifically, 20 times that of carbon. Therefore, the less silicon content in the film, the less polarizable the film and the lower the dielectric constant. Moreover, the less silicon content, the less conduction and therefore the more electrically insulating the film is.

Table 5.5. Comparison of mechanical properties between silicon carbide and silicon nitride

Mechanical properties	Silicon carbide (SiCH)	PECVD SiN
Dielectric constant	< 5	7–8
Refractive index	< 1.9	1.9–2.2
Stress	Compressive	Compressive
Mass density	$< 1.8\,g/cm^3$	$2.2\,g/cm^3$

The relationship between dielectric constant, κ and RI, n, is as follows: $\kappa \propto n^2$. Therefore, lowering the RI of the SiC film will lead to lower κ. By incorporating CH_3 groups into the structure, the RI and the κ value can be lowered. However, if the film is too carbon and hydrogen rich, the subsequent ashing process that uses an O_2-based chemistry would attack the carbon in the SiC film. Since the SiC film has hydrogen and sometimes, nitrogen, it is also known as SiCH and SiCN, depending on the precursors used.

Properties of SiCH are similar to that of SiN in many ways. They are both good copper diffusion and moisture barriers. They are thermally stable during subsequent temperature cycles. They possess good mechanical strength and adhere to copper well. They have compressive stress to balance out the tensile stress of the CDO films. They also have high etch selectivity to oxide films when fluorine etch chemistry is applied. Last, but not least, they also have low leakage and high breakdown voltage. On the other hand, SiC has slightly lower density and dielectric constant than SiN due to the carbon and hydrogen incorporation. The bulk density of SiCH films is much lower than that of pure silicon carbide film due to the high hydrogen content in the SiCH film. Oxygen is usually only present on the surface of the SiCH film since oxygen in the bulk film will degrade the copper barrier performance.

A comparison between SiCH and SiN is summarized in Table 5.5.

5.4 Application of silicon-based dielectrics

Silicon-based dielectrics are used throughout the IC fabrication sequence for both logic and memory devices. Figure 5.17 and 5.18 show the cross-section of a logic and DRAM device, respectively, with the various silicon-based dielectric layers and the corresponding materials used for each layers. In this section, we will describe the material requirements for each of these layers, and the common materials and processes used for depositing these device layers. The interface properties and the interactions between these dielectrics and its underlying and overlying materials is thoroughly described in Chapter 4.

5.4.1 Shallow trench isolation

Shallow trench isolation (STI) is used to isolate between two transistors. The fabrication sequence and structure is shown in Fig. 5.19.

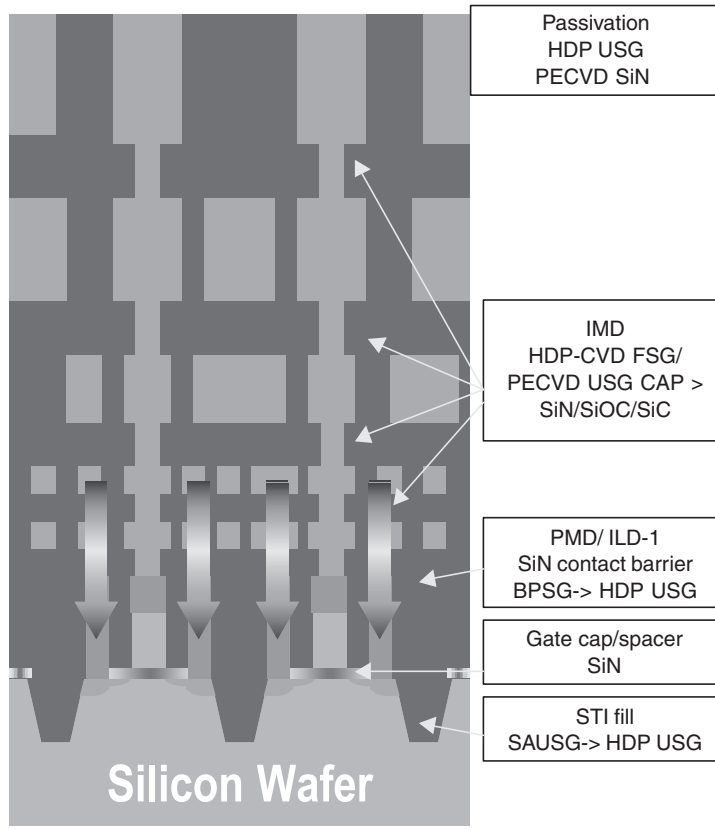


Fig. 5.17 Silicon-based dielectric layers in logic devices.

LPCVD Si_3N_4 is typically used as an etch mask for the Si trench etch and CMP stopping layer during STI formation. This is due to its better etch selectivity to Si than PECVD nitride and is less prone to erosion during CMP oxide polish.

STI also requires high aspect ratio (>5:1) gap fill, with low mobile ion and metallic contamination for low leakage current and mechanical integrity for CMP compatibility. HDPCVD is preferred due to its better gap fill capability and higher mechanical integrity than PECVD, SACVD, or LPCVD oxides.

SACVD USG films have been used but tend to have seams in the middle of the trench and, therefore, need to be annealed at high temperature to complete the fill. However, as the aspect ratio becomes higher, starting from the 0.25 μm technology node, even the high-temperature anneal is not sufficient to entirely fill the trench. HDPCVD, therefore, becomes the film of choice since the anneal step can be eliminated. However, excessive sputtering from HDPCVD can damage the corners of the trench as well as gate oxide, causing transistor leakage and low gate oxide integrity. Hence, the HDP process has to be optimized to ensure good gap fill as well as good electrical performance. Since the trench isolation step takes place before the transistor

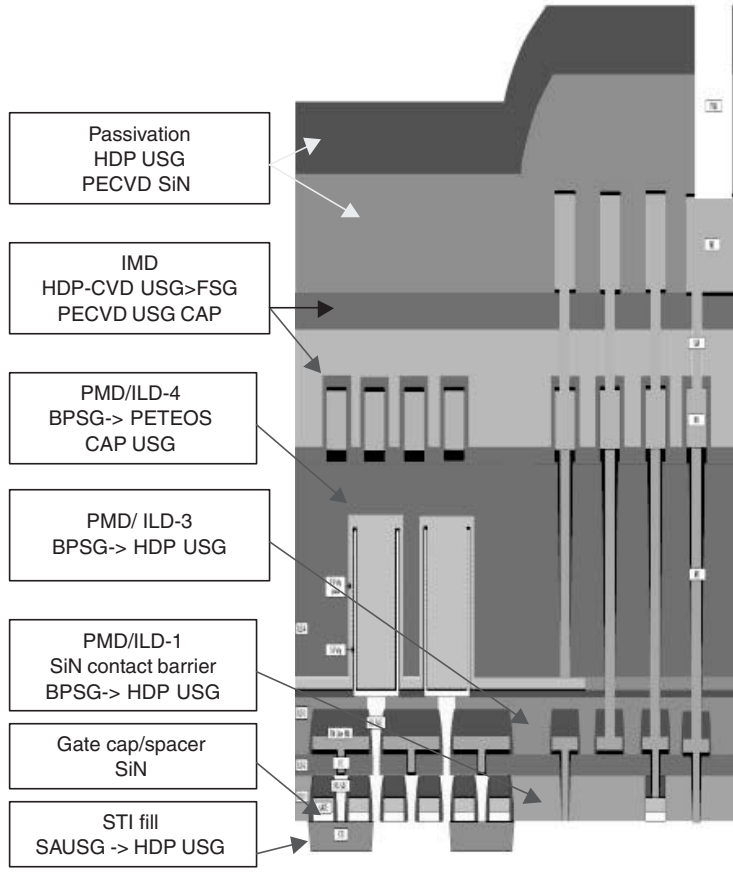


Fig. 5.18 Silicon-based dielectrics in DRAM devices.

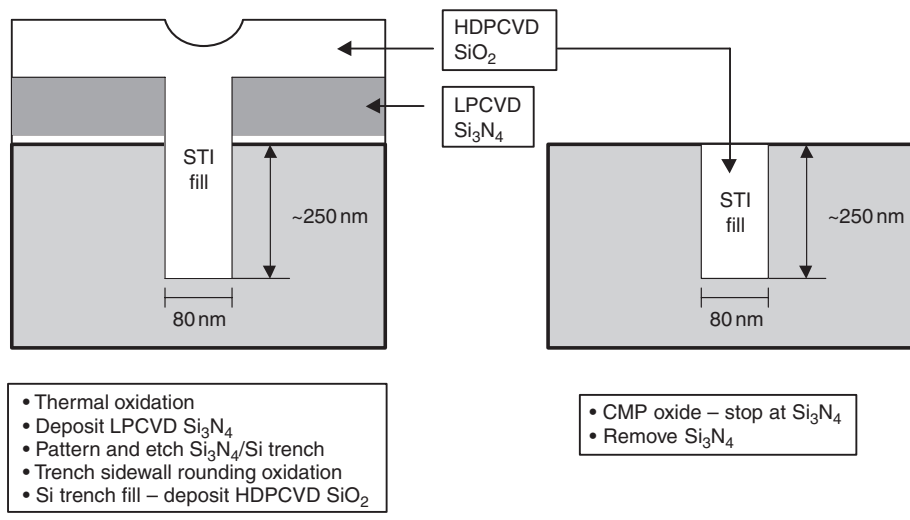


Fig. 5.19 STI formation.

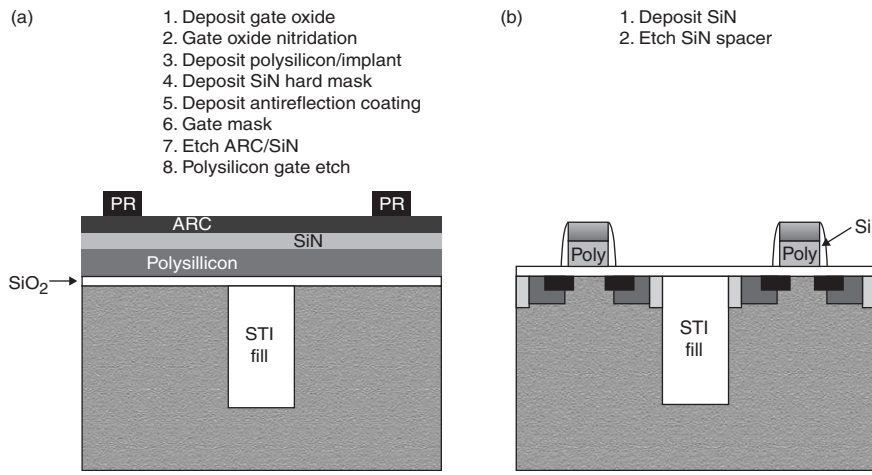


Fig. 5.20 (a) SiN as poly-etch mask. (b) SiN as sidewall spacer.

is formed, a higher-temperature (~750°C) HDPCVD process can be used to enhance gap fill of high aspect ratio structures.

5.4.2 Transistor and capacitor dielectrics

During gate transistor formation, LPCVD silicon nitride is used as an etch mask for poly-gate etch as well as sidewall spacer for salicidation and source drain implant as shown in Fig. 5.20(a) and (b).

During the trench capacitor formation of DRAM devices, LPCVD nitride and oxides are used as the etch mask for deep trench etch (7–8 μm deep), as well as in the various trench capacitor and gate transistor fabrication steps as shown in Fig. 5.21 [11].

Silicon nitride is also used as etch stop for self-aligned contact in the premetal dielectric (PMD) layer as shown in Fig. 5.22.

5.4.3 Premetal dielectric (PMD)

The dielectric layers that isolate the transistors and the capacitors from the metal interconnect layers are commonly referred to as PMD. For DRAM devices, there can be up to four PMD layers. For logic devices, there is usually only one PMD layer. It also physically protects the transistors from mobile ion contamination that might result from subsequent processing and handling.

PSG and BSG films are commonly used for PMD application. Phosphorus dopant from the PSG and BPSG is an excellent agent for gettering mobile ions like sodium and potassium.

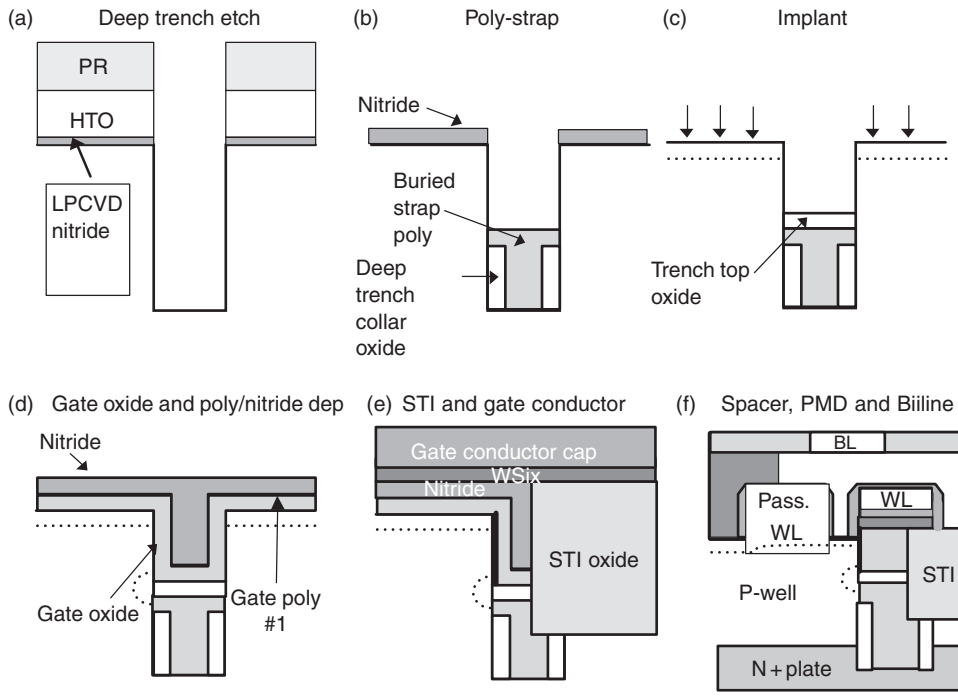


Fig. 5.21 Trench DRAM device fabrication steps.

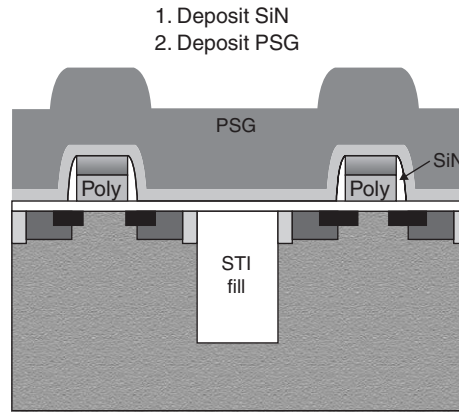


Fig. 5.22 Silicon nitride as an etch stop for pre-metal dielectric.

It prevents the mobile ions from diffusing to the active devices and degrading the electrical performance of the transistors. Boron, depending on the dopant concentration, decreases the glass reflow temperature to as low as 800°C, planarizing the topography without going to excessively high temperature.

SACVD BPSG has been the film of choice for PMD for many device nodes. However, BPSG films require high-temperature (> 800°C) anneal to flow the glass. Due to the incompatibility of the BPSG reflow temperature with titanium and cobalt silicides, which undergo phase transformations at around 600°C and increases the contact resistance, and to prevent junction dopant out diffusion, the high-temperature reflow step has to be eliminated. Therefore, HDPCVD PSG films deposited at < 550°C is gradually replacing SACVD BPSG since planarization can be achieved without the high-temperature reflow and the difficult to control boron is also eliminated since reflow is no longer needed.

5.4.4 Inter-metal dielectric (IMD)

5.4.4.1 IMD for aluminum metallization

For the 0.25-μm and above technology nodes, PECVD TEOS USG films are commonly used for IMD to fill the gap between aluminum metal lines due to the conformal step coverage characteristics. However, as the device geometry continues to shrink below 0.25 μm, the gap fill capability of TEOS USG films also runs out of steam. At that point, HDPCVD SiH_4 USG becomes the film of choice for IMD. By optimizing the D/S ratio, HDPCVD oxide films can easily fill aggressive aspect ratio structures. However, due to the high capital cost and low productivity of HDP equipment, a common scheme used today is to combine HDP and PECVD films to provide a high-productivity and low-cost solution.

In this scheme, HDPCVD is used to fill the gap just enough to cover the top of the aluminum line and then PECVD USG is used as capping layer or sacrificial layer on top of the HDP USG film. This scheme is illustrated in Fig. 5.23.

At the 0.18 μm technology node, high line-to-line capacitance of the undoped USG with $\kappa = 4.0$ becomes the limiting factor affecting the interconnect speed. Fluoro-silicate glass (FSG) with a κ value of ~3.5 provides an interim solution for reducing circuit delays. HDP FSG serves

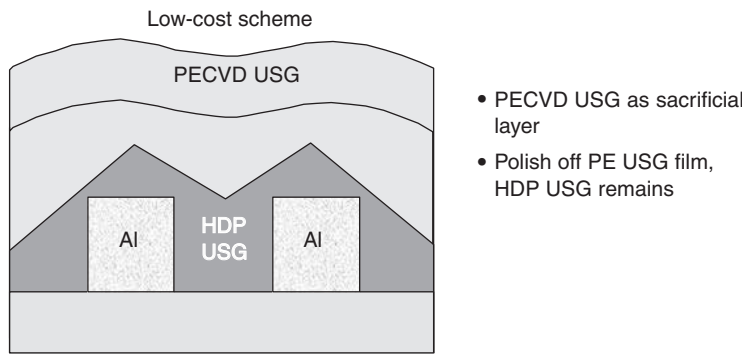


Fig. 5.23 PECVD USG as a capping layer over HDPCVD USG in the aluminum scheme.

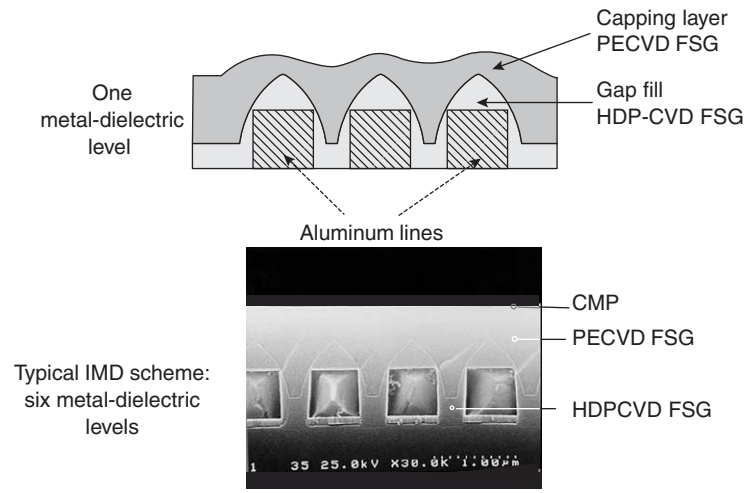


Fig. 5.24 PECVD FSG capping over HDPCVD FSG for aluminum scheme.

the purpose of gap fill as well as low κ. In order to cover the line as well as the gap, a thick layer of HDP FSG ($>1.5\,\mu m$) is needed. Since the cost of ownership of HDP films is high, it is more cost-effective to minimize the amount of HDP films deposited and then use a PECVD oxide as a cap [12]. As a result, the embedded FSG scheme, similar to the embedded USG scheme, is sometimes used (Fig. 5.24). In this scheme, only an adequate thickness of HDP FSG is used to fill the gap. Then, a very high deposition rate PECVD FSG is deposited on top of the HDP FSG as a sacrificial layer to provide enough thickness for CMP planarization. Some schemes even deposit PE USG on top of PE FSG to further lower gas cost. This way, both the gap fill and low-cost requirements are fulfilled.

Since most of the PECVD FSG is removed by CMP, it is very important that the film can withstand moisture during the CMP process. Otherwise, the film will require an extra bake out step after CMP to eliminate the moisture. Figure 5.25 shows the different FTIR Si–OH and H–O–H peaks between FSG with and without moisture absorption.

5.4.4.2 IMD for copper metallization

Since device speed is limited by the resistance of the aluminum metal lines that connect the transistors and the capacitance of the silicate glass dielectrics between them, the industry is transitioning to copper, which has lower resistance than aluminum, and to low-κ dielectrics, which have lower capacitance than USG. This switch involves many fundamental changes in the process flow. Since it is difficult to etch copper, a new approach called 'damascene' processing is used. In 'dual damascene' processing, both vias and trenches are etched and filled with copper to connect the overlying or underlying metal layers (Fig. 5.26).

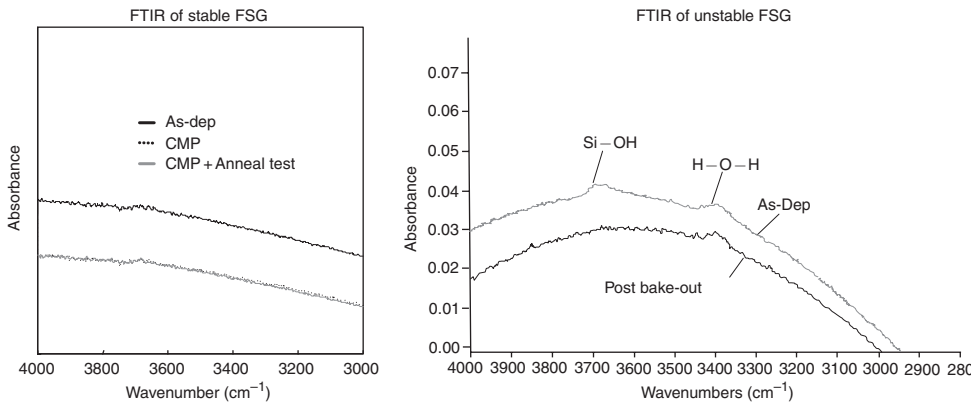


Fig. 5.25 Unstable PECVD FSG tends to absorb moisture from subsequent CMP steps.

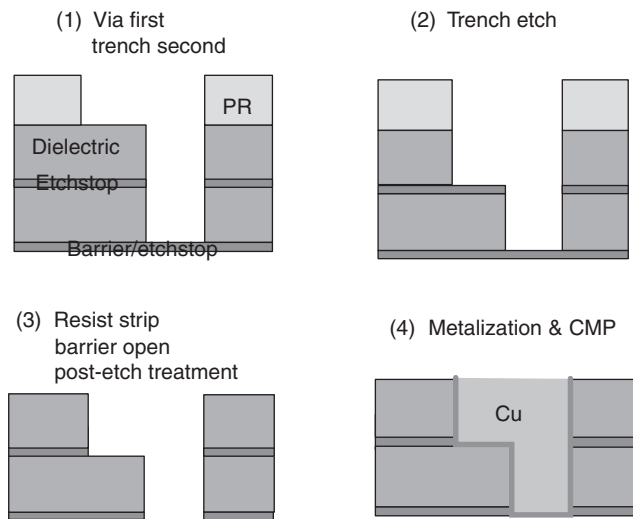


Fig. 5.26 Dual damascene scheme for copper processing.

FSG, with a κ value of 3.5–3.7, similar to that used in the aluminum scheme, has proven to be extremely effective in achieving an initial reduction in capacitance for copper dual damascene metallization. Since the properties of FSG films are largely similar to that of USG films, it can be readily adopted with the least integration risks. FSG films can be deposited either by the PECVD or HDP method. Minimal hardware modification is needed to convert a system from USG to FSG. This film, with $\kappa \sim 3.5$, is widely accepted by the industry and is being implemented as the first-generation low-κ dielectric.

Barth *et al.* [13] reported blistering problems while integrating SiH_4 FSG and SiN if the SiF_4 to SiH_4 flow ratio is not optimized. Wistrom *et al.* [14] compared the film properties and

integration of H–DP FSG, PE SiH_4 FSG, and PE TEOS FSG, and found that TEOS FSG appeared to be superior to PE SiH_4 FSG by a wide margin in several tests: stress stability ($20\times$ difference), dielectric constant (κ of SiH_4 FSG is similar to USG), blistering on as-deposited and annealed films, wet etch rate, F diffusion ($>4\times$ difference), breakdown voltage and leakage (three orders of magnitude difference). The comparison data show that a more stable FSG can be easily integrated into copper damascene schemes.

CDO is becoming the low-κ dielectric film of choice for copper dual damascene applications at the 100-nm technology node and beyond because it offers even lower κ value than FSG ($\kappa \sim 2.2$–3.0).

During the course of fabricating a device, the CDO films would go through at least 10–15 thermal cycles at about 400–425°C. CDO films and copper have similar coefficient of thermal expansion (CTE), creating less stress from thermal mismatch between metal and dielectric. This kind of stress could lead to film delamination if the adhesion between the dielectric and the metal is poor. CDO films also have high thermal conductivity, allowing heat generated from joule heating in metal lines to be removed efficiently. Lastly, mechanical strength of CDO films, that is, hardness or Young's modulus is sufficiently high to withstand all subsequent processing steps, especially during CMP processing since the film is exposed to harsh abrasive polish environment.

Although CDO films are constantly exposed to etch chemistry, post-etch photoresist removal, or ashing and solvent clean, they do not change properties after these integration steps. FTIR spectra of the CDO films show no change on the Si–CH_3, Si–H, C–H, and Si–OH peaks, before and after integration. Also, minimal change in dielectric constant after integration is found. Figure 5.27 shows the performance of a stable CDO film from FTIR analysis.

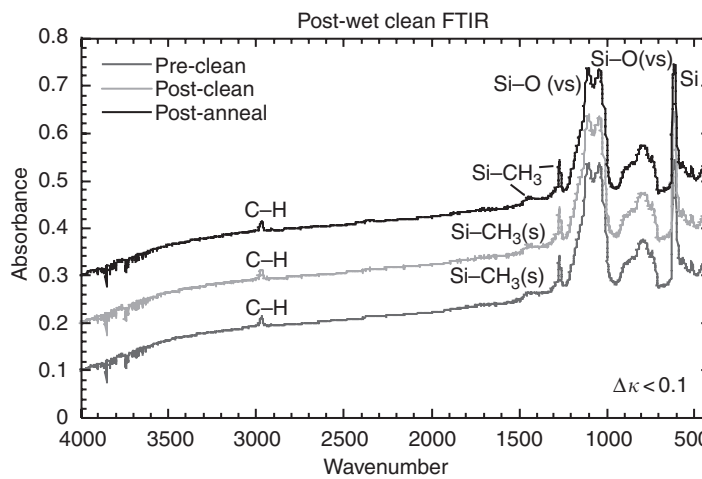


Fig. 5.27 CDO films show no change in FTIR spectra after integration.

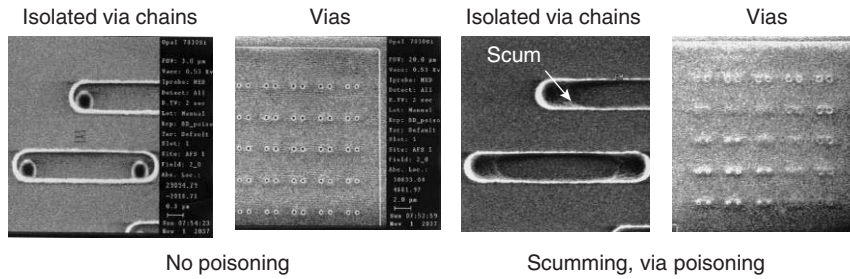


Fig. 5.28 Examples of with and without via poisoning.

Another potential problem experienced during integration of CDO is via posioning. If there are N–H bonds in the barrier/etchstop layer, during the trench lithography step, photoresist could react with the N–H species and create scumming and mushrooming in the trenches and the vias. Figure 5.28 shows the difference between with and without poisoning.

5.4.5 Passivation

The passivation layer serves to isolate the silicon devices from moisture absorption as well as metal ion diffusion resulting from soldering and other device packaging steps. PECVD nitride and oxides have been used for this application and will continue to be used, although HDPCVD may gain acceptance as device shrinks and step coverage becomes an issue.

5.4.6 Other applications

5.4.6.1 Hardmask for copper dual damascene process

USG has been used as part of the multi-layer hardmask scheme over a spin-on type low-κ dielectric in the dual damascene application. The dual hardmask scheme typically consists of a thin low-κ copper diffusion and moisture barrier such as SiCH or SiN, followed by USG. Then photoresist is applied and developed over the USG hardmask layer, preparing the stack for via and trench etching. There are many advantages of using USG as the top hardmask layer. First, USG is inert to resist interaction, therefore preventing resist footing issue. Second, the chemical mechanical polish characteristics of USG are well understood, allowing the CMP process to stop at the SiCH or SiN interface precisely.

5.4.6.2 Etch stops and copper diffusion barrier for dual damascene process

Since copper readily diffuses into silicon oxide even at room temperature, an effective dielectric barrier for copper damascene integration scheme is required. Critical properties for such

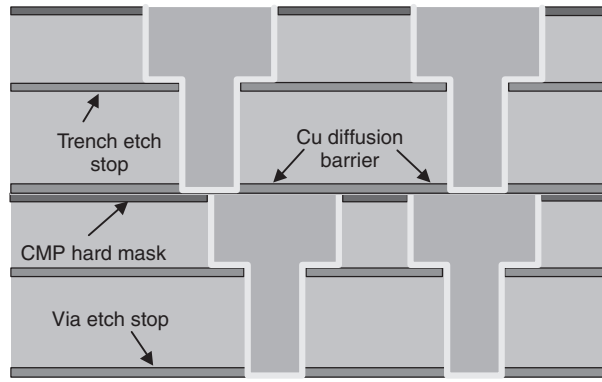


Fig. 5.29 Different applications for silicon nitride and silicon carbide.

a barrier are: good barrier performance with very short diffusion length of copper in the barrier, high etch selectivity with respect to oxide and low-κ dielectric films, low leakage and high dielectric breakdown voltage, strong adhesion to copper, oxide, and other low-κ dielectrics. In addition, the barrier film must be deposited at temperatures compatible with interconnect integration schemes.

Copper tends to oxidize when it comes in contact with air and forms native copper oxide. The presence of native copper oxide could lead to several integration problems. First, copper oxide causes poor adhesion at the copper/silicon nitride interface as well as the copper/tantalum nitride interface leading to peeling problems. Second, copper oxide degrades electromigration lifetimes. Third, copper oxide increases via resistance and eventually increases RC delay. Therefore, removal of the native oxide on a copper surface is a critical step in the damascene processing of copper-based interconnects. Unfortunately, there is no good way to determine when to terminate the NH_3 plasma during CuO removal. The only accurate way of measuring residual oxygen at the interface is by XPS.

Silicon nitride has been widely used in microelectronic device fabrication for years. The applications include final passivation layer, diffusion barriers, against mobile ions, moisture barriers, and etchstop layers for pre-metal dielectric. Recently, silicon nitride film applications have been extended to advanced dual damascene processing, such as copper diffusion barrier, etchstop, and CMP stop layers due to the film's excellent barrier properties against copper and moisture and the high etch selectivity to low-κ dielectric films. Figure 5.29 shows the different applications of SiN and SiC in the dual damascene copper process.

It is very important that silicon nitride is deposited on the copper immediately after the CuO is removed without breaking vacuum because once the copper is exposed to atmosphere, CuO will regrow right away. This process sequence is called *in situ* copper oxide removal. The oxygen concentration at the interface using the *ex situ* CuO removal method could be an order of magnitude higher than that of the *in situ* case.

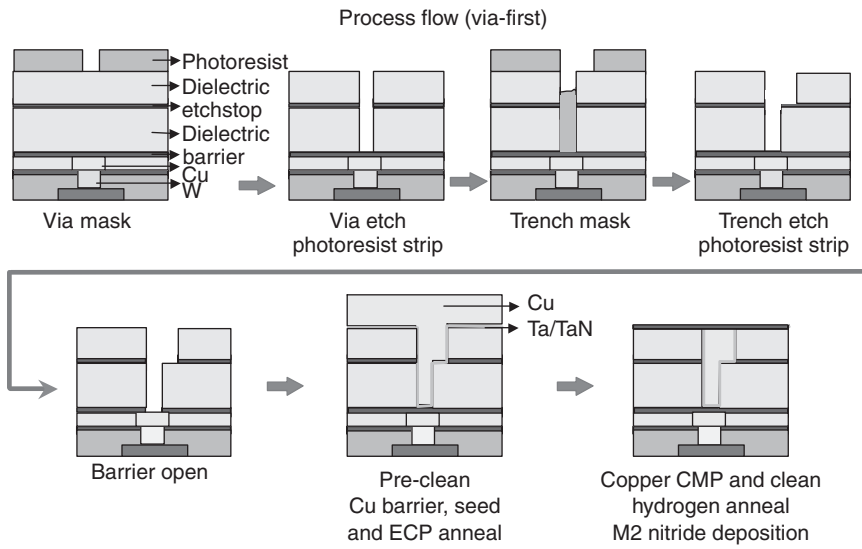


Fig. 5.30 Via-first dual damascene scheme.

The most common dual damascene etch scheme is called via-first and the scheme is shown in Fig. 5.30. After lithography is performed, the via is etched through the two layers of dielectric, without punching through the bottom nitride layer. Then the trench is patterned and etched through the top layer of dielectric, stopping at the first nitride layer. Without the high selectivity between the bulk dielectric and the etch stop, etch systems would need a tight control of etch uniformity to ensure that all the trenches are of the same depth across the wafer and from wafer to wafer. If there is no etch stop, the trench etch would have to be done based on time. Variations in the dielectric thickness would lead to differences in resulting trench depth and punch through of the bottom via.

Silicon carbide can also be used for copper diffusion and moisture barrier, etch stop for trench and via, CMP cap and hard mask layer with copper dual damascene applications.

SiCH has a lower dielectric constant than conventional SiN, and is also a good copper barrier, similar to SiN. Since SiCH is thermally and chemically stable, it can be used as a capping layer or moisture barrier over the more hydrophilic CDO films to protect the CDO films from absorbing moisture from subsequent chemical processing steps such as CMP.

Since SiCH etches slower than oxide-type materials and, therefore, exhibits high selectivity, it is also used as an etch stop layer. When used as the via etch stop in the dual damascene scheme, the high selectivity of SiCH widens the dielectric etch process window and prevents undesirable punch through to the copper underneath the dielectric. When used as the trench etch stop, it allows the trench dielectric etch to stop at the bottom of the trench; therefore, controlling the trench depth more precisely.

SiCH is also used as a CMP stop for several reasons. First, copper CMP has high selectivity to SiCH and therefore can stop easily when the SiCH layer is reached. Second, SiCH adheres to and protects the underlying low-κ material well and, therefore, allows the low-κ layer to stay intact after the aggressive CMP process.

If 248-nm lithography is used, SiCN films do not pose severe resist poisoning issues but at the same time offer greater hardness and better compatibility to the subsequent etching and ashing processes. However, when 193-nm lithography is used, nitrogen in the SiC film will lead to severe resist poisoning issues and, therefore, must be eliminated from the film. Resist poisoning is caused by N–H species reacting with photoresist in the dual damascene scheme.

5.4.6.3 Antireflection coatings

Silicon oxnitride is mainly used as an ARC during photolithography because of its ability to absorb light.

Photolithography is the process of printing images of the circuit pattern onto a wafer. This is usually accomplished by exposing a photosensitive layer called photoresist through a mask to transfer the image onto a wafer. When the underlying film is highly reflective, light reflected from the substrate surface and the photoresist surface tends to interfere with the incident light from the exposure source through the mask and cause unwanted reflections (Fig. 5.31) leading to linewidth variations, also known as critical dimension (CD) swing [15].

As the device features shrink, CD control becomes even more critical. Shrinking device features require lower exposure wavelengths, which, in turn, lead to increasing amount of substrate reflection, causing larger CD swing. Conventional ARC layers, such as spin-on polymers, have been used to suppress unwanted reflections by utilizing the absorption properties of the film. However, due to the self-planarizing nature of spin-on films, an organic ARC film has thickness variations over topology and, therefore, results in different absorptivity through the

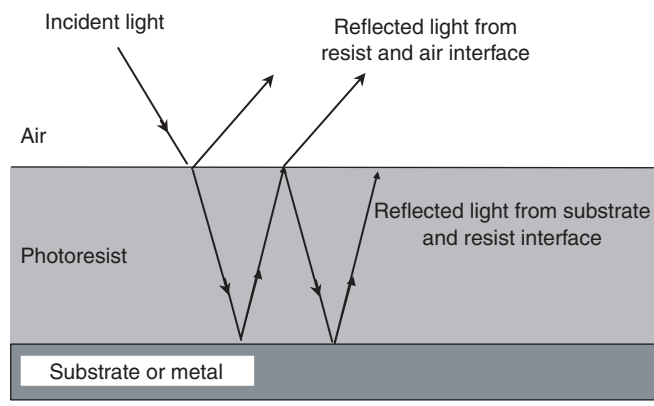
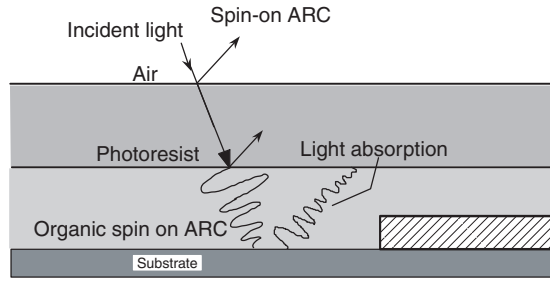


Fig. 5.31 Reflected light from substrate surface interferes with incident light.

layer. This would require the film thickness to be optimized for the thinnest layer to totally absorb light, which may result in a substantially thicker film over topography and would have to be optimized for different circuit patterns. The thickness variations in the polymer ARC would cause etching problems since there is minimum etch selectivity between organic photoresist and the organic ARC film.

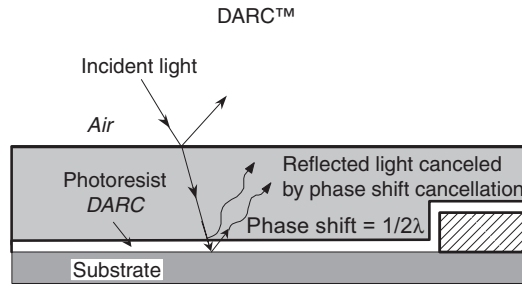
Organic ARCs reduce light reflections by absorbing the reflections (Fig. 5.32). Therefore, starting at 0.35-μm device geometry, a dielectric ARC (DARC) film is used. DARC works by using phase-shift cancellation (Fig. 5.33).

When the reflections from the substrate and that from the ARC surface are 180° out of phase with each other, the reflections will cancel each other by destructive interference. A phase



ARC mechanism	Absorption
Deposition profile	Planar
ARC thickness	~2000 Å
Reflectivity	>3%

Fig. 5.32 Organic spin-on ARC works by absorption.



DARC mechanism	Phase-shift cancellation
Deposition profile	Conformal
ARC thickness	300 Å
Reflectivity	<1%

Fig. 5.33 Dielectric ARC works by phase-shift cancellation.

shift of half a wavelength for the wave passing through the DARC can be achieved by optimizing the thickness (t) and the RI (n) of the DARC. By optimizing the optical properties of the DARC film, the reflections can be minimized.

DARC is typically a thin conformal SiON film deposited by the PECVD method. SiON films are chosen for ARC applications for several reasons. First, SiON films have the suitable range of optical properties for ARCs. Second, the stoichiometry of the plasma-deposited SiON films can be tuned to provide the specific n and k values required for the specific exposure wavelength by modifying the ratio of reactive gases used for deposition. Third, SiON films have been widely used in the semiconductor industry for years and are familiar to users in terms of properties, metrology, and integration characteristics. Last but not least, only a thin layer, of the order of 300 Å of SiON, is needed since SiON is conformal over topography. This provides a significant advantage over an organic ARC film since it enables uniform etching as well as better etch selectivity to the organic resist layer due to their differing etch chemistry. As feature size decreases, conformality and etch selectivity of the ARC layer becomes even more important due to thinner resists.

One of the phenomena observed with ARC material is the presence of 'footing' (Fig. 5.34). Footing is a result of the amine groups (NH_2) on the surface of the ARC film reacting chemically with the photoresist. Deep UV resists are especially sensitive to footing. The interaction between N–H radicals and resist results in a 'foot' after resist development, causing loss of critical dimension control. Both titanium nitride (TiN) and SiON ARCs are known to cause footing problems. One way to prevent this interaction is to deposit a thin layer of oxide on top of the SiON before the photoresist is applied. The oxide serves as an inert barrier between SiON

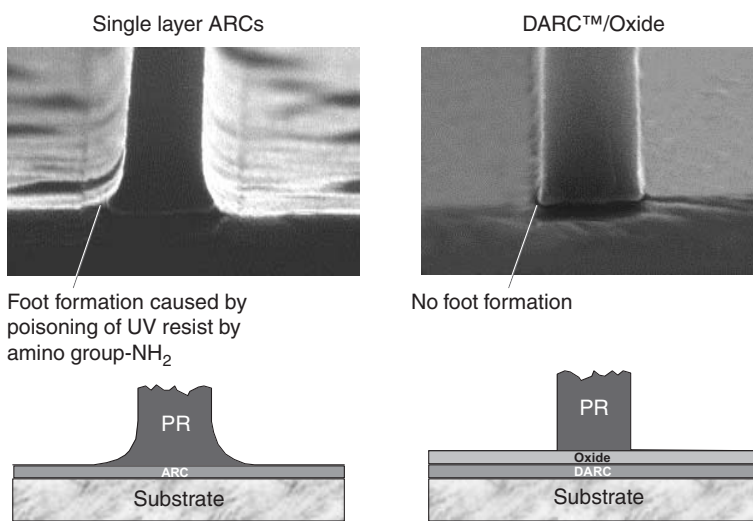


Fig. 5.34 Footing results from interaction between the amine groups in the ARC film and photoresist.

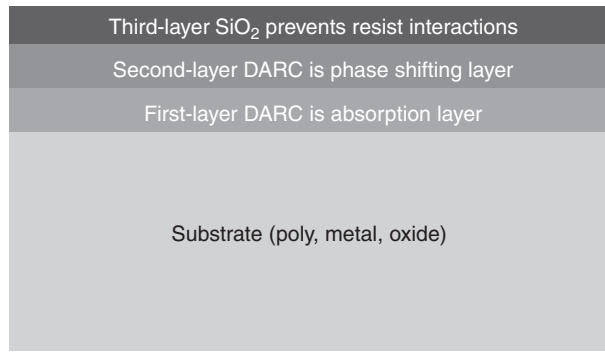


Fig. 5.35 Multi-layer ARC scheme is used to minimize reflected light and footing issue.

and resist but does not affect the optical properties of SiON. This thin oxide can be achieved by utilizing a high N_2O to SiH_4 ratio as mentioned earlier. Another way to avoid the interaction is to use an oxygen or N_2O plasma treatment after SiON deposition to effectively remove the NH groups from the surface. Both the oxide cap and the oxygen treatment can be performed *in situ*, that is, after the SiON deposition in the same chamber to prevent footing in just a simple and efficient step.

As the lithography requirements get more and more stringent, even the least amount of reflected light is not acceptable. A multilayer DARC scheme is designed to address this requirement. The first-layer DARC absorbs most of the light, the second layer of DARC uses the phase shift property to cancel out any remaining light and the last or top layer is a very thin silicon oxide film that prevents resist poisoning. The multilayer scheme is shown in Fig. 5.35.

5.5 Summary

The deposition techniques, material and film properties, as well as the applications of silicon-based dielectrics have been described. These include undoped and doped silicon oxide, silicon nitride, silicon oxynitride, and silicon carbide. Both thermal- and plasma-assisted CVD techniques have been used in the industry to deposit these films, with the resultant film properties, and their consequent applications in the semiconductor fabrication process. As discussed above, silicon-based dielectrics will continue to be the material of choice for fabricating silicon devices, albeit with new dopants (i.e. carbon) and their resultant material properties, due to its compatibility with silicon substrate as well as the industry familiarity with these materials.

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Chapter 6
Low-κ polymers

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Abstract

The need for an interlayer dielectric (ILD) material, with a dielectric constant lower than that of the silicon dioxide and preferably in the range of 1.5–2.5, has led to considerable efforts in looking at a variety of already known polymers and those being synthesized especially for this application. In this chapter we briefly examine polymer chemistry related variations in the monomers and in their polymerized products. The chapter also attempts to review the status of the polymer-ILD related works and knowledge, with special emphasis on the role of the structure and its stability, preparation methods, interactions with the surrounding materials during preparation of the device/circuit structures and under actual use conditions, and adhesion of such polymers on a metal film and of a metal film on the given polymer. It is apparent the task of synthesizing an ideal or at least a working polymer for ILD application is not simple because of the basic characteristic differences between the polymers and the material like silicon dioxide which has been the ideal, but with higher dielectric constant, as an ILD material.

6.1 Introduction

As discussed in earlier chapters integrated circuit-feature dimensions will continue to shrink until about 0.03 μm minimum feature size is reached sometime by 2010 [1]. Accordingly, due to required lowering of the *RC* delay (see Chapter 1) there is a strong need of not only the clever circuit and especially interconnect layouts (designs) but also of new materials that can effectively lower the interconnect resistance *R* and the interlayer dieletric (ILD) capacitance. Copper interconnects ($\rho = 1.7$–$2.2\,\mu\Omega\,\text{cm}$) have effectively replaced aluminum alloy ($\rho \approx 3.5$–$4.5\,\mu\Omega\,\text{cm}$) interconnects.

Now there is an effort to replace SiO_2 (dielectric constant $\kappa = 3.9$–4.1) with a low-κ ($\kappa \approx$ 1.5–3.0) ILD. Recently a low-κ material called SILK™ [2] with a $\kappa \approx 2.7$ has been introduced as an ILD to be in use with Cu-interconnects [3]. Lowering the κ value to as low as possible is essential. The need of low-κ has focused attention to polymers, fluorinated and carbonaceous inorganic, and porous materials.

Physics and materials science considerations clearly suggest that the insulating materials made up of lower atomic number species generally have low κ. Harrop and Campbell [4] have plotted permittivity as a function of the atomic number, in case of the elemental insulators like C, Si, or Ge, or the mean atomic number of the constituents that make ionic halides and oxides. It is clearly seen from these plots that lower atomic numbered atoms have and produce lower polarization and thus the lower permittivities or dieletric constants. Also the single bonds (σ-electrons) in polymers have lower polarizabilities than the double and triple bonds (π-electrons). In addition, materials with larger molar volumes are expected to have lower κ. Such considerations naturally then lead to a search for lower κ materials that may or may not contain fluorine and/or voids, since voids offer a lowest κ. Our goal in this chapter is to look at polymers as low-κ ILD material. As discussed in Chapter 2, the final applicability of such materials or ILD will depend on their having the needed properties, processability, and reliability both during processing and during actual-use-life-time. Similarly, the properties and requirements as listed in Chapter 2 may vary from application to application, for example: (a) use with copper or aluminum as interconnect; (b) the breakdown fields that will decrease as we move closer to below 100 nm gates; and (c) the thickness that may vary from one type of application to another thus affecting not only the electric breakdown field requirements but also the requirements on the thermal coefficient of expansion and Young's modulus of the polymer ILD. We may thus move into having different options for different applications.

Since the 1980s a large group of researchers have examined a large number of newly synthesized or existing polymers for their use as an ILD on a chip, using Al or Cu as the interconnect metal. Polymers of all types have been synthesized and examined for both on- and off-chip (packaging) applications. This chapter reviews such efforts with an emphasis on the applicability of such polymers.

6.2 Structure and properties

Chapter 2 has defined the qualifying properties of the polymers for ILD applications. The properties were grouped as electrical, mechanical, chemical and electrochemical, and thermal and thermodynamic. In addition the processability (e.g. deposition and formation, etching, gap-fill, planarization, and annealings) and final reliability are essential. Of course, the primary (and the first) consideration is the dielectric constant, which is desired to be in the range of 1–4, lower the better. In Chapter 2 many of these properties have been discussed. In here, we focus on the relationships between the chemical structure, types of polymerization, and the observed properties of the polymers. In this context, other properties, discussed in Chapter 2, will be touched upon very briefly as and when necessary.

Polymers are long chain macromolecules with repeating monomer. The chemical properties of polymer are determined mainly by three factors: the chemical structure of the monomer, the spatial arrangement of the monomers that determine the packing density of the polymer chains

(made of n monomers), and the molecular weight of the polymer (equal to the monomer molecular weight times the degree of polymerization). Note that as the monomers link together during polymerization; the macromolecules may align parallel to the substrate, leading to anisotropic properties. Cross-linking between polymer chains provides higher rigidity and often reduces anisotropy. Thus, the above mentioned packing density is not only related to the number of chains per unit volume but also to their spatial arrangements (e.g. cross-linking).

When a single monomer is used to form the polymer, the polymers are called homopolymers. On the other hand, polymers formed using two or more monomers are called copolymers. The simplest examples of monomers leading to homopolymers are [5]: vinylidene chloride $CH_2{=}{=}CCl_2$, leading to a polymer called poly(vinylidene chloride) or PVDC with a formula $(–CH_2–CCl_2–)_n$, and ethylene $CH_2{=}{=}CH_2$, leading to the polymer polyethylene with a formula $(–CH_2–CH_2–)_n$. Similarly one of the simplest copolymer is ethylene-*co*-vinyl acetate, ECVA made of two monomers, ethylene and vinyl acetate, $CH_2{=}{=}CH(OCOCH_3)$. The molecular weight of these polymers depends on the degree of polymerization, n, as defined later. The effect of monomer structures can be illustrated by the structurally similar polymers, which have different properties. These two polymers are PVDF [poly(vinylidene fluoride)]and PTFE [poly(tetrafluoroethene) or Teflon], whose chemical structures are depicted in Fig. 6.1. The difference between the monomers is in that the two hydrogen atoms in PVDF are substituted for two fluorine atoms in PTFE, resulting in two polymers with widely different properties. For example, while PTFE is not soluble in organic solvents, PVDF is soluble in a polar solvent. A similar effect can be achieved by the spatial rearrangement of the monomers [5, 6].

Note that the polymerization of a pure monomer does not guarantee a well defined polymer with regularly arranged structure. Thus, the polymerization process can cause the complexities in structure leading to different polymers starting from the same monomer. These variations in polymerization are associated with the branching and also with the asymmetric structure of the monomer and associated isomerisms, for example, sequence isomerism, stereoisomerism, and structural isomerism. Sequence isomerism causes a variation in monomer-to-monomer linkage (leading to polymerization) such as head-to-head, head-to-tail, and tail-to-tail as shown in Fig. 6.2(a) [5].

Stereoisomerisms arises because the substituent X placed on each carbon atom, for example, in $CH_2{=}{=}CHX$, has two possible arrangements relative to the chain and the next X group on the chain [5]. Figure 6.2(b) shows two arrangements called racemic (each X group is on the opposite side of the stretched chain) and meso (each X group is the same side of the chain).

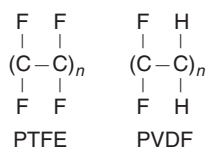


Fig. 6.1 Chemical (monomer) structure of PTFE and PVDF.

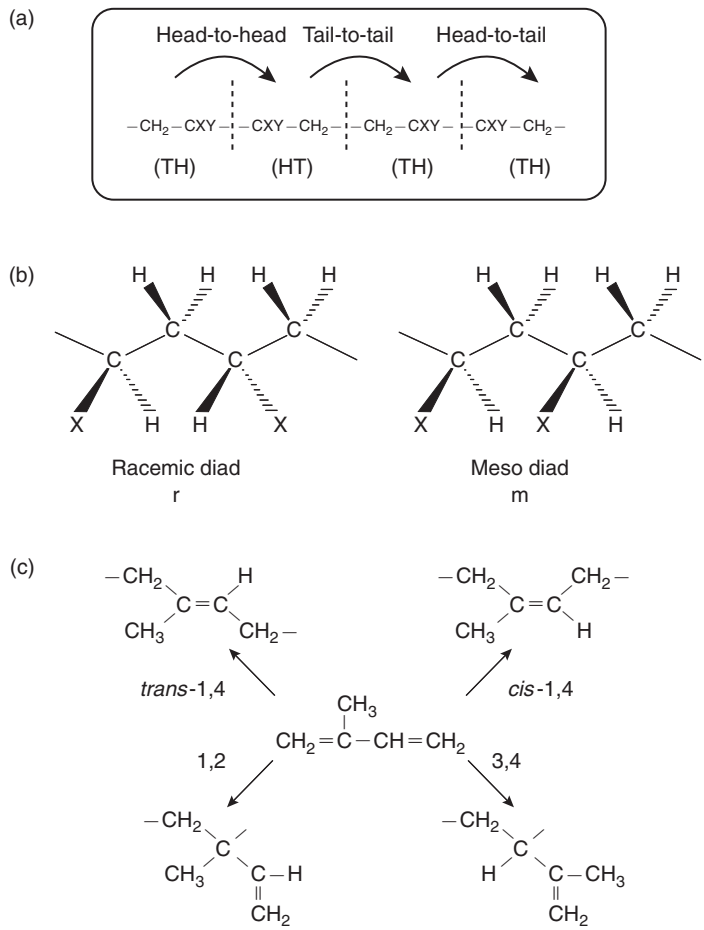


Fig. 6.2 (a) Shows head-to-head, tail-to-tail, and head-to-tail linkages in the same polymer, from the $CH_2{=}CXY$ monomer. Same monomer may lead to all one type of linkages or a mixed one such as one shown here; (b) schematic diagram showing stereoisomerism in a diad (two $CH_2{=}CHX$ monomer unit) polymer; and (c) four structural isomers of isoprene ($CH_2{=}C\ (CH_3){-}CH{=}CH_2$) [5] (reprinted with permission).

When using two or more monomers to form copolymers much more complex situations arise leading to different polymers with different properties. Copolymers can be made in a variety of ways and therefore, have been defined as block copolymers, graft copolymers, and blended polymers [5]. Block copolymer-unit-monomer is made of two or more units of individual monomers. In graft copolymers one monomer is grafted on the backbone of the chain of the second monomer leading to the grafted-copolymer-unit-monomer. Alternating copolymer units are simply alternating monomers of the two types linked together in a random fashion – generally

many at a time. In another category, the monomers are simply mixed together – they do not couple with each other but blends are polymerized. Blending may be miscible or immiscible but the end product can have better properties than individual single monomer polymers.

These variations in the properties of polymers (either homo- or copolymers) resulting from a polymerization process are the cause of a concern in producing reliable polymer dielectric (ILD) films exhibiting identical properties along the wafer surface (i.e. chip to chip) and from wafer to wafer.

When a polymer chain is added to the side of the other polymer chain (e.g. by replacing one of the side atoms), a branched polymer is produced. Occurrences of such branched structures reduce the packing density of linear polymer and this affects mechanical properties and thermally induced glass transition temperatures, T_g (see Chapter 2). Crystallinity, discussed later, is also affected: linear polymers can crystallize with high packing density whereas branched polymers may produce lower level of crystallinity – higher the branching lower is the crystallinity.

Note that by replacing the hydrogen with larger side groups one can generate asymmetry in the polymer chains. This then leads to a lower tendency of sliding past each other and higher tendency to form bonds across the chain-length and, therefore, to improved rigidity and melting point.

Polymer chains may chemically link to each other to produce a three-dimensional network of these chains. This is generally achieved by using long chain polymers with reactive groups, which cause cross-linking during the curing process. Cross-linking provides increased stiffness, allowing them to sustain heavier loads prior to switching from elastic to plastic deformation. Heavily cross-linked polymers usually, therefore, have high glass transition temperatures and good mechanical yield strengths, and are generally brittle [7]. For relatively higher temperature application, cross-linking is favored. Based only on the extent and type of the cross-linking, the polymers have been defined as thermoplastic polymers, thermosetting polymers, and elastomers. Thermoplastics have flexible linear chains with non or very little cross-linking or branching. They thus flow easily, can be reheated, and shaped easily. Naturally, they have the lowest T_g values. Examples of thermoplastic polymers are polyethylene, polystyrene, and nylons.

Thermosetting polymers are heavily cross-linked, can flow, and easily shaped when initially constituted and cured. They have high T_g values and cannot be reshaped or reheated. Examples of thermosetting polymers are epoxies, polyurethane, parylenes, polyimide siloxanes, polyimides and copolyimides, benzocyclobutene (BCB), SILK™ [8] fluorinated poly (aryl ethers) FLARE™ [9], polyaryl ethers, a variety of silsesquioxanes, and perfluorocyclobutane. For ILD applications thermosetting polymers are preferred.

Elastomers are somewhere in between the above two types and generally are cross-linked linear chain polymers. Isoprene (natural rubber), neoprene, silicones, and viton are examples of elastomers.

Many properties of the polymers are linked to so-called degree of polymerization, n, and the molecular weight. The degree of polymerization is given as

$$n = \frac{\text{Molecular weight of the polymer}}{\text{Molecular weight of the monomer or the repeat unit}}.$$

Generally, the size of the polymer chain varies leading to a mixture of molecular weights. Thus, a polymer is made of polymer chains with a variety of n and molecular weights. One then defines an average (by weight or by number, that is, degree of polymerization) molecular weight given as [5]:

$$\text{weight average molecular weight} = \overline{M}_{\text{w}} = \frac{\sum N_x M_x^2}{\sum N_x M_x}$$

or

$$\overline{M}_{\text{w}} = \frac{\sum W_x M_x}{\sum W_x}$$

and

$$\text{number average molecular weight} = \overline{M}_{\text{N}} = \frac{\sum N_x M_x}{\sum N_x},$$

where M_x is the molecular weight of a polymer molecule with a degree of polymerization x, N_x is the total number of molecules with molecular weight M_x, and W_x is the weight of all such molecules. In actual practice the degree of polymerization is obtained using one of these average molecular weights. One also defines a ratio of $\overline{M}_{\text{w}}$ and $\overline{M}_{\text{N}}$ as polydispersity of the polymer, as a measure of the breadth of molecular weight distribution. In a preparation of a polymer films it is important that these average molecular weights are reproduced on the sample, and sample to sample. Also note that the melting point and rigidity of the polymers, in general, increase with increasing molecular weight and n. There are some other generalized observations/expectations on the influence of: (a) intermolecular forces; (b) presence of polar functional groups and of bulky groups, like benzene, on the backbone or in the side chain of the polymer; (c) the diluents used to prepare monomers/polymers and; (d) copolymerization, on the melting point and glass transition temperature of the polymer. Strong intermolecular forces enhance the melting point. Similarly, presence of polar functional groups and/or bulky groups increase the melting point. Presence of the diluents in the polymer lowers the melting point. The effect of copolymerization could go either way depending on the complexity of the structure of the final polymer. These influences are clearly demonstrated when one compares the melting points (65, 135, 265, and 400°C) of poly(ethylene oxide), polyethylene, nylon, and poly (*p*-xylene), respectively.

Crystallization of some polymers can occur although a completely crystallized polymer, free of defects, is rarely seen. Crystallization generally brings a long-range (diffused) order and strongly depends on preparations. For crystallization to occur: (a) homopolymers must have

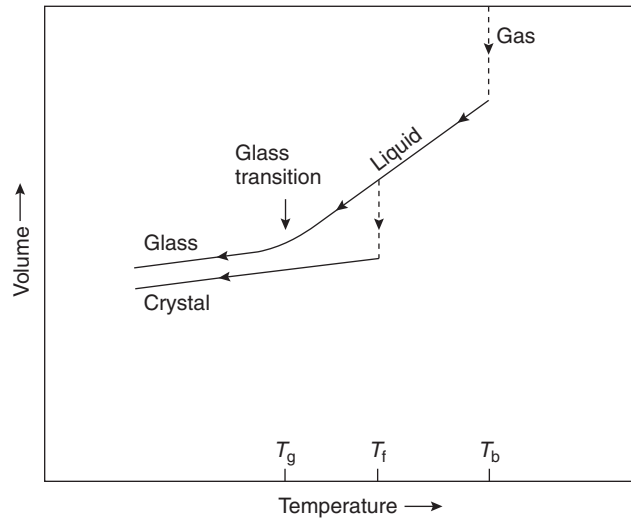


Fig. 6.3 A schematic plot of the volume of a material in various physical states as a function of the temperature (during cooling from high temperature). Transitions from vapor to liquid phase at T_b (boiling point), from liquid to a crystalline phase at T_f (the freezing point or melting point) during a very slow cool down, and from liquid to a glassy phase at T_g (the glass-transition temperature) during a fast cool down are shown.

linear ordered microstructure; (b) copolymers should have regular arrangements of the individual units; (c) an energy lowering, due to maximizing interactions through ordered close packing, should occur; and (d) it should be kinetically possible in real time. Note that as the structural complexity of the polymer increases the possibility of crystallization decreases. A highly branched and/or cross-linked polymer may not crystallize. Crystallization as well as solidification into an amorphous/glassy state leads to a decrease in volume (in liquid state). Figure 6.3 shows a schematic plot of volume as a function of temperature, both the formation of glassy and crystalline states are plotted. For most materials a fast cooling causes the formation of an amorphous/glassy state (sometimes into a very finely grained solid). The transition from the liquid to glassy solid occurs at a temperature called T_g as mentioned earlier. This is the temperature that determines the applicability of a polymer as an ILD and one requires this temperature to be higher than the highest process (post-ILD deposition) temperature. Note that intermolecular interactions, chemical structure, diluents and polar or bulky groups on the chain influence T_g as mentioned earlier. Also qualitatively T_g increases with increasing molecular weight of the polymer (see Chapter 2).

Polymers are large chain molecules, and during crystallization, the chains generally span several unit cells. Thus a crystalline unit cell holds a part of the chain and crystallographic knowledge is confined to this part only. Many polymers arrange themselves in zig-zag manner to be accommodated in the unit cell during crystallization. All those behaviors are driven (a) mainly by the energy-lowering (minimization) effect and (b) to generate-defects in the

crystalline state. In general, we see a mixture of crystalline and glassy materials that determines the density of the polymer. Thus, one can define:

$$\text{Weight \% crystalline} = \frac{d_c(d - d_a)}{d_c(d_c - d_a)} \times 100,$$

where d, d_c, and d_a refer to the measured density, the density of fully crystallized polymer, and the density of all amorphous/glassy polymer, respectively [7].

Deformation of the polymer ILD is also of concern since the ILDs, in general, may experience severe stress conditions resulting from their processing and metal deposits. Polymers have, in general, Young moduli that are about an order magnitude lower compared to metals. Also, most polymers have high coefficients of thermal expansion (see Chapter 2). Higher operating and process temperatures may then lead to viscoelastic deformation and a loss of interconnect/ILD reliability. Such deformations and poorer mechanical properties compared to metal are the result of covalent bonding and comparatively easier movement and rotation of polymer chains with respect to each other.

Three most important properties of a polymer for application as an ILD are: (a) the electrical properties; (b) mechanical stability (especially during a chemical mechanical planarization, CMP, process); and (c) thermally and electrically induced diffusive interactions with the surrounding material – generally a metal or alloy and another dieletric used to provide passivation.

The electrical properties of concern (see Chapter 2) are: (i) the dielectric constant; (ii) the leakage currents under applied basis; (iii) the electrical breakdown fields or voltages; and (iv) stability under very high frequency applications. When comparing various polymers these properties will be focused. Similarly, the adhesion of polymers to underlying and overlying films and its relationships with the CTE and the stress in the films have been discussed in Chapter 2. In this chapter we will emphasize them only in relation to the polymer processing.

Diffusive interactions (subject of discussion in the following section) between the polymer ILD and its surroundings are very important in determining the reliability (via the affect on the electrical and mechanical stabilities) of the ILD in particular and the device/circuit, in general.

6.2.1 Representative polymer structures

A large number of polymers have been developed and tested for application as ILD in a multilevel interconnection scheme. Figures 6.4–6.10 show the structures of several of such polymers, while their dieletric constants and T_g are listed in Table 6.1 [11–19].

6.3 Diffusive interactions in polymer surroundings

Many polymer–surface material interactions are weak and dispersive as in case of polyethylene and graphite. On the other hand, polymer and metals interactions are strong and lead to metal

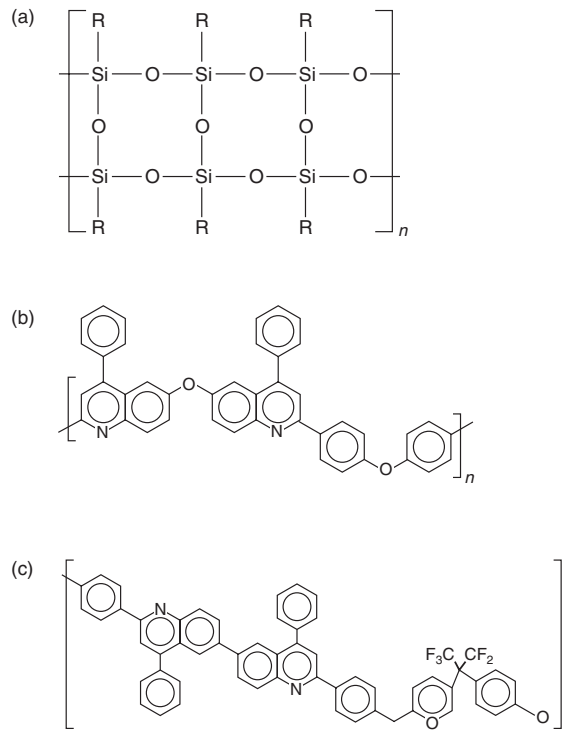


Fig. 6.4 Representative structures of: (a) hybrid organosiloxane (HOSP); (b) poly(quinoline)s; (c) poly(quinoline) (PQ)-100.

diffusion in the bulk of polymer [21]. Besides externally induced forces (thermal, electrical, chemical, and occasionally mechanical), the structure, porosity and surface functional groups play a very important role in these interactions. The effect of an applied electric field on the polarization and charge generation within the dielectric is expected to influence the diffusion and interactions. With respect to diffusion in the so-called crystalline polymers, the micro-crystallites in polymers can be regarded as impermeable islands embedded in a continuum of permeable amorphous media. The diffusion coefficients of penetrating atoms in a polymer microcrystal are much smaller compared to their values in the amorphous phase. A non-uniform distribution of diffusant can be expected during thermal processes. In the amorphous phase diffusion and viscoelastic properties are expected to be strongly influenced by the amount of free volume. Unfortunately, there is not enough experimental data on void distribution in most polymers that may have been subjected to different preparation conditions. However, non-uniform to layered distributions of voids together with existence of microcrystallites may cause changes in physical properties of polymers. Our interests lie in polymer–metal, polymer–moisture (including CMP slurry), and polymer-process gas environment interactions and their impact on the polymer properties.

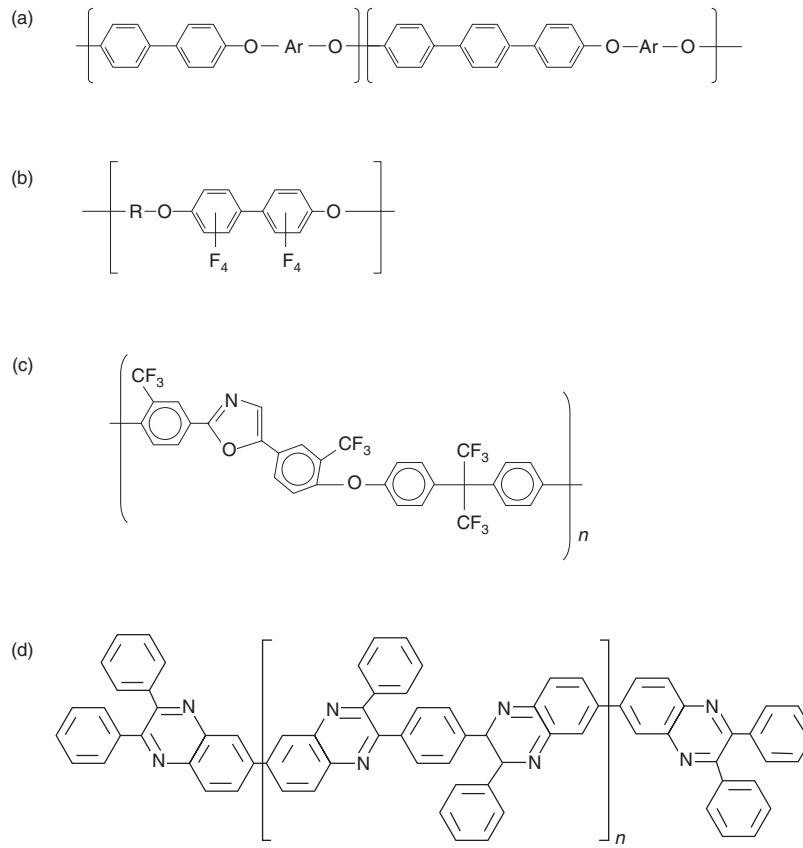


Fig. 6.5 Representative structures of: (a) poly(arylethers); (b) fluorimated poly(arylethers) (one of them is (FLARE™); (c) poly(arylene ether oxazole); (d) polyphenylquinoxaline.

6.3.1 Diffusion in polymers

Many theories have been developed describing diffusion of species in polymers. These theories can be classified as either molecular or free-volume models. [22, 23]. Molecular models involve specified motions of the diffusant molecular and the polymer chains relative to each other and take into account intermolecular forces. The diffusers are localized in holes of suitable size in the polymer matrix above the glass transition temperature (T_g) as a result of random motion of polymer segments. Occasionally, the diffusers acquire thermal energy from collisions with surrounding segments to jump into neighboring holes large enough to accommodate these diffusants (molecules). In such theories diffusion is a thermally activated process, and the diffusion coefficient D exhibits an Arrhenius-type behavior [22]. Within these theories the activation energy can be temperature dependent and is based on model experiments involving diffusion of

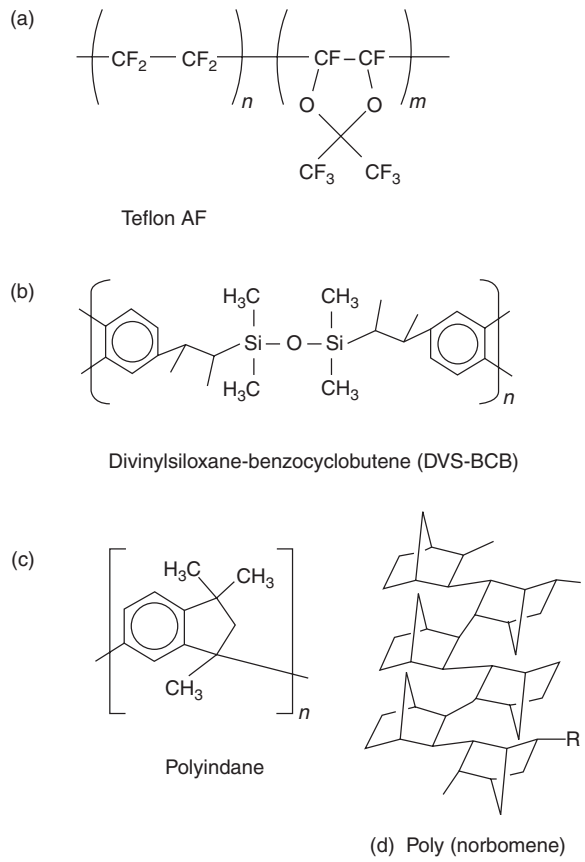


Fig. 6.6 Representative structures of: (a) Teflon AF; (b) divinylsiloxane-benzocyclobutene (DVS-BCB); (c) polyindane; (d) poly (norbomene).

small molecules in polymers. In such experiments diffusions is characterized by almost linear Arrhenius plots over a wide temperature range.

Non-linear Arrhenius plots observed for diffusion of larger molecules [23, 24] have been explained on the basis of free-volume models. In free-volume models, the specific free volume is given by the difference of the total specific volume V^* and the specific occupied free-V_F^* volume V_0^*, which is usually assumed to be total free volume at 0 K. As the temperature is raised the material expands homogeneously due to increasing amplitude of the anharmonic vibrations with temperature. In addition, holes are formed, which are distributed discontinuously throughout the polymer material. The first type of the volume is called interstitial free-volume V_{FI}^*. It is distributed uniformly among the molecules. V_F^* can then be expressed as:

$$V_F^* = V_{FI}^* + V_{FH}^*, \quad (6.1)$$

where the hole free volume V_{FH}^* is assumed to be redistributed without any change in energy.

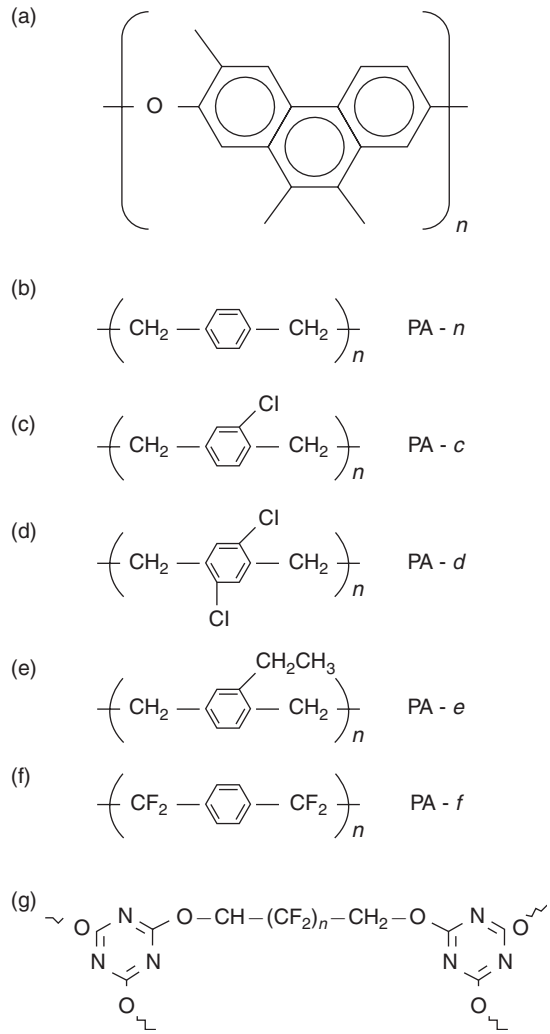


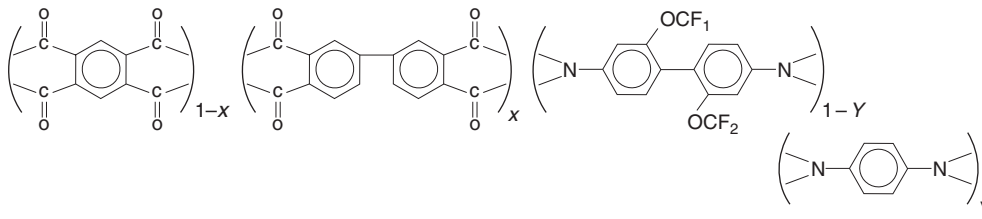
Fig. 6.7 Representative structures of: (a) SILK; (b–f) five different parylenes; (g) fluoromethylene cyanate ester.

In these models diffusion of solute molecules is described in terms of its coupling to matrix, with an expression for the solute diffusion in a polymer matrix evaluated as [23]:

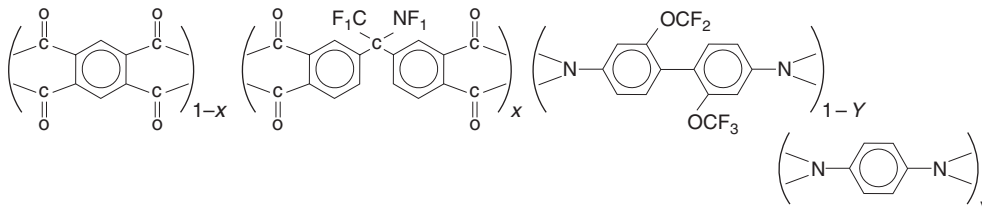
$$D = D_{0S} \exp\{-\gamma p V^*/V_f^*\} \exp\{-E^*/k_B T\}, \tag{6.2}$$

where γ is a geometrical constant depending on configuration of matrix and E^* the activation energy for diffusion. The coupling parameter $p = V_S^*/V_f^*$ only depends on the critical molar volumes of the solute V_S^* and the polymer V^* (volumes are now taken per molecule). According

FPI-45M



FPI-136M



where $0 \leq x, y \geq$:

(a)

(b)

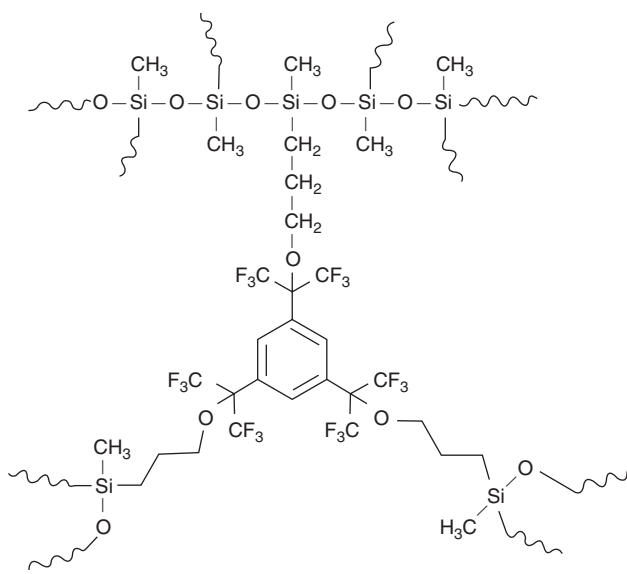


Fig. 6.8 Representative structure of: (a) fluorinated polyimide copolymers; (b) fluoro aromatic triallyl-ether copolymer.

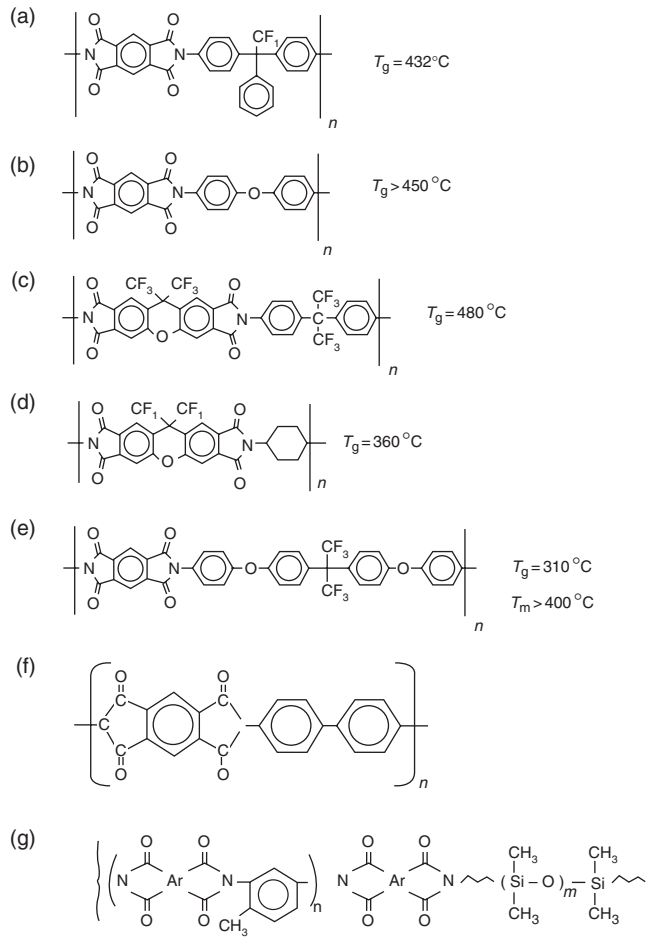


Fig. 6.9 Representative structures of: (a) PMDA/3FDA polyimide; (b) PMDA/0DA polyimide; (c) 6FXDA/6FDA polyimide; (d) 6FDACH polyimide, (e) PMDA/4–8DAF polyimide; (f) polyimide; (g) polyimide siloxane SIM™2010.

to [24] V_S^* is purely a geometrical constant and should not be matrix dependent. The volume V^* is the critical volume for a polymer jumping unit, typically a monomeric unit, to jump from one position to another.

Vrentas and Duda [24] assumed that the free volume increases linearly with temperature within a moderate range in accordance to the following relation:

$$V_f^* = V_f^*(T_g) + \alpha_f V^*(T - T_g), \tag{6.3}$$

where α_f is the mean thermal expansion coefficient of free volume and V^* is the mean molar volume over a certain temperature range. Coefficient is smaller than the total thermal expansion

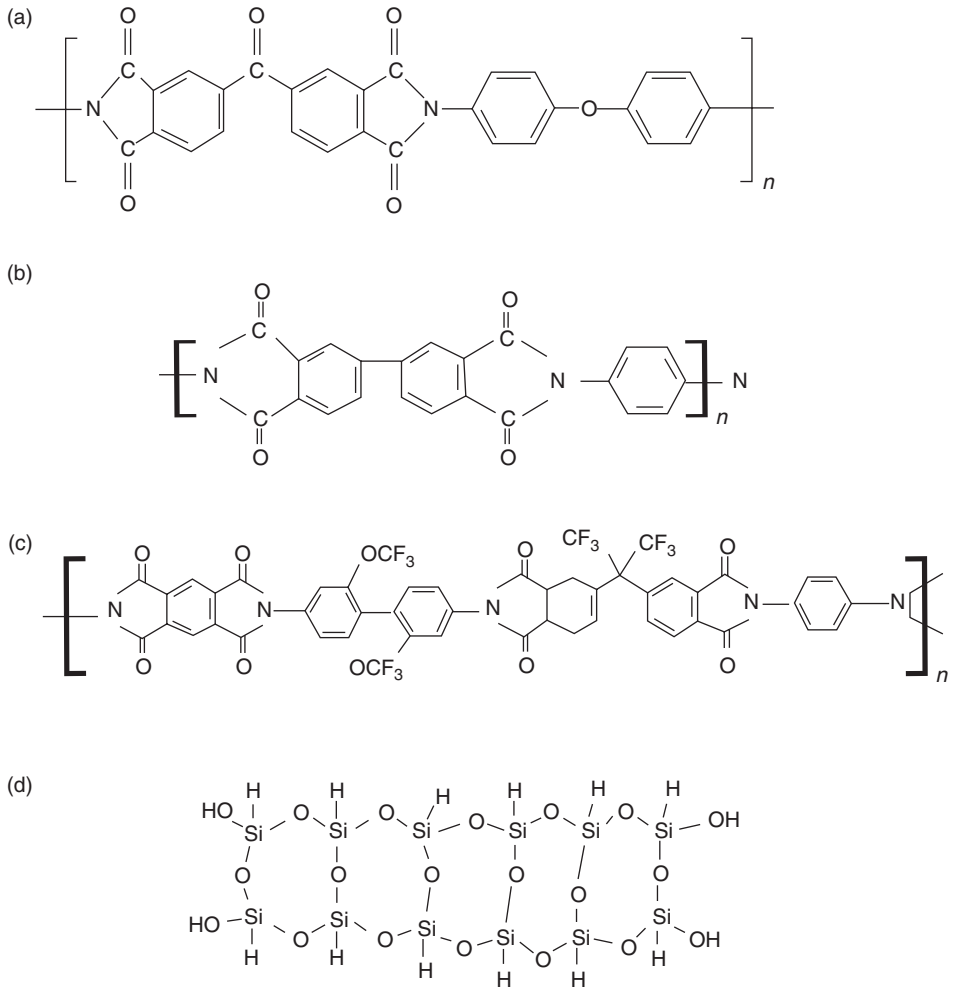


Fig. 6.10 Representative structures of: (a) BTDA–ODA; (b) PMDA–BPDA–PDA; (c) PMDA–TFMOB–6FDA–POA; (d) hydrogen oilesquioxane (HSQ) (methyl group replaces hydrogen in MSQ).

coefficient, which accounts for the formation of free-volume holes and the homogenous expansion of the material due to the increasing amplitude of the anharmonic vibrations. This parameter is approximately equal to the difference in the volume expansion coefficients above and below T_g [25]. Combining (6.2) and (6.3) it is possible to obtain the Williams–Lander–Ferry equation for diffusion in polymers [24]:

$$\ln\{D(T)/D\ (T_g)\} = A(T - T_g)/(B + T - T_g), \tag{6.4}$$

where $A = \gamma V^*/V_f(T_g)$ and $B = V_f(T_g)/\alpha_f V^*$.

Table 6.1 List of some of the polymers investigated for application as ILD[a]

Polymer[b]	Moisture absorption (wt%)	κ	T_g (°C)
HOSP	1–2	~2.5	
Polyquinolines		2.8	250–420
PQ-100		2.9–3.1	
Polyarylethers	<0.4	2.6–2.8	260–450
FLARE	<0.2	2.4–2.6	280–300
PAEO		2.6–2.8	205
PPQ	1	2.7–2.8	365
Teflon AF		1.9	⩽360[c]
DVS-BCB	<0.2	2.6–2.7	⩾350
Polyindane		2.6	420[c]
Polynorborene	<0.1	2.2	365
SILK	<0.25	2.6–2.7	>450
Parylene-n	<0.05	2.6–2.8	420
Parylene-c		2.7–3.0[d]	
Parylene-d		2.7–3.0[d]	
Parylene-f		2.2–2.4[d]	> 530[c]
FMCE		2.3	⩾300[c]
FPI-45M	0.95	2.80	≈500[c]
FPI-136M	1.5	2.64	≈500[c]
F-TAE		2.2–2.8	⩾300[c]
PMDA/3FDA		2.8	432
PMDA/ODA		3.6	⩾450
6FXDA/6FDA			460
6F/DACH			360
PMDA/4-BDAF			310
Polycimide	1.5–3.0	2.7–3.1	350
Polyimide siloxane SIM 2010		2.8	>350
BTDA–ODA		3.5	
PMDA–BPDA–PDA		~2.6	
PMDA–TFMOB–6FDA–PDA			
MSQ		2.7–3.0	>500[c]

[a]From Refs. [19,20], also see Chapter 2.
[b]See Figs 6.4–6.10.
[c]Decomposition temperature.
[d]Estimated.

The authors extended their model to glassy polymers, assuming that the polymer material is in equilibrium state above the glass transition temperature and in a non-equilibrium state below T_g. The structure below T_g is assumed to remain invariant during the diffusion process. The rapid changes in the volume expansion coefficient can be characterized as a step change at T_g.

The phenomenological parameter $\gamma(0 < \gamma < 1)$ was introduced to describe the character of the change in volume contraction, which can be attributed to the glass transition. If the equilibrium liquid structure is also realized below T_g then $\gamma = 1$, while if the structure is frozen at T_g, $\gamma = 0$; in the latter case the hole free volume below the glass transition is given by the volume at T_g. Note that the value of γ is the thermal free-volume expansion coefficient below T_g.

Stress also influences the diffusion process. In polymer films, large mismatch in thermal expansion between film and substrate gives rise to thermal stress. Additional stress is introduced by film shrinkage during the curing procedure. However, due to the small Young's modulus of polymers and the ease of stress relaxation, the stress level is relatively low and goes to zero as the temperature approaches the maximum curing temperature of 400°C [26]. Therefore, no significant influence on diffusion is expected.

While there are other theories of diffusion in polymers (e.g. [23]), metallic diffusion cannot be described in terms of these models. Relation between polymer structure and diffusivity of species is not well characterized, or understood. Fractal models for describing diffusion in polymers are particular promising.

6.3.2 Diffusion of metals in polymer

A large volume of the research results are available reporting the interactions of a metal on a polymer or vice versa. Most of this work, carried out up until the early 1980s, focused on applications unrelated to microelectronics [19, 20, 27, 28], although some of the focus was on applications of polymers as a dielectric in electronic packages or as a sealant. Use of a polymer as an ILD on a chip is especially a recent thing. Thus, whereas earlier work used a variety of analytical techniques to elucidate the metal–polymer interactions, the recent ILD applications-related research added on the electrical degradation/property studies using *C–V* and *I–V* measurements. These electrical tests are necessary to determine the impact of metal diffusion in polymer (or the metal–polymer interactions) on the electrical stability of the ILD polymer. Conventional analytical techniques, then used, help elucidate the mechanisms of such interactions. It is important to point out that theses metal–polymer interactions are controlled, at least initially, by the interfaces and thus depend on whether: (a) a metal is deposited on the polymer; or (b) a polymer is deposited on the metal. In case (a), the metal is generally deposited by a physical vapor deposition (PVD) technique or a chemical vapor deposition (CVD) technique, both of which expose the polymer surfaces to vacuum conditions and to energetic metallic species. In addition, there is an exposure to electrons and X-rays in an e-gun evaporation, to plasmas in sputtering, and to CVD precursors adsorption and decomposition processes on surfaces. Also, some polymer films may degas during the pump-down (to create-vacuum) cycle, leading to voids and/or pits in the film or on the surfaces. Each of these processes affects the surface and/or the electrical behavior of the underlying polymer. Note that the deposition rates also influence the metal–polymer interactions. For example, Cu and Ag, when deposited at low

rates but at comparatively higher temperatures, are found to diffuse into and cluster both near the surfaces and in the bulk of a polyimide film. The clusters, however, did not form at high deposition rates [29–32] (also see discussion below).

In case (b), a polymer is deposited on the metallic film either by a spin-on technique, CVD, or plasma polymerization process. Metallic surfaces in all such cases are exposed to atmosphere and are in general oxidized prior to polymer deposition. A spin-on-polymer exposes the metal to polymer forming precursors, solvents and to the reaction products including the desired polymer. The reaction products, other than the polymer, and solvents are driven out during the so-called curing and annealing processes. CVD or plasma processes may affect the metal surface as in case (a) discussed above. Both type (a) and (b) process combinations are to be used in a multilevel scheme where polymer forms an ILD between two metal layers and thus should be investigated to elucidate the metal–polymer interactions. Table 6.2 summarizes possible effects in the two cases.

Generally metal is a diffuser at the metal–polymer interface. However, there are cases where reactive groups or ions present on the polymer chain react with the metal and produce species that diffuse in the metal. The reactivity is highest for oxygen containing moieties (e.g. $=C=O$, –COOH, –CHO, $\equiv C–O–C\equiv$), followed by those containing nitrogen (e.g. –CN, $–NH_2$, $=NH$). Alkyl groups have least reactivity although phenyl-type groups have comparatively higher reactivity [33]. Fluorine and other halogens also have considerable reactivity; a classic example is that of interactions between Al films and fluorinated polymers [34].

Table 6.2 Comparison of resulting effects in metal-on-polymer and polymer-on-metal structures

Effect	Metal-on-polymer	Polymer-on-metal
Metal reactivity	High as energetic species impinge on polymer	Surface metal oxide may reduce activity
Electron, X-rays and plasmas in e-gun, sputtering, PECVD or PACVD	Affect polymer surfaces and occasionally bulk behavior	Metal surface only affected during CVD type depositions
Solvent	None	Affects metal surface and metal diffusion (from solution into polymer)
Post-deposition treatment (interactions)	Generally annealing and CMP, may induce metal/polymer interactions	Curing, leaking, annealing may induce initial interactions, metal may oxidize and/or act as a catalytic agent, dry etch and CMP also affect these interactions
Adhesion	Possibly improved physical bonding due to energetic metal species	Possibly improved chemical bonding
Deposition environment effects	Metal may be contaminated	Polymer may be contaminated particularly with solvents
Surface modification	May occur	May occur

The interactions, sometimes, lead to interfacial reaction products that form barriers to further interactions and diffusion. Literature is full of metal–polymer interactions, organometallic formations and decompositions. We will concentrate only on interactions of metals, with emphasis on Cu and Al, with a variety of polymers.

Information on the diffusion behavior of copper and other metals in polymers, especially regarding the correlation with reactivity of the metal, have been obtained from ultraviolet photoemission spectroscopy (UPS) and X-ray photoemission spectroscopy (XPS) studies [35, 36]. The following conclusions were reached: Cr and Ti interact strongly with polymer, whereas the reactivity of Ag and Cu is relatively weak and that of Al and Ni is somewhere in between. For copper, the core level intensity decreases substantially upon heat treatment, indicating that copper diffused into the polymer.

Tromp *et al*. [29] investigated interdiffusion at the copper–PI (polyimide) interface employing high-resolution medium energy ion scattering (MEIS). MEIS spectra of copper evaporated onto PI at various temperatures and very low rates clearly indicate that Cu strongly diffuses into the PI. The tails of scattering intensity at lower energy are a direct indication of this diffusion. However, the depth distributions do not resemble simple diffusion profiles. In particular, the occurrence of a maximum concentration below the surface indicates the existence of copper clusters buried in the polymer.

The formation of copper and silver clusters in the bulk of PIs at low evaporation rates and elevated temperatures has been confirmed by means of cross-sectional TEM studies [29]. The size of copper particles can be found at a greater depth in PI than silver particles [37]. Transmission electron diffraction patterns of the metals spheres indicate a structure of crystalline copper; interestingly, the spread in sizes of the spheres at a given temperature was found to be very small. Near surface layer of imperfections (voids) can be a reason of copper clusterization on such sinks.

The diffusion of copper in PI (Kapton–H PI films) was studied [37] by Rutherford backscattering (RBS) for high deposition rate (1 nm/s) deposits. Annealing treatment significantly enhanced the diffusion of metal atoms. The high-deposition rate copper shows Fickian diffusion behavior with no evidence of near-surface copper clusterization. The diffusion-measured coefficient of copper is 3×10^{-14} and 1×10^{-13} cm^2/s at 200 and 400°C, respectively.

Studies of Cu, Ag, Ni, and Mo diffusion in PI at elevated temperatures using RBS was reported in [38]. No mobility of Ni and Mo was observed up to 375°C, while Cu and Ag diffuse well into PI at that temperature. Das and Morris [39] also found cluster formation effect for ion-implanted Cu in Kapton (PMDA–ODA) films by means of RBS. Based on the same technique, Cu diffusion was demonstrated in parylenes [40]. It should be noted that due to the low energy loss in polymers, the depth resolution of RBS is limited to approximately 10 nm. Therefore, results from this indirect technique should be treated with caution.

Cross-sectional TEM studies of copper diffusion in PMDA–ODA have been reviewed in [40]. After evaporation of copper on PMDA–ODA film at different rates and temperatures, samples

were thinned to electron transparency in a direction perpendicular to the Cu/PMDA–ODA interface. Copper formed nearly spherical agglomerates inside the polymer when evaporated at very low rates (about one monolayer per minute). The size of these particles and their average distance from the interface increased markedly with increasing deposition temperature. At 300°C cluster sizes in the 100 nm range were observed. However, clusters deep in the bulk of the polymer were only detected at very low deposition rates, of the order of one monolayer per minute. At higher rates (on the order of 1 nm/s) and low deposition temperatures, Cu forms an uniform film at the surface. Subsequent annealing results in island formation on the top of polymer. At higher evaporation rates, high-temperature (>300°C) deposition did not produce copper clusters inside the polymer, at least to the detectable limit of these techniques.

The formation of large metal clusters deep in the bulk of a polymer as observed for copper and silver in PMDA–ODA is fascinating and of great scientific curiosity. Metals with low reactivity tend to cluster in islands on polymer surfaces due to their high cohesive energy [42]. Also, subsurface particle formation has been reported for polymers above the softening temperature, as metal aggregates form completely within the polymer substrate [43]. The driving force for this process is apparently related to high cohesive energy of the metal, which gives rise to a surface energy σ_M that exceeds the surface energy of the polymer σ_P by one or two orders of magnitude. If the surface energy of the metal is also larger than the sum of the interfacial energy σ_{MP} and the polymer surface energy ($\sigma_M > \sigma_P + \sigma_{MP}$), a driving force is present for a metal cluster to be embedded completely in the bulk of polymer. Below T_g the strain energy for the cluster in the polymer matrix must also be taken into account. The voids in polymers, originating sometimes from the imidization process, could also play a role, for example in reducing the strain energy for cluster formation. Void filling would additionally eliminate surface energy of the voids, the void sizes being comparable to those of the metal clusters in the bulk.

An important factor in the kinetics of metal aggregation in polymers is the formation of big clusters inside the polymer during low deposition rates and at elevated temperatures, where a large portion of the metal atoms can diffuse into the bulk (as shown by the radiotracer studies discussed below). This suggests that copper particles inside the polymer do not form by migration of surface clusters into the bulk, rather by diffusion of single atoms or very small complexes and subsequent aggregation.

A radiotracer technique in conjunction with ion-beam sputtering (IBS) for depth profiling has been proven to provide the required depth resolution and sensitivity to measure diffusion of metals in polymers. Diffusion of ^{67}Cu and ^{110}Ag in spin-coated PI films of pyromellitic dianhydride–oxydianiline (PMDA–ODA) [43] and of ^{67}Cu in biphenyl dianhydride–phenylene diamine (BPDA–PDA) has been studied over an extended temperature range [44, 45]. Penetration profiles of the ^{67}Cu copper exhibit an initial non-Fickian steep drop in the activity followed by a Fickian tail. The linear ranges of the penetration profiles were attributed to diffusion of isolated atoms, and diffusivities were determined from the slopes. The first part was attributed to the cluster formation of the copper tracer during deposition via surface diffusion.

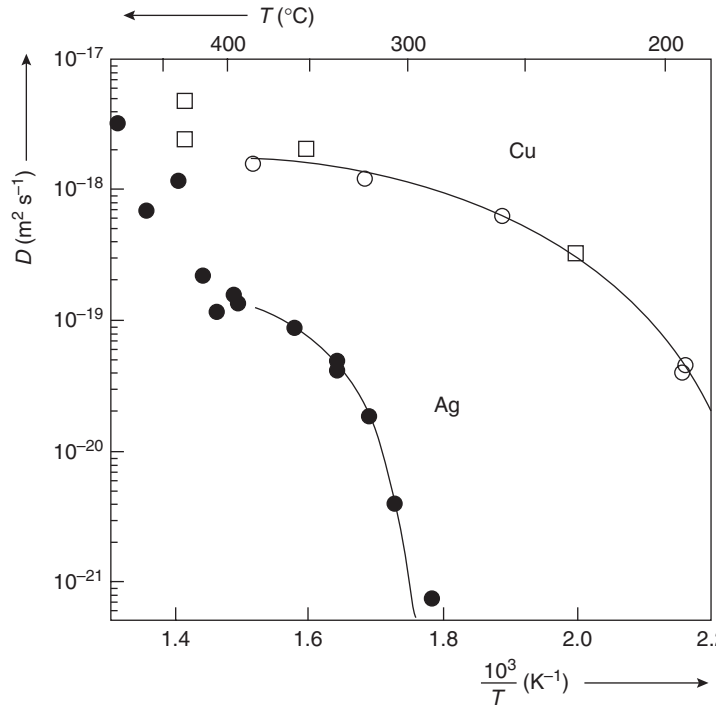


Fig. 6.11 Arrhenius plot for the diffusion of Cu and Ag atoms in polyimide. From Faupel [45].

Three-dimensional Monte Carlo calculations simulating the copper–polymer interface indicate that clusters tend to form even with the deposition of only one-fourth monolayer of copper. In practice, both processes (clusterization and diffusion in to the bulk of polymer) can take place in different quantities, depending on parameters such as temperature, deposition rate, type and condition of polymer surface and, perhaps, method of deposition. The actual mechanism(s) involved can be difficult to determine even with carefully controlled and well-instrumented experiments.

Results for diffusion of copper and silver atoms in PMDA–ODA are summarized in an Arrhenius plot ($\ln D$ versus $1/T$) in Fig. 6.11 [45]. Note that the smaller Cu atoms diffuse considerably faster than Ag atoms. For silver, an increase in slope occurs at approximately 400°C, slightly below the expected T_g. For copper, a corresponding break in the Arhenius plot at this temperature cannot be established definitively. The Arhenius plots for both diffusants exhibit strong non-linearity, the convex curvature being stronger for the larger atoms (Ag) and the break near T_g predicted by the free-volume theory, as described in the previous section. This free-volume theory predicts that a plot of $\ln D$ versus $1/T$ will not be linear either above or below T_g. It should be noted that in this work the concentration of the tracer was too low in the linear range of the profiles to promote clusterization.

Measurements have shown that copper diffusion in BPDA–PDA proceeds substantially slower than in PMDA–ODA. Although the chemical reactivity of both polymers is expected to be much the same, BPDA–PDA forms a more compact polymeric structure [46]. Apparently, the diffusion of weakly chemically interacting metal, such as copper can serve as an effective probe to examine the molecular morphology and polymer dynamics.

Studies of copper diffusion in parylene (PA)-type polymers were also evaluated [39, 46, 47], with diffusion of copper as a function of different crystalline states (phases α and β) of PA-n reported [47]. Copper was deposited on PA-n by partially ionized beam (PIB) technique with the substrate temperature kept at room temperature and the samples of Cu/PA-n were annealed at 390 and 350°C. RBS measurements showed that copper diffusion starts at temperature about 300°C with more intensive diffusion at higher temperature. The α to β phase transition is not influenced by diffusion of copper and vice versa. Copper deposited on α-PA does not diffuse even after a long time (6 h) annealing at 300°C.

Similar investigations were carried out with copper, silver and aluminum deposited by PIB technique on PA-n [48] and annealed at 300, 350, and 400°C with the diffusion of the metals subsequently studied using SIMS. Metal diffusion into PA-n was observed comparable to that in PI. The copper diffusion profiles were of low concentration but extended fairly deep. Under the experimental conditions (method of deposition, annealing temperature), non-linear diffusion was not observed with PA (unlike the observation in PIs). Comparison between the diffusion constant of copper (6×10^{-14} cm^2/s at 400°C) and aluminum (4×10^{-14} cm^2/s at 300°C) indicates that copper has at least a comparable diffusion constant. On the other hand, for PA-f the diffusion constant for copper is much smaller, approximately 0.2×10^{-14} cm^2/s at 300°C [49].

As briefly mentioned earlier, it is noted that the chemical structure of the polymer, the nature of the functional groups (moieties), the amount of cross-linking, the available free-volume, the solvents (and other impurities) trapped in the film, and the type of the metal (its oxidation tendency) play very important roles in determining the metal–polymer interdiffusion. In Section 6.4, chemical interactions are specifically examined. Such interactions may seriously affect interdiffusion behavior. But first, in the following sub-section, the changes in the electrical properties/behavior particularly the capacitance–voltage characteristics (see Chapter 2) of the capacitors with polymer as a dielectric are examined with emphasis on the role of diffusion (thermally or electrically induced) and that of polymer itself.

6.3.3 Metal ion drift in polymers – C–V measurements

In Chapter 2, *C–V* behavior of an ideal and that of non-ideal metal–insulator–semiconductor (MIS) capacitors were discussed. The source of the non-ideality, in *C–V* plots, was linked to the presence of the oxide traps, interface states, fixed charges, and the mobile charges in the insulator or at the insulator–semiconductor interface. Thus a careful study of a MIS capacitor, made with the as-deposited and annealed dielectric with or without being subjected to a electrical bias and temperature (so-called BT stressing or simply BTS), is essential even before the diffusion of

metallic species in such dieletric is investigated. Such a systematic study is necessary to isolate the intrinsic electrical instabilities in polymer ILD from those induced by the metallic diffusion and interactions. A classic example of such a study is that of isolating the role of water and other hydrogenous species in CVD SiO_2 films from the basic metal related effects, as discussed in Chapter 2 [50, 51]. It is also important to recognize that semiconductor–insulator interface should be kept as near ideal as possible, because the interactions across this interface complicate the interpretation of resulting electrical behavior. Thus an adopted practice is to use a thin thermally grown dry oxide on silicon prior to the application of polymer films [52, 53]. In such a case the total capacitance of this dual dielectric capacitor is given as

$$C_{\text{total}} = \frac{\kappa_{\text{p}}\kappa_{\text{SiO}_2}}{\kappa_{\text{SiO}_2}t_{\text{p}} + \kappa_{\text{p}}t_{\text{SiO}_2}},$$

where κ and t are the dielectric constant and thickness, respectively. Subscript p represents the polymer dielectric. When $t_{\text{SiO}_2} \ll t_{\text{p}}$ one can approximate that capacitance is mainly due to the polymer dielectric.

Figure 6.12 shows *C–V* characteristics of variously treated DuPont polymer called FPI-46, which is a fluorinated copolymer composed of three BPDA, TFMOB, and 6FCDA monomers [53, 54], the structures of which are shown in Figs. 6.4–6.10. Three different samples 1, 2, and 3 are tested with or without BTS as shown on the figure. The polymer films were spun and soft baked at 250°C followed by a hard bake at 325, 350, or 375°C, respectively for sample number 1, 2, or 3. Following this the copper metal electrodes were deposited. All the samples show same accumulation capacitance (hence same κ) and no movement of curves on BTS (at 0.6 MV/cm, 1 MH_z and 150°C). However, sample 1 showed a shift towards negative voltages indicating immobile fixed positive charges in the polymer or at the interfaces. Authors attribute this behavior to incomplete polymerization at low temperatures (less than 350°C) and the presence of excess monomers with charged functional groups, ionized (unterminated) end of the polymer chain, and broken parts of functional groups. Annealing at or above 350°C eliminate or reduce these charges. Note that BTS did not indicate Cu drift in this polymer although one may consider the applied bias to be less severe.

Although a large number of publications have disqualified several polymers simply by looking at the *C–V* shifts during the BTS of the Cu–polymer–thin SiO_2 on Si capacitors, a careful look at the intrinsic role of the polymer and its structure on such shifts (independent of the metal used as the electrode) is essential. Mallikarjunan *et al.* [55] studied a hybrid organosiloxane (OS) polymer with $\kappa = 2.5$ in conjunction with different gate metals – copper, aluminum, tantalum, and platinum. The results obtained with Cu and Al metals could not be explained satisfactorily with existing understanding; therefore other gate metals Ta and Pt were also investigated. Tantalum, pure or as a nitride, is useful as an adhesion promoter/diffusion barrier layer; and is similar to aluminum. Platinum, on the other hand, is a noble metal and is not expected to diffuse or drift into, or interact readily with the dielectrics.

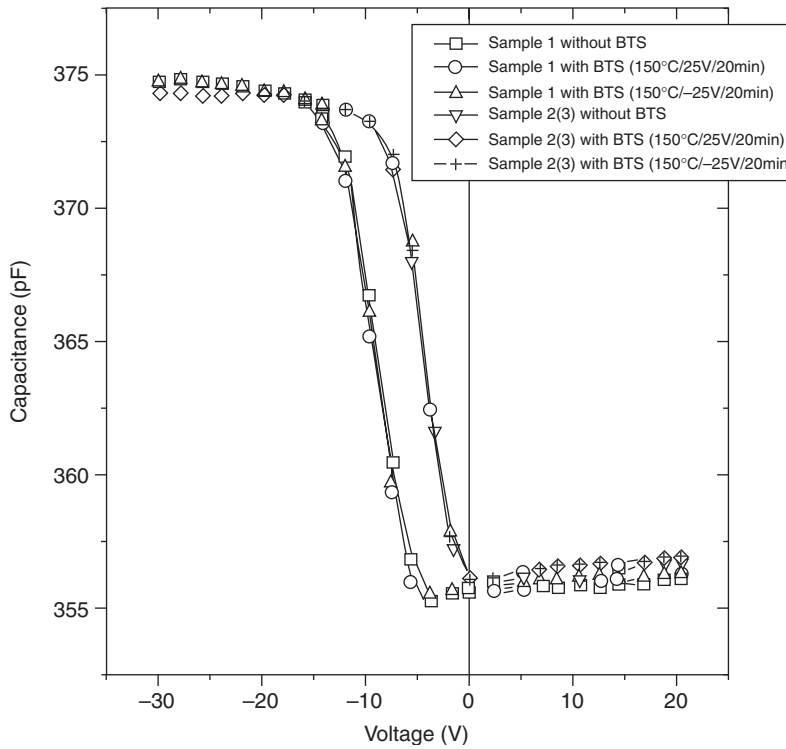


Fig. 6.12 High frequency (1 MHz) *C–V* characteristics of samples 1, 2, and 3 annealed, respectively, at 325, 350, and 375°C and then tested with or without BTS. From Lee [53].

In Fig. 6.13, the total number of charges obtained from measured *C–V* shifts under BTS increases in the order Pt, Cu, Ta, and Al, with no charges detected for Pt and maximum detected with Al as the gate metal. (In this calculation, it was assumed that singly ionized mobile metal ions entered the dielectric both because of ease of ionization and instantaneous movement under bias and because the solid solubility of higher ionized states of most metals are much lower than that of the singly ionized state [56]. Once injected, it was assumed that the ions penetrated up to the OS/thermal SiO_2 interface. This is because both aluminum and tantalum react strongly with SiO_2 and could be trapped by dangling bonds at the SiO_2/OS interface. Moreover, copper is known to penetrate into thermal oxide only under more aggressive test conditions [57, 58].

Also shown as an inset in Fig. 6.13 is a plot of the number of charges as a function of the heat of formation for the oxides of these metals per oxygen atom. This plot clearly points out that the number of charges (or metal ions) per square centimeter that reach the OS/SiO_2 interface is directly related to the metal's oxidation tendency as measured by their oxide's heat of formation. Also note that first ionization energies of Pt, Cu, Ta and Al are 9.0, 7.726, 7.89, and 5.986 eV, respectively.

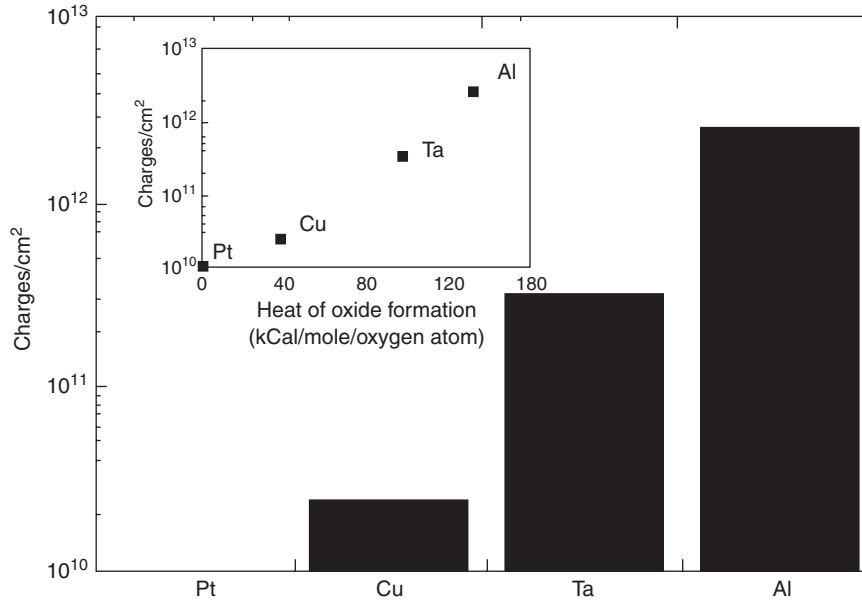


Fig. 6.13 Total number of charges after BTS at 150°C and 0.5 MV/cm for 30 min for all metal/HOSP/SiO_2/Si capacitors. Inset shows relation of total charges to the heat of oxide formation per oxygen atoms. From Mallikarjunan *et al.* [55].

Pt has the highest and Al the lowest, with Cu and Ta in the middle. These numbers are reasonably in line with the oxidation tendency.

For metals (such as Al, Ti, and Ta) that show strong reaction with SiO_2, the formation of a stable metal–oxide diffusion barrier limits diffusion or drift into SiO_2. However, in polymers with significant organic content, such a reaction may not occur. Instead, oxygen-containing groups may increase the ionization tendency of the metal, and aid the drift process. Loke *et al.* [59] have used such a model to qualitatively explain Cu drift kinetics in different polymers.

A large number of studies have been carried out in the past examining metal diffusion in and metal interaction with polymers [20]. The metal's chemical reactivity has been reported to play a role in many cases. For example, Nguyen *et al.* [60] examined the nature of the interface between Al, Ni, Au, Cu, and Cr and poly*para*phenylene (PPP) and concluded that the formation of the oxygen–metal–carbon complexes at the interface correlated with the electrical characteristics (of the metal–PPP–metal structures) that were influenced by the oxidation ability of the metal used as the electrode. Similarly Hirose *et al.* [61] have reported that the penetration of the reactive metal species (Al, Ti, In, Sn, Ag, and Au) in the molecular organic semiconductor 3,4,9,10-perylenetetracarboxylic dianhydrede (PTSDA) film is inversely related to their first ionization energy. As suggested earlier these results clearly indicate that the interpretation of thermal and/or electrical bias induced metal diffusion and its effect on the electrical properties

of the metal–polymer–substrate capacitors is strongly related to the polymer's molecular structure, composition, crystallinity, and how they are affected by the thermal and electrical treatments.

6.4 Chemical interactions

As mentioned earlier (see Table 6.2), deposition of metals on polymers or vice versa requires thermal treatments, plasma exposures during deposition and reactive ion etching, and CMP, all of which can induce chemical reactivity of different types at the metal–polymer interface. Such reactivity promotes adhesion through chemical bonding across the interface but could also lead to reactions away from the interface. In the following various types of reactivities and reaction products are briefly discussed by Krishnamoorthy and Murarka [62].

6.4.1 Precipitation and agglomeration

Copper binds weakly to the PI and therefore is characterized by significant diffusion into the PI and least chemical interaction with the PI at room and elevated temperatures. Ultraviolet photoelectron spectroscopy spectra of Cu/PI resemble the one obtained by simply superposing Cu 3d spectrum on top of PI spectrum, indicating again a weak interaction between Cu and PI. When the chemical bonding is weak, the metal is free to diffuse into the polymer and form clusters. Nearly spherical agglomerates of Cu were formed inside the polymer at low coverages, that is, about 1 nm giving rise to intermixing and cluster formation [63]. Diffraction pattern revealed that these agglomerates were Cu single crystals [41]. This precipitation was found to be a thermally activated process. It is expected that such precipitations may enhance mechanical strength of the polymer and affect the dielectric constant and current leakage.

6.4.2 Complex formation

In general, the presence of interfacial metal–oxygen chelate complexes correlates with the adhesion strengths. For Cu, Ni, and Cr, the adhesion strength of the metal film with one of the oxygen containing polymers is always greater than that with the oxygen-free polymer. Au films, which never formed complexes at the polymer interfaces exhibited low adhesion strength. These correlations imply that the presence of interfacial chelate complexes is desirable when bonding metal films to organic substrates. However, competing reactions on more complex polymer surfaces might prevent the formation of these chelate-like complexes and thus the presence of oxygen groups on a polymer surface does not necessarily guarantee a large adhesion strength for a metal film.

Polymeric units maintain structural integrity upon interaction with metal by means of complexing where the metal atoms form complexes with organic functional groups (ligands)

such as carbonyl groups. The most extensively investigated C 1s level in PIs consists of a well-separated carbonyl (>C═O) peak. The changes in this peak position and shape were attributed to the chemistry occurring near this functional group. Haight *et al.* [64] have observed significant broadening and reduction of the intensity of the carbonyl peak when metal contracted polymer. This has led a number of investigators to conclude that the metal atom initially attacks the carbonyl functionality locally and is involved in the actual cleavage of carbonyl atoms from the PMDA unit [65]. But Haight *et al.* [64] have concluded on the basis of computational examination that the creation of an arene–metal π complex yields results that are fully consistent with the X-ray photoelectron spectroscopy (XPS) observations they have obtained. Also, the coordination of π-acceptor ligands to metal atoms is a process of much lower activation energy than oxidative addition that others have proposed [65].

Another strong evidence for this π-complex comes from the work by Konstadinidis *et al.* [66] in Cr–polyimide structure which was formed by ion implanting 3.3×10^{17} atoms/cm^2 at 100 keV using extended X-ray absorption fine structure (EXAFS). They observed that the Cr/PI data gave a first shell of six carbon atoms that were 2.03 Å away from the Cr atom. This six-fold symmetry is indicative of a Cr-complex with a six member aromatic ring (arene). These results are corroborated by Cr reaction with model compound benzene, forming bis(benzene) Cr complex with the Cr to the center of the ring distance of 1.61 Å [67]. A Cr–C distance of 2.03 Å translates to Cr–ring center distance of 1.62 Å, which provides an excellent agreement between the two studies. Similar case of chromium–arene π-complex at low chromium coverage is reported on different polymers such as phenylacetylene–*para*-nitrophenyl-acetylene (PA–PNPA) [68,69]. Similar to Cr-systems, the bonding of Al metallization with polystyrene was reported to be formed of a weakly bonded complex of Al with phenyl ring of polystyrene.

It is now well established that metal atoms adsorbed on polymer surfaces interact preferentially with strongly electronegative atoms [70], leading to the formation of a metal–oxygen–polymer complex at the interface. In systems such as Al/polycaprolactone [71], and in Al/PI systems [63], a reaction between Al and the oxygen of the C═O groups formed Al–O–C complex [72]. In this reaction, charge was first transferred from Al to C via O with consequent breaking of C═O. Al–O–C and Ni–O–C complexes are reported in Al/PPP and Ni/PPP systems where the polymer has no oxygen functionality. This is attributed to the initial oxide layer on the metal surface [73].

6.4.3 Carbide formation

The initial reactivity of metals such as Al, Cr, Ni, and Ti with polyimide seems to reside in the oxygen affinity of the metal at low metal coverages. However, as the coverage is increased, an additional mechanism, metal–carbon bond formation, is involved in the reaction. The metal carbide formation is suggested for Al [74–76], Cr [77–81], Ni [82], Ta [83], and Ti [84, 85] in contact

with PI. For example, on going to higher thickness in Cr on PA–PNPA [68], and on diethynybiphenyl [69] a sigma-bonded carbide-like species are formed.

The C 1s spectra obtained from *in situ* plasma treated BPDA–PDA indicated modification of the surface chemistry of the polymer. In Ar plasma, a typical graphitic-type carbon appeared on polymer. On deposition of Ta on this surface, C 1s peak appeared at 282.7 eV, and this was attributed to a metallic carbide species. The Ta 4f spectrum was consistent with this in that the $4f_{7/2}$ peak appeared at 22.9 eV, a shift of 1.2 eV up in binding energy from the metallic Ta. Hence the dominant interaction was attributed to Ta–C bond formation – possibly a stoichiometric TaC [83].

In $–NO_2$-group containing polymers, in the early stages of the interface formation, Cr was found to interact with nitrogen atoms of the $–NO_2$ groups of polymer, forming nitride-like species. N–O bond was broken as evidenced by the modifications occurring in the N 1s and O 1s spectra [68]. In studies of Al and Cr on PI, low binding energy N-products were attributed to nitride formation. In these cases stable nitrides exist. Chemical model studies using cyclic voltammetry and UV–visible spectroscopy of Cr on simpler polymers or monomeric model compounds which contained structural subunits of the polyimide indicated an initial rapid reaction with the carbonyl groups of polyimide, causing reduction of the dianhydride portion of the polymer, with concomitant chromium oxidation. Continued deposition of chromium onto the reacted polymer surface resulted in the formation of chromium carbide, oxide, and nitride [80] species disrupting the polymer chemical structure.

6.4.4 Oxidation

Both the metal and the polymer can undergo oxidation when they are in contact with each other. It appears that in most of the cases, the metal under consideration was Cu in contact with a wide variety of polymers. A lot of reports are available dealing with oxidative degradation of either the polymer or the metal or both. In cases where the metal is Cr or Ti, the oxidation reaction at the interface results in bond formation and in improving the adhesion. Here a few representative results concerning the oxidation of M/P systems are presented.

In general, many polymeric coating materials undergo oxidation degradation at an enhanced rate in the presence of Cu or Cu-compounds [86–94]. The catalytic effect on the kinetics of oxygen uptake by bulk PE and PP was measured by Hansen [86] who studied the reaction in the presence and absence of Cu powder dispersed in the polymer matrix. The proposed mechanism for the enhanced oxidation rate involves the reaction of cuprous Cu with hydroperoxides to form alkoxy radicals which propagate chain scission. Interfacial reactions between Cu (or Cu-oxide) and polyolefin films have been studied in detail by Allara and coworkers [87–90], primarily by infrared (IR) techniques. Their results indicate that Cu-carboxylates form at the Cu–polyolefin interface, which subsequently diffuse into the polymer matrix and catalyze further polymer degradation. Miller *et al.* [91–93] studied the oxidation of PP coatings on copper oxide surfaces by ion scattering profiles through the films before and after oxidation degradation.

By pre-oxidizing the Cu surface in a O^{18} environment, and then conducting the polymer oxidation in O^{16}, they noted an increase in the relative O^{16} content in the oxide film, which they attributed to the reduction of Cu-oxide by the polymer at the interface (followed by its re-oxidation by the O^{16}). Burrell *et al*. [94, 95] have reported a similar enhanced oxidative degradation of Cu in contact with more complex polymers such as poly (esterimide). Thus, the Cu–O–polymer reactions at the interface, and the reactions occurring within the polymer due to mobile Cu-species formed at the same interface contributed to catalytic degradation.

Similarly, when Cu/PI was formed by spin coating and curing of polyamic acid, Cu was oxidized [96]. The oxidation rate was found to be a function polymer coating thickness and the oxygen level in the curing ambient. Especially an oxidized Cu film was found underneath a thin PI film under high oxygen levels. Chambers and Chakravorty [97] have found that the oxidation of Cu surface began within an hour of the curing process. The culprit for this oxidation was trace contaminants of Cl and H_2O, which would react slowly with Cu surface by virtue of their low concentrations and diffusivities. This conclusion is in stark contrast with that drawn for the inverse system, Cu on PI, which has been shown to be essentially unreactive in vacuum over a time scale of several hours. Oxidation of Cu can be prevented by passivating the Cu with a continuous Cr film.

In general, O_2 plasma treated polymer surfaces result in the formation of metal–oxide bonds. These oxides in some cases improve adhesion, but in other cases disrupted the interface. The oxide formation was reported in many systems, one of which is Ta/PI [83]. –C–O and C═O bonds were found to be disrupted by the Ta deposition on O_2-plasma treated PI. In Ta 4f spectrum, the spin–orbit coupling was not well resolved due to the presence of many chemical states, including Ta-C (at 22.9 and 24.8 eV), Ta_2O_5 (at 25.7 and 27.6 eV) and intermediate sub-oxides. The O 1s spectrum exhibited a peak at 530.7 eV, which is characteristic of metallic oxide.

EXAFS of implanted Ti into PI (dose = 3.3×10^{17} atoms/cm^2, depth = 1000 Å) provides information on the bond formation [98]. The pre-edge peak shows a tetrahedrally coordinated Ti with a peak position corresponding to that due to titanium ethoxide. This suggested a Ti–O–C bonding configuration. This was later proved by XPS data of Ti deposited on PI showing an initial interaction with oxygen functionalities at low coverage, and the formation of metal carbides and nitrides at higher coverage.

Iwamori *et al*. [99] have reported the deterioration of Cu/PI after heat treatment at 150°C in air. The deterioration involved Cu_2O microparticles (10–100 nm) penetrating the PI substrate with both the substrate and film being oxidized. An interfacial layer of Ti or Co was found to be effective as barrier against the penetration of Cu_2O particles.

Interfacial oxidation of Cr or Ni involving PI may occur in one of the two likely ways: (a) formation of metal–oxygen–carbon complex with subsequent scission of C–N bonds; and (b) formation of a separate oxide phase at the interface following the breakage of C═O bonds. Assuming the formation of oxide phases to be the limiting case, an interesting criterion for oxide formation based on thermodynamic calculations was derived by Chou and Tang [100].

According to these authors, interfacial reaction will occur if $-\Delta G$ of the oxide of the metal selected is greater than 141 kcal/mol. Metals such as Al, Mg, Mn, Sn, Ti, and V, which have large heat of sublimation and heat of oxide formation, are expected to fulfill the criterion. If the intrinsic adhesive strength between the metal and the PI is the only consideration, the choice of metal would be quite straightforward.

6.4.5 Defluorination

Deposition of metals onto flouropolmers may cause both defluorination and the formation of organometallic species [101]. Roberts *et al*. [102, 103] and Vogel [104] have associated the defluorination of the Teflon upon metal deposition with increased metal adhesion. The formation of metal fluorides was reported for the deposition if some metals onto flouropolmers [105–107] and the fluorides were not found to contribute to bonding to the substrate. Wheeler and Pepper [108] suggested a possible mechanism, which involved the formation of C–metal–F chemical bonds. The interactions of Cr and Al with PFA (a copolymer of Teflon and perfluoroalkoxyvinyl ether) resulted in the formation of fluoride and carbide; the poor adhesion of PFA to Al was correlated to the negligible quantity of these compounds in Al/PFA system. Reaction of fluoropolymer with Al leading to Al-fluorideformation has been noted earlier [34].

6.4.6 Metal–conjugated polymer interaction

Unsaturated π-conjugated polymers can be doped to form semiconducting polymers. In applications such as Schottky or MIS diodes, interactions at the metal–polymer interfaces are a concern. Stafstrom *et al*. [109] investigated to which extent the delocalized π-electron system, which is responsible for the semiconducting properties, is disrupted by chemical interactions at the interface. Several π-conjugated polymers have been studied in the context of Al–polymer interactions. Aluminum interacts strongly with polythiophene and forms Al dimers on the polymer chain with a transfer of electronic charge from Al to the sulfur and α-carbon of thiophene ring. The geometry of the polymer is modified such that the delocalization of the π-electrons system is blocked. This, in turn, affects the semiconducting properties of the polymer. Similar results are reported in: (i) Al/DP7 (α,ω-diphenyltetradecaheptane) system [110] where Al interacts pair-wise with polymer chain (i.e. as a pair of atoms) breaking π-conjugation and twisting the polymer chain out of plane; and (ii) in Al/poly (aniline) systems [110] where Al atoms form a complex with the N═quinoid ring═N segments of the chain forming complex that strongly perturbs the π system and bond to the amine nitrogen sites.

6.4.7 Moisture absorption and permeation

Moisture absorption in ILD films creates reliability issues: stress, ionic charge carriers, instability of the dielectric constant, and source of moisture that may interact with underlying or overlying

metal. The required maximum water absorption is less than 1 wt%. Highly cross-linked polymers and fluoro polymers generally satisfy this criterion. Table 6.1 lists the observed moisture absorption for polymers for which data were available to this author.

Permeation of water through the polymer films is also of concern when such films are exposed to humid environments. Once again many polymers have low permeation rate, generally below 0.1 gm per Micrometer thickness of the film, per 100 cm^2 area per hour. Teflon, parylene N, PVC, polyethylene etc all have values lower than this value.

6.5 Adhesion at the metal–polymer interface

Table 6.3 summarizes the observed enhanced adhesion at the metal–polymer interface as a result of the deposition process related effects. Further enhancement in adhesion has been achieved by the surface treatments before deposition, either *ex situ* or *in situ* as summarized in Table 6.4. It is noted that in many of these cases the resulting adhesion is good enough to pass the so-called tape-peel test and therefore is expected to survive the chip fabrication, packaging, and in-use excursion of thermal and mechanical effects.

Table 6.3 Examples of process-affected chemistry-dependent metal–polymer adhesion

Metal	Polymer	Chemical compound	Technique employed
Cu (E)	PEI	Cu_2O [111]	XPS and AES
Cu (E)	ABS, PVA, Polystyrene	Cu-O–polymer complex [112]	XPS
Cr (E)	PI	Electron-rich carbide-like carbon species	XPS
Ti (S)	PI	Strong charge transfer via the carbonyl Group and a Ti–C bond formation [30]	XPS
CuCr alloy (S)	PI	Cr oxide [113]	AES and TEM
Cr, Ni (E)	PS, PVA, PEO, PMMA	Metal–oxygen chelate complexes (result of charge transfer) [114]	XPS
Cr, Ni (E)	PI	Metal–oxygen reactions [100]	XPS
Ag, Al, Au, Cr, Cu, Ni, Ti (E)	HDPE	Organometallic complexes [115]	XPS
Al, Cu, Ti, Ni (E)	PE	Polymer cross-linking [104]	XPS
Ti, Cr (E)	PTFE, FEP	Carbide-like bonding [107]	XPS

ABS = Acrylonitrile butadiene styrene; PVA = polyvinyl alcohol; PEO = polyethylene oxide; PS = polystyrene; PE = polyethylene; PMMA = polymethyl methacrylate; PEI = polyethylenimine; HDPE = high density polyethylene; PTFE = polytetrafluoroethylene; FEP = fluorinated ethylenepropylene; E = evaporated; S = sputtered.

Table 6.4 Polymer surface treatments used to improve the adhesion of polymers to metals

Metal	Polymer	Surface treatment	Technique employed	Reason for enhanced adhesion
Cu (S)	ABS	Oxygen plasma	XPS, IR(ATR), SEM	C–O–Cu bonds [116]
Al (E)	PP	N_2 plasma	SIMS, AES	Nitrogen–metal complex [117]
Al (S)	ABS	N_2 plasma	SEM, RES, and Profilometry	Surface sputter cleaning [118]
Al, Cr, Cu, Ni, and Ti (E)	HDPE	Ar-ion bombardment	XPS	Dehydration, increased cross-linking, C–H bond breaking, organometallic complex [115]
Cr (S)	BPDA–PDA	Ar or O_2 RF plasma	AES, peel test, X-ray analysis	Cr-carbides [77]
Metals	PP	Chromic acid	Peel test	Cr(III)–organic complex
Cu	PS	Nitric/sulfuric acid	Peel test	Carboxylic group–metal bond

PP = polypropylene, others are listed in Table 6.3 or in the text.

Although there are differences in the adhesion behavior of a metal on a polymer and a polymer on a metal, the adhesion is generally weak. Chemical bonding across the interface is expected to provide a good adhesion. This, however, may be challenged by stress in the films and substrate and by the process parameters (e.g. shear stress during CMP). Interface stability also plays important role in keeping of adhesion properties constant for a reasonable time. Near-interface changes of polymer properties due to diffusion and/or precipitation processes can affect adhesion. Small copper atoms can form different precipitates and clusters in polymers. The Cu/PI (see Section 6.4) near-interface regions can contain copper-related defects after thermal treatment, and copper can diffuse into the bulk of polymers. Short range diffusion (tens of nanometers) is however not expected to affect polymer properties and adhesion, unless strong clusterization occurs.

The role of oxygen on the adhesive bonding at the PI-on-metal has been examined [119]. Both PMDA–ODA PI and BPDA–PDA PI were cast and fully imidized on metal surfaces of Cu, Cr, Ni, Co, Cu/Ni, and Cu/Co in a nitrogen atmosphere. Very little or no change in peel strength was measured on all metals after annealing in nitrogen, while significant degradation were measured on all metals after annealing in air. The loss of PI adhesion to the copper surface was attributed to metal catalyzed thermal-oxidative degradation of the PI at the metal–PI interface, as was characterized by PI thickness reduction, Fourier transform infrared (FTIR) spectrometry and XPS. The rate of degradation of PMDA–ODA films on copper or cobalt was several times faster than that of the BPDA–PDA films. The degradation products were characterized as CO_2, CO, copper carboxylate salt and nitride moiety entrapped in partially degraded

PI films. The extent of degradation was found to increase with increasing oxygen content in the annealing ambient or with decreasing PI thickness, indicating that oxygen diffusion through the PI over coating to the PI–copper interface plays a critical role in causing of degradation.

Stewart *et al*. [120] investigated the PI-on-metal structure by using IR and XPS to study interfaces formed during the curing of the PMDA–ODA on gold, chromium, and copper. These data indicate that chromium and copper react with PI at the interface, resulting in reduced thermal stability of the polymer film. This thermal instability was stronger at the interface than in the bulk. The data showed that copper interacts with the polymer structure at the point where ring closure occurs to form the PI from polyamic acid. The formation of copper precipitates also was observed. Similar behavior was observed in the studies of PI–metal adhesion degradation by Anderson *et al*. [121].

Studies of the polymer-on-metal system, in general, do not demonstrate such dramatically changes in adhesion properties at the copper–polymer interface. Main properties of this interface are the weak interactions between the metal and the polymer. Often compound formation is not observed during growth of pure crystalline copper on polymer substrates. However, interface adhesions are properties strongly dependent on the beginning stages of the copper layer formation. The character of this stage and the subsequent growth and resultant adhesion properties correlated with initial structural conditions of polymer surface and its chemical activity.

Changes of adhesion properties for electron beam deposited copper-on-PTFE system has been examined by Kim *et al*. [122] using SEM, RBS, and XPS techniques. Polymer substrates were treated by either:

1. an oxygen ion-beam pre-sputtering with the ion energy of 500 eV, ion flux of 3×10^{14} ions/cm^2/s, and the sputtering time between 0 and 5 min;
2. an ultraviolet (UV) irradiation prior to metal deposition using an eximer laser with a wavelength of 248 nm; or
3. heat treatment for 1 h at temperatures of 300, 350, 375, 400, and 450°C after metal deposition.

In the first case the adhesion increased rapidly with an increase in sputtering time and reached an average value of 53 g/nm according to peel strength test (compared to 1–2 g/nm before sputtering). Similar behavior was found during Ar^+ ion sputtering [120]. The increase in interacting activity of copper with polymer was explained due to polymer surface cleaning and modification of the polymer structure mechanically and chemically. However, other studies [124] demonstrated that cleaning is not the dominant factor; instead, changes of morphology and chemical properties of surface are responsible for enhanced bonding. Ions make the surface more ‘crumbly’ as was observed in SEM photography [125], which produces active sites (dangling bonds, i.e. unsaturated places in polymer chains) with which copper actively interacts. These free radicals can be formed, for example, during ion-induced evaporation of fluorine atoms from polymer structure.

UV irradiation of the surface of polymer prior the metal deposition has also shown an enhancement in the adhesion. The adhesion increased as the irradiation fluence increased. The highest peel strength obtained using UV irradiation was about 16 g/nm, which shows that this treatment is less effective than ion-beam sputtering in enhancement of the copper–polymer adhesion; no changes in surface morphology were observed. One of the possible mechanisms is formation of the cross-linked or branched structure at the polymer surface, as was observed by Wheeler and Pepper [125] from X-ray irradiated samples of PI. Similar, changes in adhesion of copper to PTFE after treatment of PTFE polymer by pulsed UV eximer laser and metal deposition were reported in Ref. [126]. The interaction between the laser and the polymer was examined by characterizing the neutral and charged species emitted from the surface during irradiation. The nature of the species emitted indicated that significant chemical modification of the polymer surface occurs. In addition to chemical modification and in contrast to [125], changes in surface morphology were found. Irradiation at fluence 0.6 J/cm^2 results in an overall planarization of the surface, while irradiation at higher fluence results in the formation and enlargement of voids and localized melting. The enhancement of adhesion was significant for fluence >0.8 J/cm^2. Thus, bonding of copper on defect places (surface voids) is a reason for increase in adhesion.

Thermal treatments also cause changes in adhesion properties, but more complicated than that induced by ion-beam sputtering and UV irradiation. The adhesion was strongly dependent on the heat treatment temperature, which revealed a maximum peel strength of 35 g/nm after 1 h at 350°C. In contrast with other processes like ion-beam sputtering, this treatment does not involve the surface roughening or the ablation of polymer. The reason of enhanced adhesion by heat treatments was attributed to the increase in chemical interactions between metal and polymer at higher temperatures as well as changes in polymer properties such as wetability and crystallinity during heating. Since the bonding between copper and fluorocarbon polymers involves mainly metal–carbon interactions, increasing the temperature at the metal–polymer interface would promote such interactions and consequently contributes to the stronger bonding. The RBS analysis also indicated that copper diffused into polymer substrates during annealing. Increase of peel strength occurs near the melting point of PTFE (327°C).

Shonhorn and Ryan [128] reported that melting and crystallization of PTFE, in contact with a high-energy surface like gold, produced a surface region of high mechanical strength in the polymer and improved the wetability of PTFE. Further increases in temperature however, caused decrease in the adhesion, although the authors did not propose a clear explanation. Changes in polymer mechanical properties and the higher temperature may cause dissociation of copper–polymer bonds and stimulate out-diffusion of copper from the interface to the bulk of polymer.

The bonding structure of an amorphous fluoropolymer (AF 1600) with metals such as Al, Ag, Au, and Cu were examined using XPS in Ref. [129]. In the case of fluoropolymer/Al, both chemical reactions and intermixing of Al with fluoropolymer were observed. No chemical reaction was measured between AF 1600 and Ag, Au, and Cu. All XPS spectra of these metals as a function

of sputtering time were identical to that from pure metal. No thermal treatment was applied in this work to study diffusion of metals in fluoropolymer at different temperatures.

BCB polymers have demonstrated reliable adhesion (with adhesion promoter and/or surface treatment) to Cu, Al, and Au. No copper migration was reported during processing or high temperature and high humidity exposure during investigations of the feasibility of BCB/Cu interconnect integration. During plasma treatment (reactive ion etching), oxygen from this plasma reacts with BCB with the efficiency of the reaction depending on pressure and RF power. Reactions of copper with oxygen at the polymer–metal interface and in near-interface region can affect adhesion, suggesting a need of more complex and systematic investigation of diffusion and adhesion properties of copper to BCB.

The adhesion of the plasma enhanced CVD copper on parylenes (PAs) was examined by the peel-test and was compared to sputtered copper [130]. The adhesion of copper on PA-n polymer was also studied using 350°C thermal annealing cycles. Both CVD-deposited copper and sputtered copper demonstrate good adhesion properties for Cu/PA-n films without any special features. The PIB-deposited Cu has relatively good adhesion to PA. However, the adhesion between copper and PA-n deteriorated when annealed beyond 300°C, with oxygen-plasma treated PA found to have better adhesion to copper than an untreated surface. This treatment formed a mixed layer and created damage in the polymer, both of which enhanced the copper active bonding with polymer [130, 131].

Bonding of Cu/Cr films to several polyamides has been studied as a function of polymer surface modification by ion beam and chemical pre-treatment [129]. It is found that for PMDA–ODA polyimides systems, exposure to low energy (200 eV) Ar^+ and/or O_2^+ ions improves adhesion to the metal overlayer (role of O_2^+ is not understood in terms of adhesion improvement [129]). The fracture location is found to lie 2–3 nm within the polymer, depending upon the ion beam dose and the specific polyimide employed. However, in other studies [132], polyimide film after O_2^+ etching also has enhanced adhesion to copper films. The adhesion of evaporated copper on the modified by O_2^+ surface was substantially increased. The effect of ion bombardment on polyimide have been studied using XPS techniques (energies of irradiation from 0.5 to 1.0 keV, doses from 8×10^{13} to 10^{15} ions/cm^2 [133]. Irradiation of the surface improved adhesion of Cu to polyimides.

Enhancement of the adhesion of thin copper films on fluoropolymer substrates was found when the substrate was irradiated with a pulsed UV eximer laser prior to metal deposition [134, 135]. Ion-beam modification of surface can change bonding interactions and bonding structure of polymers/metal/substrate-layered structures. Bonding at the initial coverages of the copper was well described by the formation of metal to the polymer unit. The adhesion energies of several interfaces show a good overall correlation to chemistry to the microstructure and adhesion characteristic of the metal/polymer interface. Modifying the thin polymer films or substrate cause change in adhesion properties of polymer/metal film stacks [136]. Similar results were obtained for downstream microwave plasma modification of polymer surface [137].

6.6 Self-assembled (polymer) molecular films

Recently the use of ultra-thin films of self-assembled monolayers (SAMs) comprised of molecules as small as ≈ 2 nm, as adhesion promoter/diffusion barrier has been demonstrated [138]. SAMs are generally organic molecules that self-assemble on a surface (from a liquid or vapor phase) to form a monolayer of the film [139, 140]. The use of SAMs as capacitors in molecular electronics devices has been shown [141]. They are likely to produce good step coverage because of the high probability of one end of the molecules sticking to the substrate, and the low tendency for multilayer formation. A few examples of SAM molecules of interest in Cu-technology are listed in Table 6.5. These SAM molecules have one common functional trimethoxysilane group, –Si–$(OCH_3)_3$, which tethers to the SiO_2 substrate and thus provides a bonding.

Krishnamoorthy *et al*. [138] have demonstrated the use of SAMs as an adhesion promoter/diffusion barrier between Cu and SiO_2 by examining Cu/SAM/SiO_2/Si capacitors for their *C–V* and *I–V* behavior. Comparison of the *C–V* and *I–V* characteristics of the MOS structures with and without a SAM at the Cu/SiO_2 interface indicates that certain SAMs inhibit Cu diffusion into SiO_2. Figure 6.14 shows representative normalized-capacitance ($C/C_{maximum}$) verses gate voltage plots for a control sample and a SAM1-coated MOS structure prior to BTA (annealing time $t_{BTA} = 0$ min), and at failure. The flatband (FB) voltage of the control sample $V^{FB}_{control}$ shifts to lower values with increasing t_{BTA}. Such shifts in V^{FB} accompanied by an increase in leakage current density $j_{leakage}$ are characteristic signatures of Cu-ion diffusion into SiO_2 [142]. The control samples failed ($j_{leakage} > 1000$ nA cm^2) at ≃150 min, at which point the flatband voltage shift $\Delta V^{FB}_{control}$ was ≃18 V. At the same t_{BTA}, SAM1-coated samples showed significantly smaller changes: $V^{FB}_{SAM1} < 1.5$ V and $j_{leakage} \simeq 10$ nA/cm^2 (see Fig. 6.15) and failed only at 650 min – a four-fold increase in the time to failure.

Figure 6.15(a) shows ΔV^{FB} plotted as a function of t_{BTA} for control and SAM1-coated samples. $\Delta V^{FB}_{control}$ increases with t_{BTA} rapidly [d(ΔV^{FB})/dt ~ 0.11 V/min] and continuously all the way to failure. But, ΔV^{FB}_{SAM} remains relatively unchanged at ≃1.5 V with only a marginal increase of ≃0.0029 V/cm until failure, at which point ΔV^{FB}_{SAM} increases to ≃5 V. The leakage current density $j_{leakage}$ also shows similar characteristics [see Fig. 6.15(b)]. In the control sample,

Table 6.5 Chemical fromulae and nomenclature of the SAMs

Molecule	Chemical formula	IUPAC Name
SAM1	 CH_2-CH_2-Si-$(OCH_3)_3$	3-[2-(Trimethoxysily) ethyl] pyridine
SAM2	 CH_2-CH_2-Si-$(OCH_3)_3$	2-(Trimethoxysily) ethyl] benzene
SAM3	CH_3-CH_2-CH_2-Si-$(OCH_3)_3$	*n*-Propyl trimenthoxysilane
SAM4	 Si-$(OCH_3)_3$	Phepyl trimetholysilane

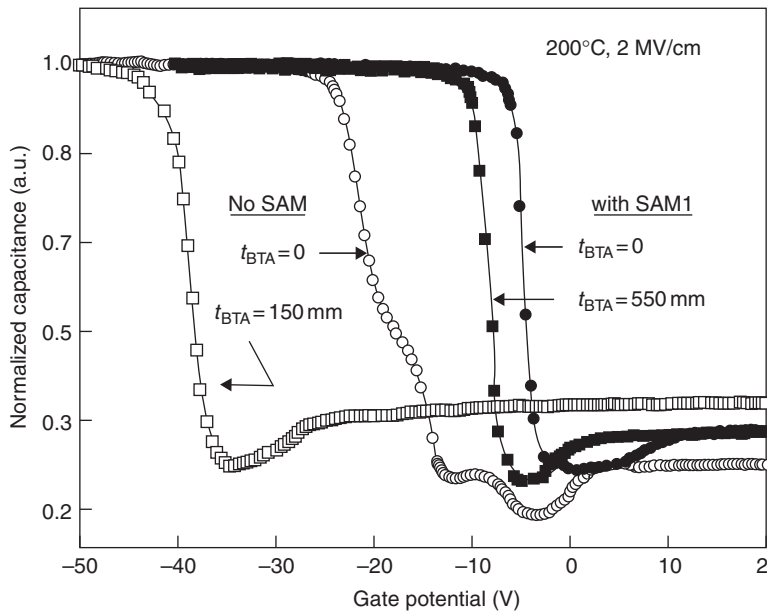


Fig. 6.14 Representative *C–V* curves from a control sample (open legends) and a SAM1 coated MOS structure (filled legends) obtained prior to BTA (bias temperature annealing |equiv| bias temperature stressing) and after BTA at failure. From Krishnamoorthy *et al*. [138].

$j_{leakage}$ continuously increases at a rapid rate, while in the SAM-coated sample a relatively constant $j_{leakage}$ value of $\simeq$10–30 nA/cm^2 persists right until failure, when it abruptly shoots up to values $>10^5$ nA/cm^2. We note that at t_{BTA} corresponding to the failure of the control sample, $j_{leakage}$ in SAM1-coated samples is more than four orders of magnitude smaller.

The success of a given SAM, in this case SAM1, was explained in terms of the size and the molecular chain length. The larger volume (compared with, for example, aliphatic groups) occupied by the aromatic rings sterically hinder Cu diffusion between the molecules through the SAM layer. SAMs with long chain lengths screen Cu atoms from the influence of the SiO_2 substrate, thereby preventing ionization and consequent acceleration by the externally applied electric field. The Si–$(OCH_3)_3$ head group is unlikely to play any significant role in hampering Cu diffusion because the Si–O–Si linkages they form – to tether the SAMs to the substrate – are similar to those in SiO_2. While the mechanism by which the SAMs eventually fail (at 650 min in Fig. 6.15(b)) is not clear from our experiments, the probable cause is the development of defects such as pinholes [142] at the interface.

It is apparent from these findings and the research in molecular electronics that polymers hold many opportunities that need to be carefully evaluated and linked to a given set of polymers, including those for ILD applications.

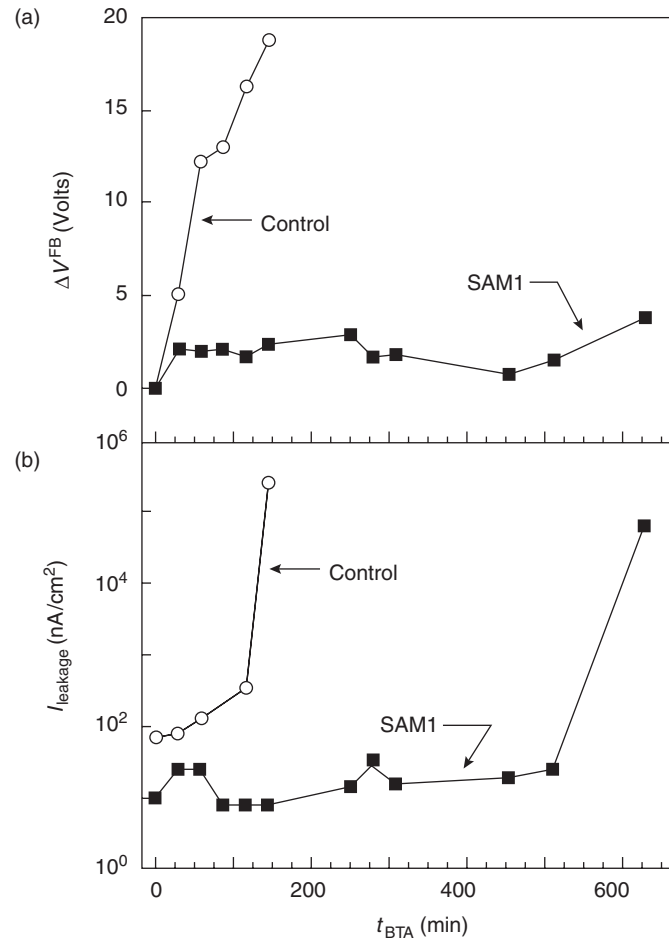


Fig. 6.15 (a) Flatband voltage shift, ΔV^{FB} and (b) leakage current density, leakage, plotted as a function of t_{BTA} for control and SAM1 capacitors. From Krishamoorthy *et al*. [138].

6.7 Summary

Polymers are attractive for application as interlayer dielectrics because of their potential of having low dielectric constant by virtue of being light-element-materials. This chapter has briefly examined polymer types and type-dependence on the dielectric properties. Besides the needed low-κ, the polymers must be processable in a multilevel interconnection scheme and reliable during and after processing. This chapter, therefore, examines the stability of the polymers and their structures, interaction with surrounding materials, adhesion, and impact on electrical properties and their characterization. Besides Cu, other metals have been investigated in contact with polymers and they all have been considered and reported, as necessary, in this

write up. A brief introduction to self-assembled monolayers of organic materials is also presented.

It is apparent that there is considerable effort being expended in finding a really low-κ polymer. From simple homo-polymers to a variety of copolymers have been synthesized and tested. When aiming for a low dielectric constant material, it becomes quickly apparent that a compromise on thermomechanical properties becomes essential. One may have to take some unconventional approach (voids in material is one of them) to achieve the desired characteristics in one material.

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Chapter 7
Chemical vapor deposition of C–F low-*k* materials

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Abstract

C–F low-*k* interlayer dielectric materials, deposited by plasma-enhanced chemical vapor deposition (PECVD), are the subject of this chapter. Low-*k* film properties as well as film deposition rate can be controlled easily by plasma process parameters. Properties and integration issues of an organic PECVD polymerized material, consisting mainly of carbon, fluorine, and hydrogen, will be discussed with respect to the semiconductor industry requirements. The lowest dielectric constants ($k \approx 2.0$), ever measured on nonporous materials, were reported from this plasma deposited material group. Other electrical film properties (leakage current density and break down field strength) show excellent values too. Unfortunately, insufficient adhesion of CF dielectric materials is reported in literature. As described in this chapter, the insertion of an *in situ* deposited, very thin additional adhesion promoting layer offers excellent adhesion to technology relevant films. The influence of the adhesion layer on dielectric film parameters could not be measured or is negligible. Plasma-induced cross-linking in the low-*k* material is responsible for high thermal and mechanical stability of the dielectric films. Its mechanical stability and inertness to solvents, water, and different chemicals are the basis for polishing the dielectric by chemical–mechanical polishing (CMP) process. Both, CMP and good patterning ability, are required for use of the CF polymer dielectric in a Damascene structure, combining low-*k* insulator with copper lines. Due to the compatibility of CF low-*k* dielectric deposition and patterning with present IC technology, CF polymers, deposited by PECVD process are promising candidates for later application as low-*k* interlayer dielectric.

7.1 CVD low-*k* material survey and requirements

Based on the well-known low dielectric constant of the organic material polytetrafluoroethylene (PTFE) the search for new insulating materials for thin film deposition in metallization technology started with intensive investigations in 1993 [1]. As a result, a huge variety of materials designed and investigated with respect to a later application as low-*k* intermetal dielectric material was presented in literature. The main deposition processes for low-*k* film deposition are summarized in Fig. 7.1.

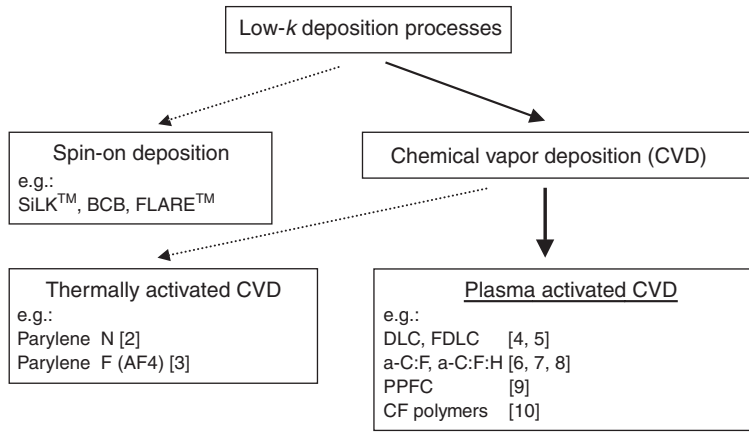

Fig. 7.1 Low-*k* deposition processes for carbon-based materials.

With respect to the deposition technique these materials can be separated into spin-on and CVD materials. Spin-on dielectrics are described in the Chapters 5, 6, 8, and 9. CVD materials, not based on the chemical element silicon, can be divided into two classes [11]:

- organic films, deposited by thermal CVD
- amorphous or polymeric films deposited by PECVD.

Examples for *organic films deposited by thermally activated CVD* are the parylenes. Parylene is a pseudo-crystalline family of materials [12]. In the film deposition process a solid precursor with low melting point, consisting of molecular dimers, decomposes in a high-temperature pre-reaction chamber. In presence of a carrier gas, the parylene monomers enter the deposition chamber and condense on the cooled substrate (temperature below 0°C) where the polymerization and crosslinking process takes place. Parylene monomers are very reactive diradicals, and thus, no higher wafer temperatures are required for the process. Parylene N or poly(*p*-xylylene), $-[CH_2-C_6H_4-CH_2]-$, and parylene F, $-[CF_2-C_6H_4-CF_2]-$, in which all of the methylene groups are replaced by difluoromethylene, achieve values of the dielectric constant of 2.6 and 2.4, respectively [2, 13]. Wary *et al*. [3] presented $k = 2.28$ for parylene F (AF4). After the deposition an annealing process up to the temperature of later application is required. Parylenes have high thermal (400–450°C) and chemical stability but unfortunately poor adhesion to other films. The pseudo-crystalline structure of the material causes orientation dependent optical and electrical properties. The dielectric constant of AF4 varies from 2.1 (out-of-plane) to 2.4 (in-plane). This anisotropy will limit the use of AF4 in a damascene architecture.

This chapter will focus on *carbon-based low-k materials, deposited by plasma enhanced chemical vapor deposition*. In literature these materials are also named as fluorinated amorphous

carbon a-C:F [6, 36], diamond-like carbon (DLC), hydrogenated DLC, fluorine containing DLC (FDLC) [4, 5], plasma-polymerized fluorocarbon PPFC [9], fluorinated amorphous- carbon, a-C:F:H [8], amorphous carbon fluoride, a-CF [12]. All these amorphous or organic materials (in this case the difference between amorphous and organic is not quite clear in literature) are deposited by PECVD processes from C and a selection of F, H, and O containing precursor gases.

Grill and coworkers [4, 5] from IBM deposited DLC layers from pure hydrocarbons and FDLC from fluorinated hydrocarbons or mixtures with hydrogen in a RF parallel plate reactor. The dielectric constant, internal stresses and the thermal stability of DLC films decreased with decreasing RF power and increasing pressure. If fluorine was added to the precursor gas, stress and dielectric constant decreased and thermal stability increased. Conclusions from these results are that the properties of plasma deposited DLC films can be controlled easily by changing the plasma process conditions and that the addition of fluorine to the precursors has a beneficial influence on the low-*k* film properties.

Endo and coworkers [6, 14] from NEC deposited low-*k* layers from typical fluorocarbons (CF_4, C_2F_6, C_4F_8 and their hydrogen mixtures) in a parallel plate PECVD reactor too. Low-*k* films with $k = 2.1$ were deposited from a CF_4/CH_4 gas mixture. It was found that the creation of an amorphous C–C cross-linked structure is necessary to increase the thermal stability. Using C_4F_8 precursor gas in a high density helicon plasma, film adhesion and deposition rate could be increased. Additionally Matsubara *et al*. [15], designed and tested a low-*k*/Cu damascene architecture with a-C:F low-*k* material and copper metal lines.

Among different candidates for low-*k* materials, amorphous carbon fluoride is one of the more promising low-*k* materials with stable *k* value down to 2.3 as reported by Korczynski [12]. CF polymers are organic aliphatic or cyclic molecules consisting of the elements carbon, fluorine, hydrogen, and oxygen. Due to the weak tendency to polarize in external electrical fields these materials can achieve low dielectric constants. The lowest dielectric constant that has ever been measured on bulk polymer materials was achieved by PTFE ($k \approx 1.9$–2.1 [16, 35]). To remind, SiO_2 usually applied as dielectric material in semiconductor device fabrication has $k \approx 3.9$–4.2 depending on the deposition process.

In general, three possible ways exist to reduce the permittivity of a material. If it would be possible to decrease the density of the material (lower density causes a lower number of bonded atoms that can be able to polarize), the value of the dielectric constant would decrease in the same manner. A general rule for designing new polymer dielectric materials is to avoid straight polymer chains that can be able to arrange very close to each other. Thus, the material has a relatively high density and often inhomogeneous physical properties. Steric rearrangement of atoms or atom groups inside the molecule can reduce the number of atoms in a given volume and thus the density decreases too. An increased steric hindrance of polymer molecules can be achieved by shortening the polymer chains and adding a certain number of side chains to

Table 7.1 Selection of PECVD deposited CF dielectric materials with low *k* values, recently published from different companies and institutions

Reference	*k* value	Deposition process	Company/institution
Endo *et al.* [14]	2.1–2.85	PECVD	NEC Corp., Japan
Uhlig *et al.* [10]	2.0–2.7	PECVD	Chemnitz Univ. of Technol., Chemnitz, Germany
Han and Bae [18]	2.4–3.6	PECVD	Korea Adv. Inst. of Sci. and Technol., Taejon, Korea
Shieh *et al.* [19]	2.3	PECVD	Nation. Chiao Tung Univ., Hsinchu, Taiwan
Agraharam *et al.* [20]	2.23–2.55	PECVD	Georgia Inst. of Technol., Atlanta, USA

the molecule. Furthermore, as published by Xu *et al.* [17], the *k* value can be reduced by making the organic dielectric material porous. Examples for these porous materials will be described more in detail in Chapters 8 and 9. Another idea to reduce *k* is the substitution of atoms or parts of the molecule by atoms or atom groups with lower tendency to polarize. Usually organic polymers consist of a high amount of C–H, C–O, O–H, and C–C bonds. Especially the O–H and the C–H bonds have a relatively strong tendency to polarize in external electrical fields. Thus, these bonds should be replaced by, for example, C–F bonds with lower polarization behavior. Because of this theoretical background, amorphous fluorocarbon polymers should have the potential to become a dielectric with low *k* value. Recently a certain number of papers dealing with amorphous fluorocarbon low-*k* materials was published. A selection of publications including the results for the dielectric constant is presented in Table 7.1.

The application of CF polymers in damascene interconnect process flow (see Section 7.4.1) requires, in addition to the low-*k* values, the knowledge of further material characteristics. The most important properties of amorphous CF polymers with respect to the semiconductor industry requirements for low-*k* material are summarized in Table 7.2.

As generally agreed, all organic polymers suffer from their relatively low thermal stability. It is known that a high degree of cross-linking increases the thermal stability of organic materials [22] and its mechanical stability [8]. To summarize the demands, polymer materials designed for intermetal dielectric (IMD) application must consist of nonlinear, highly cross-linked polymer chains, formed by strong bonds with lowest tendency to polarize. Such a material will combine the most important low-*k* material properties: low dielectric constant, high thermal and mechanical stability.

Table 7.2 General properties of amorphous CF polymers in comparison to Semiconductor Industry requirements (summary from: SIA Roadmap [21])

IMD material requirements	General CF polymer evaluation[a]	Comments of PECVD CF polymers
Low *k* value	+	
High thermal stability	− (low decomposition temperature)	Sufficient for further processing
Low number of charges in bulk material	+	
Sufficient mechanical stability (for CMP)	O,− (elastic, soft)	Stable enough for CMP
Good adhesion to neighboring layers	− (Teflon™-like)	Excellent adhesion using special adhesion layer (see Section 7.3.1)
Low moisture uptake	+	
High resistance against acids, bases, solvents	+	High resistance against solvents, CMP chemicals
Good conformity with materials used in IC fabrication	+	
Good conformity with established process technology and equipment	+	

[a]Evaluation of CF polymer dielectric: + = good; O = medium; − =bad.

7.2 Chemical vapor deposition process

At present two approaches are employed for the deposition of low-*k* CF polymer films: Chemical vapor deposition (CVD) and spin-on. SPEEDFILM™, a spin-on deposited CF polymer, is described by Rosenmayer *et al*. [23]. The CVD process seems to be the mainstream regarding CF polymer application as low-*k* IMD material.

7.2.1 Fundamentals of PECVD

Using organic precursor materials (usually gases or evaporated liquids) as initial materials for the polymerization process, typical CVD temperatures are sometimes relatively high. The organic precursors would be destroyed or no polymerization on the wafer surface would take place because most organic polymers can not survive the elevated temperatures. An other way to deliver the energy for the polymerization process is to perform the reaction under plasma conditions in a so-called plasma-enhanced chemical vapor deposition (PECVD) process.

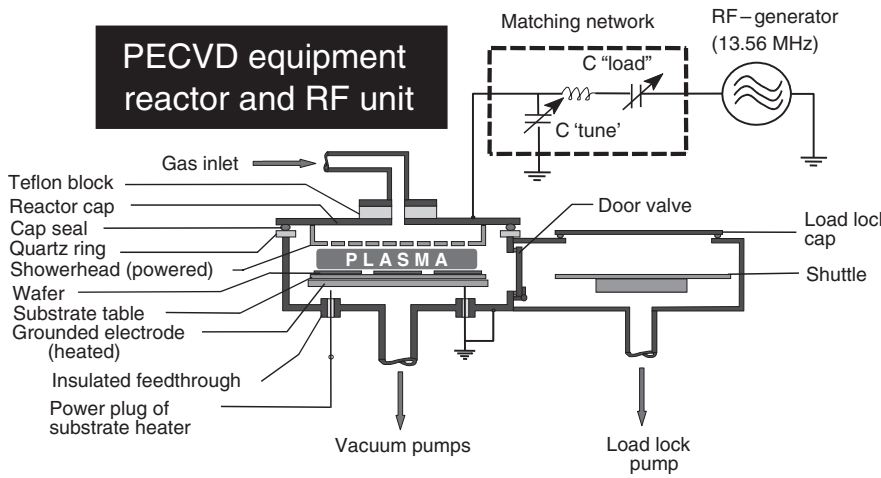

Fig. 7.2 Schematic of a PECVD deposition tool.

Generally, chemical reactions require a certain amount of energy for the dissociation of the precursor materials and the following formation of the desired material of the deposited layer. Thermal CVD delivers the energy by heating up the wafer surface. In PECVD the precursor materials receive a high amount of reaction energy by collisions with highly accelerated particles (electrons accelerated up to energies of some electron volts, and ions) and decompose into various components (atoms and molecules in ground and excited states, electrons, ions and free radicals). These highly reactive fragments (gaseous) deposit on the relatively cold wafer surface (solid) in a heterogeneous chemical reaction by formation of a new film material. On the other hand certain materials with special properties can only be fabricated under plasma conditions. PECVD is a special type of low pressure CVD. In contrast to thermal CVD, the energetic conditions for the polymerization can easily and fast be tuned by changing the plasma parameters (power, pulsed plasma). It offers a high flexibility in controlling the polymerization process and thus in changing the properties of the deposited polymer films. Figure 7.2 shows a typical PECVD deposition tool.

The substrate (wafer) can be loaded into the plasma reactor chamber from an evacuated load lock system. Both reactor and load lock are connected to the vacuum system. The gas inlet unit controls the precursor gas mixture and the precursor gas flow into the plasma reactor. For special applications it is advantageous to have a heated or cooled substrate table (chuck). The radio frequency (RF) generator supplies the high frequency (i.e. 13.56 MHz) or low frequency (some hundred kilohertz) voltage for the plasma chamber. To achieve a maximum RF power transmission from generator to reactor a matching unit is inserted. Different types of plasma sources are used in PECVD reactors. They can be divided into two mean groups, the RF plasma sources (capacitively coupled plasma, CCP; inductively coupled plasma, ICP; in direct or remote use)

and microwave plasma sources (electron cyclotron resonance plasma ECR, microwave downstream plasma MWDS).

7.2.2 Plasma polymerization process – a special PECVD process

Plasma polymerization is a thin film forming process where monomers are converted into polymers directly on the surface of a substrate. The reaction takes place in presence of plasma to deliver the polymerization energy. In some cases the plasma polymerization process is supported by elevated substrate temperatures. Gaseous precursors (plasma activated monomers) react on the solid substrate surface to form a new material, for example, a polymer (heterogeneous reaction).

Monomers polymerized by catalytic breaking the C═C double bonds have a more straight structure with straight polymer chains. Plasma polymerized materials are highly cross-linked. The high degree of cross-linking causes a higher stiffness and a higher thermal stability of the polymer material [24]. These two properties are desirable for the application of the polymer as intermetal dielectric material. A principal reaction mechanism for plasma polymerization is depicted in Fig. 7.3.

In a glow discharge, the precursor gases (e.g. C_4F_8 and CH_4) dissociate into highly reactive fragments. These activated fragments receive additional energy from heating up the substrate (kT), interaction with photons energy (hf), and from the bombardment by ions and other charged particles, accelerated in the plasma field. The implemented energy causes the polymerization process on the substrate surface. This special PECVD process is able to form highly cross-linked CF(H) polymer structures.

7.2.3 Equipment and special requirements for CF polymer deposition

Special results for CF polymer deposition are described within this section. The investigated CF polymer films were deposited on 6 in. silicon (100) wafers by PECVD using a single wafer

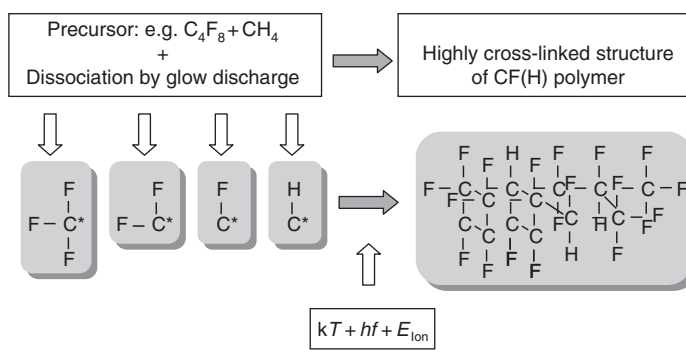

Fig. 7.3 Scheme of CF plasma polymerization process (PECVD).

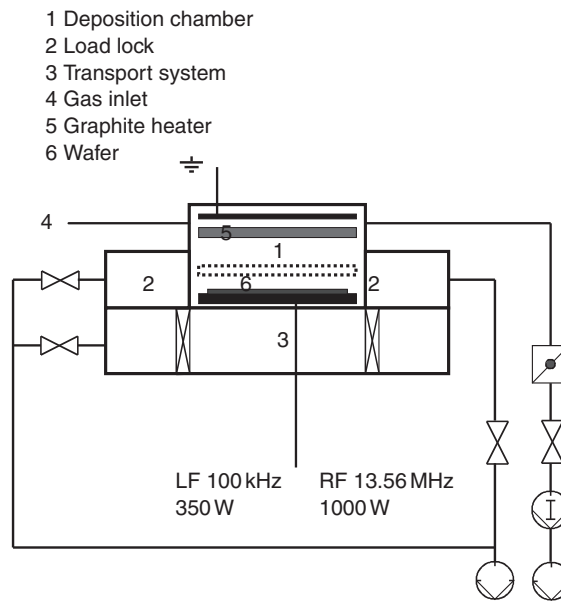

Fig. 7.4 Schematic of a commercially available etch tool (Tegal 1514e) used for CF polymer deposition, additionally equipped with heating system.

plasma system. The wafers were coated in a dual frequency (RF 13.56 MHz, 1000 W and LF 100 kHz, 350 W) modified Tegal R&D system. To enable elevated deposition temperatures (20–400°C), the Tegal system was equipped additionally with a graphite heater placed within the deposition chamber (see Fig. 7.4).

Mixtures of different perfluorated hydrocarbons (CF_4, CHF_3, C_2F_6, C_4F_8) in combination with CH_4, H_2, N_2, He, and Ar were used to produce thin films. The deposition temperature (temperature on the wafer surface) has been varied from room temperature up to 250°C. Usually a 150–300 W RF plasma supported by a 0–150 W LF plasma was applied to the parallel reactor plates. Inside the reactor the deposition pressure (0.3–0.5 Torr) was controlled by changing the position of a throttle valve placed in between the reactor and the vacuum system, and the precursor gas flow (2–60 sccm), adjusted by mass flow controllers. The deposition rate of the CF polymer layers could easily be varied from 200 to 1000 nm/min depending on the process parameters [25]. A deposition rate of about 400 nm/min was preferred offering an acceptable compromise between deposition time, wafer-to-wafer film thickness uniformity and deposition requirements from semiconductor industry. Figure 7.5 gives an overview about the process parameters having a strong influence on the deposition process and thus the properties of the deposited CF polymer layer itself.

As an example the influence of the normalized precursor gas flow on the deposition rate is shown in Fig. 7.6.

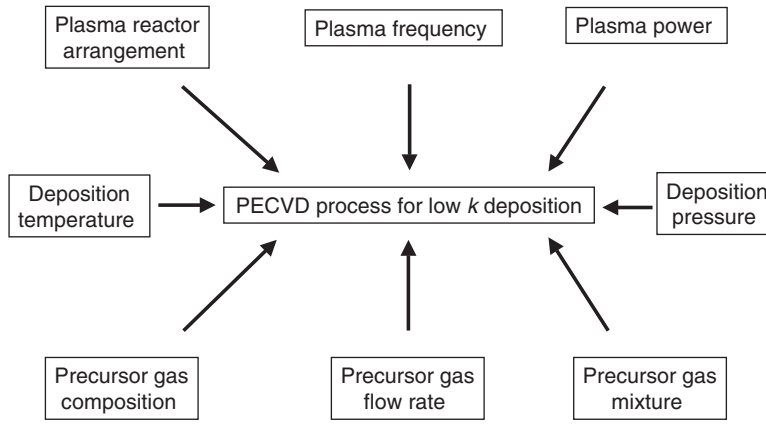

Fig. 7.5 Influence of process parameters on CF polymer deposition.

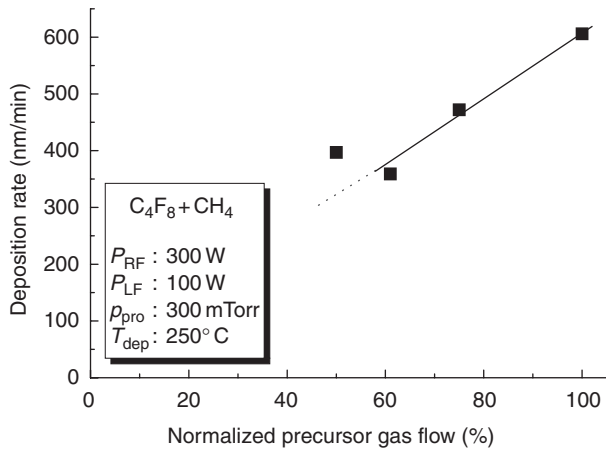

Fig. 7.6 Film deposition rate of CF polymers deposited at different normalized precursor gas flows.

Normalized precursor gas flow is the actual flow compared to the maximum flow. The deposition rate of CF polymers can be changed widely by varying the precursor gas flow. For a fixed set of process parameters (plasma power, temperature, pressure, precursor gas mixture), the deposition rate lowered from about 600 to about 350 nm/min when the precursor gas flow was reduced to about 60%. Instable plasma conditions in the deposition chamber prevent a further reduction (less than 60%) of the normalized precursor gas flow. That is the reason why the deposition rate shows a deviation from normal behavior for low precursor gas flow rates. An increased RF plasma power also causes a higher deposition rate (see Fig. 7.7).

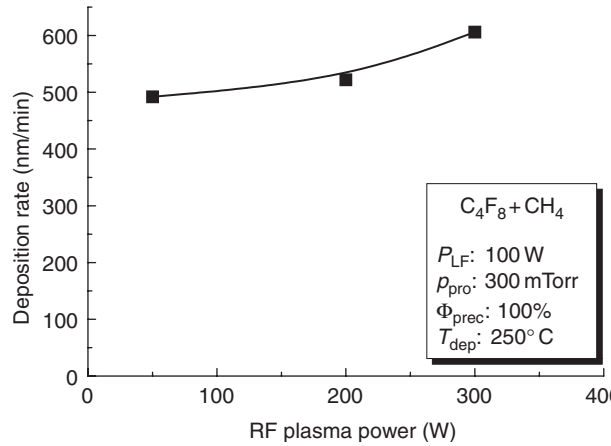

Fig. 7.7 Film deposition rate of CF polymers deposited at different RF plasma power.

Other dependencies how the deposition rate can be adjusted by process parameters are not reported here more in detail because all deposition parameters strongly depend on the equipment used. In general the deposition rate for CF polymer deposition can be increased by increasing LF plasma power, process pressure, and CH_4 content in the precursor gas. However, increasing the deposition temperature ($T > 100$°C) reduces the deposition rate. This result is in contrast to other PECVD processes. The reason is that at elevated temperatures the highly reactive fluorine radicals will etch the deposited CF polymer layer more efficiently and thus the deposition rate decreases [19].

The adhesion of deposited CF films to the underlayer and to layers deposited on top of the low-*k* material is unfortunately unacceptably low. It seems to be a general problem for CF polymer layers. As reported by Tanaka *et al.* [26], CF polymer films have very smooth surfaces covered with fluorine atoms and thus low adhesion. Matsumoto and Ishida [9], Ariel *et al.* [27] as well as Han and Bae [28] discussed this problem too. But an excellent adhesion of all stacked layers is required to achieve sufficient mechanical stability and to avoid delamination during the fabrication of the IC device before the final encapsulation. An essential improvement of adhesion could be observed after the insertion of a very thin carbon based adhesion layer, previously described by Uhlig *et al.* [25]. No additional equipment is necessary to deposit the adhesion layer before and after CF polymer dielectric deposition. Without breaking the vacuum, the adhesion layer (thickness 5–10 nm) can be deposited by PECVD from CH_4 precursor gas in the CF polymer deposition tool. The deposition of the amorphous CH adhesion layer requires elevated deposition temperatures (up to 300°C) and an RF plasma power of more than 300 W. Compared to the CF polymer deposition rate the deposition rate of the CH adhesion layer is very low (about 10 nm/min). Because the film can be very thin and the deposition can take place within the CF deposition chamber, no time consuming additional process step is necessary. A further

advantage is that the adhesion layer can be deposited from a precursor gas already used for CF polymer deposition. No cleaning step between CH and CF deposition is required.

7.3 Film properties of CF polymers

In the following sections a selection of CF polymer properties is described with respect to an application as intermetal dielectric in IC fabrication. All the polymer films, investigated to determine their mechanical, electrical, optical, and surface properties and their thermal stability, were deposited with a film thickness of 400–500 nm from a C_4F_8/CH_4 precursor gas mixture on 6 in. silicon (100) wafers by using the experimental setup described in Section 7.2.3.

7.3.1 Mechanical and surface properties

7.3.1.1 Film adhesion to substrate

Concerning the demands of employing the CF polymer dielectric in damascene architecture (see Section 7.4), the adhesion of the CF polymer films to different etch stop, cap, barrier and lithography mask layers was investigated. Without the CH adhesion layer, enclosing the amorphous CF polymer, in every case the X-cut tape test (according to the American National Standard ASTM) failed or showed low adhesion strength. When the adhesion layer was inserted in between CF polymer and underlayer, an excellent adhesion was achieved. The results for film adhesion of different layer combinations are summarized in Table 7.3.

Table 7.3 Tape test adhesion evaluation of CF polymer dielectric to adjacent materials with and without adhesion layer

Material/film	Peeling evaluation[a]	
	Without adhesive layer	With adhesive layer
Si	0	5
SiO_2, SiN	0	5
TiN, TiW, WN	0	5

ASTM tape test, performed with tesa® tape 4130 (adhesion force 10 N).
[a]0: total peeling, 5: no peeling [10].

7.3.1.2 Surface roughness

The surface roughness of annealed and not annealed CF polymer samples was determined from atomic force microscope (AFM) pictures. In Fig. 7.8(a) and (b) the AFM plots of as-deposited and annealed (400°C) CF polymer samples are shown.

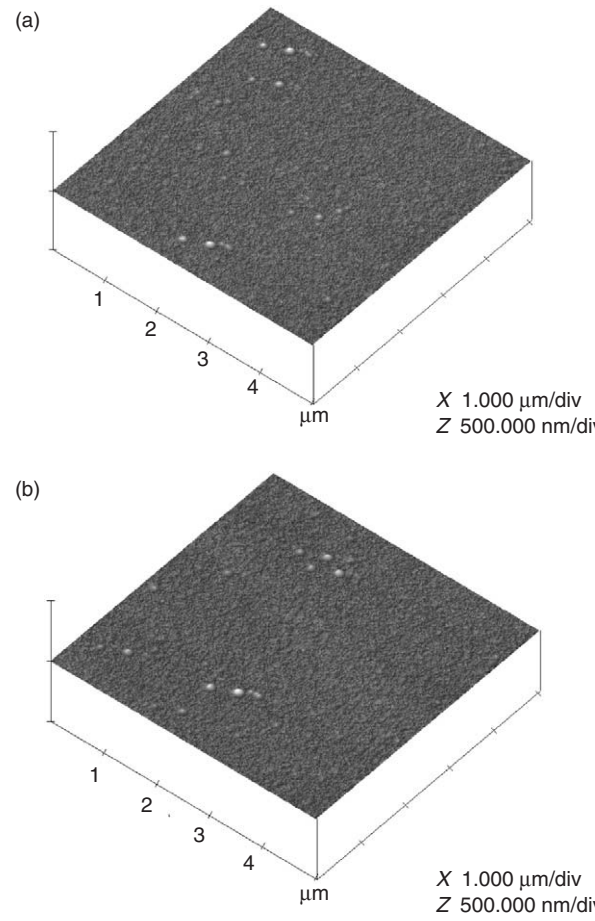

Fig. 7.8 (a) AFM plot of CF polymer (as-deposited). (b) AFM plot of CF polymer surface (annealed at 400°C in vacuum) [29] (© 2001 IEEE).

No changes of surface roughness after thermal cycling up to 400°C in vacuum could be observed. In all cases RMS (mean) surface roughness was less than 1 nm. SiO_2 films deposited by thermal oxidation have equivalent roughness [29]. Similar CF polymer layers deposited and investigated by Matsumoto and Ishida [9] have significantly higher values of roughness (about 100 nm) obviously depending on the deposition parameters.

7.3.1.3 Mechanical stability

All low-*k* materials have a relatively low mechanical stability (low hardness and stiffness). Organic polymers in most cases, are soft and flexible. Fortunately, according to Jacobsohn *et al.* [8], CF polymers deposited by PECVD are harder and have a higher stiffness compared

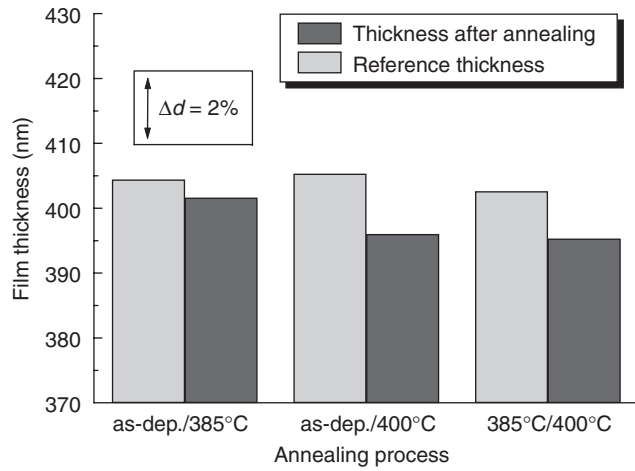

Fig. 7.9 Thickness change of CF polymer films annealed 30 min at highest temperature in vacuum [29] (© 2001 IEEE).

with CF polymers deposited from the same materials by thermally activated polymerization due to their higher degree of cross-linking. Sufficient hardness is required especially for CMP processing (see Section 7.4.2).

7.3.1.4 Thermal stability

Thermal stability was tested by measuring the polymer film thickness before and after the annealing process. That means the film shrinkage of the intermetal dielectric may not exceed 5% within the temperature range. In Fig. 7.9 the shrinkage of the investigated CF polymer is shown.

Up to a temperature of 385°C, the dielectric film shrinkage is negligible and remains within the detection limit (lower than 0.5%). At annealing temperatures higher than 385°C a slight increase in film thickness change can be detected, but will not exceed 2% in film thickness loss. The annealing investigations offer promising results regarding the thermal stability of the CF polymer dielectric up to 400°C. CF films, deposited at elevated temperatures, show increased thermal stability [10, 30, 34].

7.3.2 Electrical properties

The electrical measurements (determination of dielectric constant k, leakage current density I_{leak} and breakdown field strength E_{bd}) were carried out using a capacitance–voltage mercury probe, SSM-495 CV System (Solid State Measurements Inc.), and in some cases, for comparison, with a MISCAP (metal–insulator–semiconductor capacitor) measuring system using the polymer film directly deposited on Si and covered by wet etched metal dots (1.0 mm^2, Al). Usually CV

measurements were carried out at a frequency of 0.1 MHz, but at higher frequencies (1 MHz) comparable results were obtained. Profilometer technique and spectral ellipsometry were used to determine the film thickness.

7.3.2.1 Dielectric constant

The dielectric constant can be calculated from Eq. (7.1):

$$k = Cd/(A\varepsilon_0) \tag{7.1}$$

where C is the capacitance, measured with the mercury probe, d the thickness of the dielectric film, A the area of the mercury droplet acting as upper electrode of the capacitor, and ε_0 the vacuum permittivity (8.8542×10^{-12} F/m).

The dielectric constant of CF polymer films, directly deposited on the silicon wafers, varied from 2.0 to 2.7. These different k values could be achieved for different process conditions, C/F ratios, precursor gas flow rates and different mixtures of C, F, and H containing precursors.

The influence of different flow rate ratios of the precursor gases on the dielectric constant is depicted in Fig. 7.10.

Low k values of the dielectric material require a high C_4F_8 concentration in the precursor gas. High fluorine concentration (with respect to carbon) is necessary to reduce the dielectric constant. The same results were obtained by Han *et al*. [18] and Endo *et al*. [14]. This is due to the formation of an increasing number of C–F_x bonds in the polymer having a low electrical polarizability (see Section 7.1).

The influence of normalized precursor gas flow on the dielectric constant is shown in Fig. 7.11.

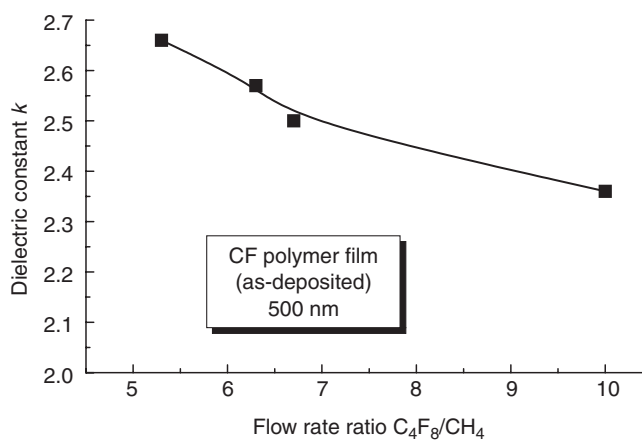

Fig. 7.10 Dielectric constant of CF polymer layers deposited from different C_4F_8/CH_4 precursor gas mixtures.

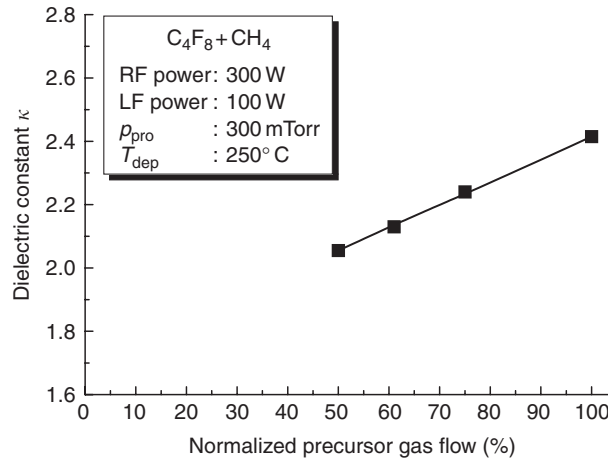

Fig. 7.11 Dielectric constant of CF polymer layers deposited from different C_4F_8/CH_4 precursor gas flows.

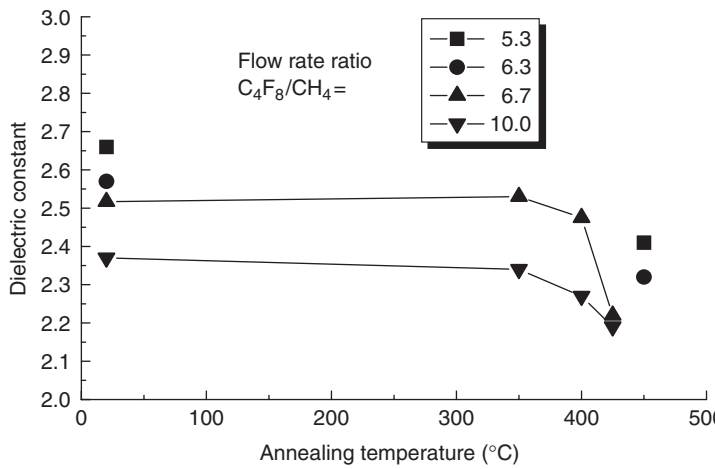

Fig. 7.12 Influence of annealing temperature and C_4F_8/CH_4 flow rate ratio on the dielectric constant of CF polymers [10].

One explanation of this phenomenon could be due to the formation process of the polymer film. The time the polymer molecules may have to form, to arrange on the surface and to cross-link under particle bombardment may have an important influence on the ability to form polymer structures with low polarizable bonds.

Furthermore, the thermal stability of CF polymer low *k* values was investigated. The dielectric constant of CF polymer layers versus annealing temperature is shown in Fig. 7.12.

In Fig. 7.12 two different properties of CF polymers are depicted. The dielectric constant of PECVD polymers can be reduced by annealing in vacuum. According to Uhlig *et al.* [10] this

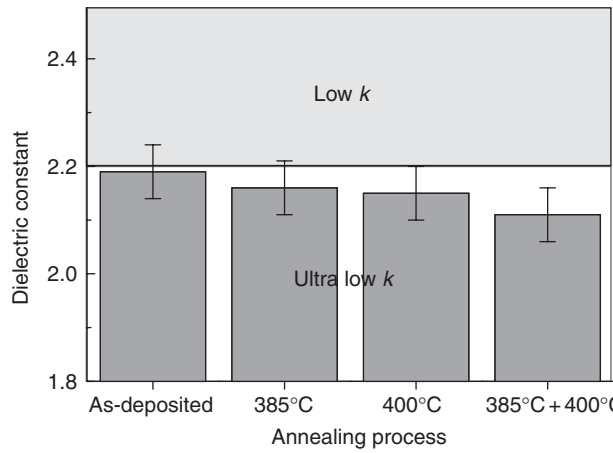

Fig. 7.13 Dielectric constant of CF polymer after annealing in vacuum [29] (© 2001 IEEE).

can be related to the existence of high CF_2 and CF_3 bond concentrations in the deposited polymer layers. C–F bonds are thermally less stable than CF_2 and CF_3 bonds. When the C–F bond breakes at elevated temperatures and fluorine disappears from the molecule, CF_3 fragments can bond to the carbon [18]. Thus the relative fluorine concentration in the polymer molecule is increased and the dielectric constant decreases [6]. CF polymer films deposited from high C_4F_8/CH_4 precursor gas ratios have generally lower k values and lower temperature dependency. Higher C_4F_8/CH_4 ratios cause higher fluorine concentration in the precursor gas and thus in the deposited layer. The general effect of reducing the k value with increasing fluorine content was already described in Section 7.3.2. The thermal stability of the dielectric constant is illustrated more in detail in Fig. 7.13. The permittivity of the polymer slightly lowers with annealing in vacuum. That may be due to an evaporation of residual humidity from the surface or the effect described above (see Fig. 7.12). According to the classification of low-k materials published by Peters [31], these results allow the amorphous CF polymer (nonporous organic material) to be included in the class of ultra-low-k materials with dielectric constant lower than 2.2.

7.3.2.2 Leakage current density I_{leak} and break down field strength E_{bd}

Current–voltage measurements performed with the mercury probe in a voltage range of $\pm 5\,V$ indicated low leakage current densities of less than $2 \times 10^{-11}\,A/cm^2$ for as-deposited and annealed (maximum temperature 400°C) polymer samples. These results look promising regarding the comparison of thermally grown SiO_2 dielectric with CF polymer (see Fig. 7.14).

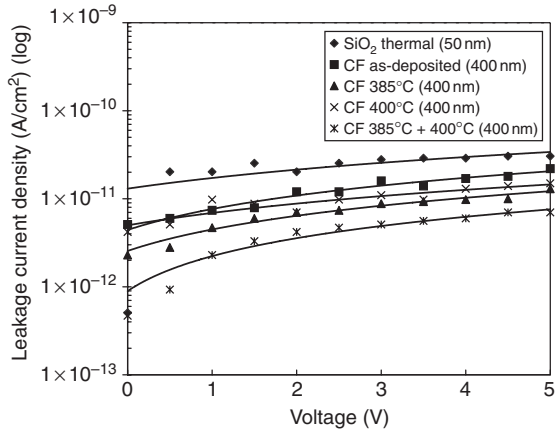

Fig. 7.14 Leakage current density of 400 nm CF polymer films (as-deposited and annealed up to 400°C) in comparison to SiO_2.

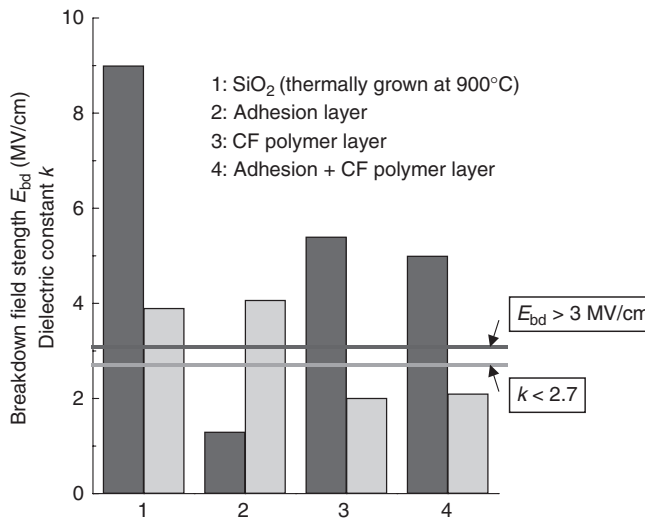

Fig. 7.15 Electrical properties of polymer layer stack in comparison to SiO_2 dielectric [29] (© 2001 IEEE).

7.3.2.3 Influence of CH adhesion layer on electrical properties of CF polymer dielectric

The influence of the very thin adhesion layer deposited *in situ* before low-*k* dielectric film deposition was tested in relation. Due to the low thickness of the CH adhesion layer, compared with the thickness of about 400–500 nm for the CF dielectric, no important changes of electrical low-*k* properties (dielectric constant and breakdown field strength) are expected [25]. The results are presented in Fig. 7.15.

SiO_2 layers grown by thermal oxidation at more than 900°C have very high breakdown field strength (about 9 MV/cm, depending on the process) but a relatively high k value too (about 3.9). The adhesion layer itself has a dielectric constant of about 4 and an $E_{bd} \approx 1.3$ MV/cm. Adhesion layer and low-k CF polymer film alone ($k \approx 2.0$, $E_{bd} \approx 5.5$ MV/cm) and layer stacks (10 nm CH adhesion and 400 nm CF polymer layer) were investigated. Results for the dielectric layer stack obtained from the mercury probe show a negligible deterioration of breakdown field strength and no change in dielectric constant. The stack has a breakdown field strength of about 5 MV/cm and the dielectric constant remains stable at $k \approx 2.0$.

The present goal values for breakdown field strength ($E_{bd} > 3$ MV/cm) and dielectric constant ($k < 2.7$) required for next generation IC feature sizes [21] can be achieved obviously by using the investigated polymer layer stack.

7.4 Integration issues

7.4.1 Concept for single damascene integration

Some issues of CF low-k material/copper integration in a single damascene structure are discussed in this section. Figure 7.16 shows a single damascene architecture for one-level metallization with CF polymer serving as low-k dielectric between two copper lines.

In contrast to the traditional process flow with aluminum and SiO_2 IMD the damascene process requires a new technology. It is necessary to deposit a planar dielectric serving as insulating underlayer. In Fig. 7.16 this isolating layer is named pre-metal dielectric (PMD).

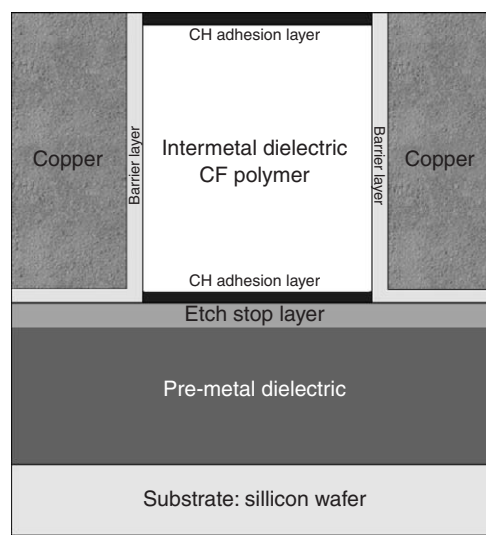

Fig. 7.16 Single damascene architecture for copper/low-k (general description).

The PMD is usually a doped SiO_2, depending on the application. Because the surface has to be absolutely planar (necessary for a well-defined geometry of the damascene metal lines), an additional planarization step performed by CMP may be required. If the dielectric does not serve as etch stop layer for IMD etch an additional layer (e.g. SiN) has to be deposited on top of the PMD. The next step is the CF polymer deposition by PECVD including the deposition of the CH adhesion layers. IMD patterning to create via holes or trenches is performed by photolithography (special processing for CF polymer dielectric, see below). Due to the high aspect ratio (height to width) of the small pattern sizes in the IMD, wet etching can not be used. Dry etch processing with high density plasma etch tools is applied. The IMD etch process must stop in a well defined depth at the etch stop layer. In some cases it is necessary to remove the etch mask by dry or wet etch. Before copper deposition into vias and trenches, a barrier layer is required in each case to avoid any diffusion processes between copper and low-*k* dielectric. For this purpose a very thin TiN, TaN or an other barrier layer is deposited by physical vapor deposition (PVD) or metal organic CVD (MOCVD) followed by the copper deposition. Two different copper deposition techniques are used, electrochemical deposition (ECD) and Cu-MOCVD. The ECD technique requires a start layer called seed layer for the final deposition of copper. The seed layer itself is deposited by PVD or MOCVD. Since barrier and metal deposit on all the surfaces, a CMP operation has to be performed to polish back the copper. The final result of all this process steps is a planar surface and separated copper vias or lines embedded in low-*k* material.

Figure 7.17 illustrates possible process steps to create a single damascene structure with CF polymer IMD and copper.

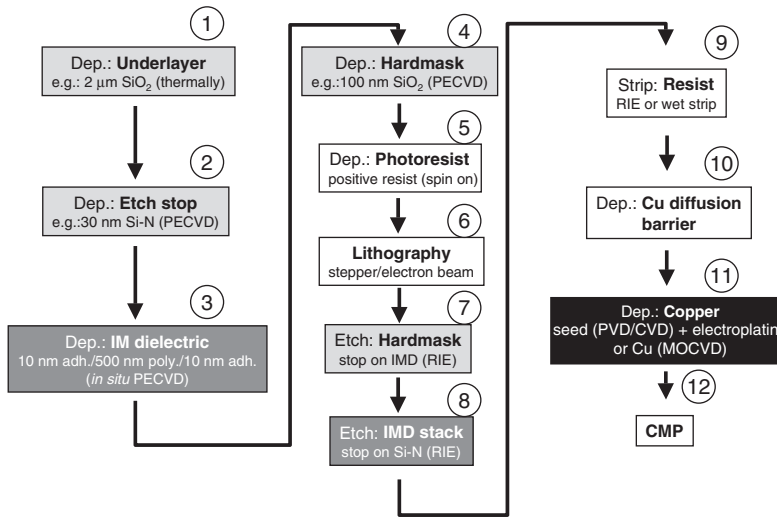

Fig. 7.17 Damascene process flow adopted to special requirements for CF polymer IMD.

The process for IMD deposition (3) [numbers in brackets refer to Fig. 7.17] can be carried out in the way described in Section 7.2.3. The second CH adhesion layer covering the low-*k* IMD is useful to ensure a good adhesion of the IMD to the cap layer or to the PMD of the next metallization level.

7.4.2 Special requirements for CF polymer patterning and copper CMP

7.4.2.1 Patterning of CF polymer film stacks

As an example for some integration issues of CF polymers the etching behavior of this low-*k* material should be described more in detail. The technology for patterning of CF low-*k* films was tested with common bi-level masking technique. Patterning has been performed in the following way. Deposited polymer film stacks (10 nm CH adhesion layer + about 500 nm CF polymer + 10 nm CH adhesion layer) were covered with a PECVD hard mask layer (4) [numbers in brackets: see Fig. 7.17]. Because of the similar properties to resists a hard mask layer like, for example, SiO_2 has to be applied. Usually a 100 nm SiO_2 mask, deposited at temperatures below 400°C by PECVD, was used. On top of the hardmask a photoresist (positive resist) (5) was spun-on and patterned by electron beam lithography (6). Dry etch of the hard mask (7) and polymer (8) was performed in an inductively coupled plasma (ICP) etch tool. Figure 7.18 shows a dry etched 400 nm CF polymer layer stack deposited on silicon wafer and patterned by bi-level masking technique.

Vias with diameters as low as 200 nm were etched representing an aspect ratio of 5 (see Fig. 7.19). The etching results are summarized in Table 7.4.

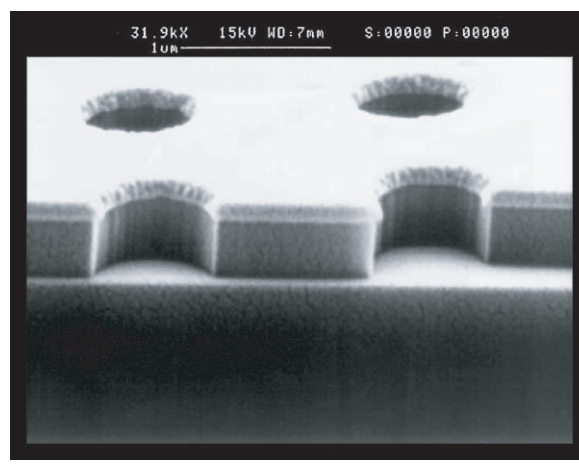

Fig. 7.18 Dry etched low-*k* polymer stack (hard mask on top, substrate silicon) [29] (© 2001 IEEE).

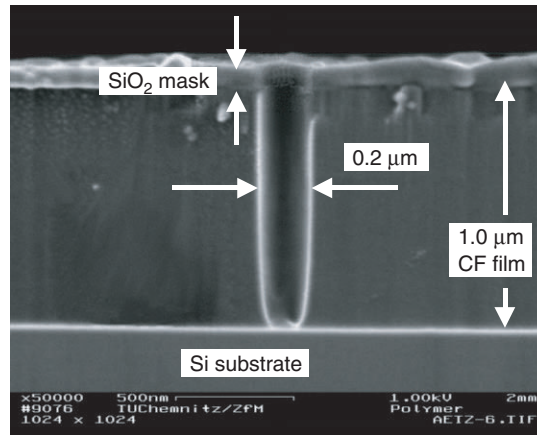

Fig. 7.19 ICP etched via22 (O_2 plasma) [10].

Table 7.4 Results for CF polymer etching

Parameter	Results for CF polymer
Etch rate	≈ 500 nm/min
Edge slope	≈ 90°
Mask	Hard mask
Selectivity to mask	⩾ 10
Selectivity to underlayer	⩾ 10
Edge surface quality	Smooth

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The polymer etch was performed with oxygen plasma (ICP: 500–1000 W plasma power, supported by RF plasma: 0–100 W). After polymer etch optimization etch rates of more than 500 nm/min were achieved. According to the straight and smooth sidewalls shown in Figs 7.18 and 7.19, the edge slope determined from high resolution scanning electron microscope (HR SEM) was about 90°. To receive good agreement between mask sizes and etch geometry, a high etch selectivity (>10) between mask and IMD material is demanded. An etch selectivity ⩾10 was evident. To stop the etching process in a well defined depth, the etch selectivity of the CF polymer with respect to the etch stop or underlayer (e.g. SiO_2 or SiN) should also be as high as possible. Investigations showed a selectivity ⩾10 for this material combinations, too.

After polymer etch the resist can be removed (9) either by reactive ion etching (RIE) or wet strip. The CF polymer films survived wet strip in acetone without dilution or delamination of the polymer films.

Table 7.5 CMP requirements and results for CF polymer

Requirements for low-*k* material	Results for CF polymer dielectric
Good adhesion to the layer under beneath the IMD	Excellent adhesion, tested by tape test (adhesion force >10 N)
Sufficient stiffness	No problems during CMP
Sufficient mechanical strength:	
Hardness: >0.3 GPa	Hardness: > 5 GPa [8]
Young's modulus: >3 GPa [32]	Young's modulus: ~ 3 GPa [32]
Polishing rate technology relevant	20 nm/min with de-ionized water 170 nm/min with Cu slurry QCTT 1010 + H_2O_2
Chemical resistance against CMP chemicals	No changes in electrical properties after CMP

7.4.2.2 CMP of copper integrated with CF polymer dielectric

Besides low-*k* dielectric patterning, CMP (12) of low-*k* integrated with copper is a big challenge due to the challenges arising from the soft, more fragile nature [31] and insufficient adhesion of low-*k* materials and the chemical resistivity. To perform CMP with copper and low-*k* material the dielectric has to meet several requirements. These requirements and the results for CF polymer are summarized in Table 7.5.

The insufficient adhesion of the CF polymer dielectric could be eliminated by the additional CH adhesion layer (described in Section 7.3.1). CMP of polymer film stacks (CH adhesion layer + 500 nm CF polymer) was carried out on blanket wafer samples. Results for CF polymer polishing rates are shown in Table 7.5. Polymer samples survived CMP without delamination. CH adhesion layers deposited on top of the CF polymer may act as CMP stop layer due to their elevated hardness. Jacobsohn *et al.* [8] reported that hardness of CF polymers depends on the carbon content. Sufficient stiffness and mechanical strength of the low-*k* material are required for CMP processing. Among candidates for ultra low-*k* application, bulk materials like plasma deposited CF polymers should have higher mechanical strength compared to porous materials. The ability of performing CMP of CF polymer films was also tested successfully by Endo [6] and Hara *et al.* [33]. No influence of the CMP chemicals on the properties of the low-*k* material could be detected. Due to the final surface cleaning process with ultrasound in DI water after CMP, moisture uptake of CF polymers was investigated. The dielectric constant of a material is extremely sensitive to the absorption on or incorporation of smallest amounts of water into the dielectric because of the high electrical polarizability ($k \approx 80$) of water. CF polymer samples directly inserted into DI water did not change their electrical properties and no changes in film thickness due to water absorption could be measured. Before the measurements the polymer films were simply dried by storing the coated wafers in room atmosphere for about half a day.

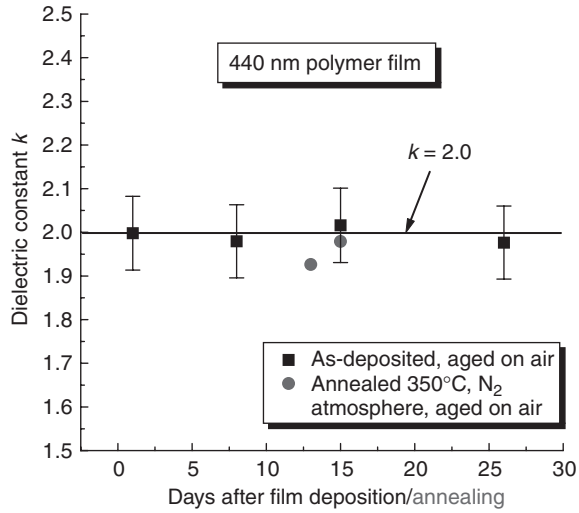

Fig. 7.20 Aging of CF polymer layer [10].

No drying or heating processes were used to remove residual water. Previous investigations demonstrated that storage of polymer films in room atmosphere did not alter the dielectric constant within 1 month [10] (see Fig. 7.20).

7.5 Summary and conclusions

- In an overview low-*k* interlayer dielectric materials, deposited by chemical vapor deposition, are briefly described. C–F polymer low-*k* materials, deposited by plasma enhanced chemical vapor deposition, are the subject of this chapter.
- The properties of the plasma deposited CF polymers can widely be influenced by the selection of the precursor material and the plasma deposition process parameters.
- High rates for plasma deposition were achieved. No additional step (e.g. curing) is necessary for the low-*k* film deposition, and thus, a high wafer throughput is possible.
- The electrical properties (dielectric constant, breakdown field strength, leakage current density), film surface roughness, refractive index of CF polymer layers remain stable even after exposure to high temperatures (400°C).
- Film adhesion problems can be eliminated by *in situ* deposition of an ultrathin adhesion promoting layer.
- The influence of the adhesion layer on dielectric stack properties is negligible, even after annealing up to 400°C.
- Due to the high degree of cross-linking, plasma polymerized CF dielectrics have relatively high thermal stability (400°C), and orientation dependent properties could not be observed.

- Plasma deposition of CF polymers causes higher stiffness, hardness, and Young's modulus, compared with equivalent materials, deposited by thermal CVD or spin-on.
- CF polymer dielectric is mechanically stable enough for CMP processing.
- Interactions of CMP chemicals with CF polymer could not be detected.
- Patterning (ICP etch) of the dielectric layer stack resulted in structures with straight, smooth side walls, tested for high aspect ratio (5) in structures down to 200 nm.
- All the deposition and patterning processes can be performed with IC fabrication compatible chemicals, processes, and tools.
- By making fully dense plasma deposited CF polymer (with $k \approx 2.0$–2.2) porous, this material will offer lowest dielectric constant values.
- Regarding integration issues in dual damascene metallization schemes, further work on CF polymer dielectric, deposited by PECVD, has to be done.

Acknowledgments

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Chapter 8
Spin-on Si-based low-*k* materials

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Abstract

The chapter covers a brief review of silsesquioxane (SSQ) materials and a detailed introduction to deposition, properties and selected integration results of porous SiO_2-like films. All materials described are based on silicon and deposited by using the spin-on process. The review on SSQ materials covers polymerisation and integration issues of various types of SSQ. Different suppliers of precursors for depositing SSQ based low-*k* dielectrics are summarised. The SiO_2-like porous dielectrics are introduced via a short excursion to fundamentals related to introduction of porosity to dielectric materials. An overview covers all known routes to deposit this group of low-*k* dielectric films using spin-on processing before focusing on the deposition and hydrophobisation post-treatment of SiO_2 aerogel thin films in detail. Furthermore, detailed insight is provided in the main film properties required for integration by highlighting film morphology, chemical composition and structure, electrical, mechanical as well as thermal properties. Wherever possible, dependence of properties on different porosities is shown. After a brief discussion of the main integration challenges of porous low-*k* dielectrics into Copper Damascene interconnect schemes, all basic material and process compatibility issues are discussed for the porous SiO_2 aerogel films. This comprises lithography compatibility, cap layer and hard mask deposition, etching, diffusion barrier deposition and chemical mechanical polishing of Copper at the porous films.

8.1 Silsesquioxane low-*k* dielectric materials

Candidates for low dielectric constant materials in interconnect systems are the silsesquioxane (SSQ) spin-on glasses. In general, SSQs have the chemical formula $(RSiO_{1.5})_n$ with R standing for a low molecular weight organic substituent (e.g. CH_3, C_6H_5) or hydrogen. They are usually derived as oligomers with cage or ladder structure (see Fig. 8.1) [1]. According to the substituent present they are called:

hydrogen-silsesquioxane (HSQ, HSSQ)
methyl-silsesquioxane (MSQ, MSSQ)
phenyl-silsesquioxane (PSQ), etc.

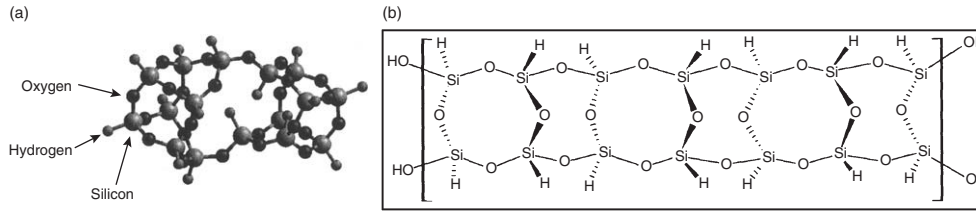

Fig. 8.1 Cage (a) and ladder (b) structure of HSQ as an example for the SSQs.

Table 8.1 Different SSQ-based low-*k* materials and examples for available precursor materials

Material	Trade name	Company	Dielectric constant
HSQ	FOx (flowable oxide)	Dow Corning	2.9–3.0
MSQ	e.g. RZ25–15	Hitachi	2.6
MSQ	HOSP	Honeywell	2.6
Porous HSQ	XLK	Dow Corning	2.2
Porous MSQ	LKD 5109	JSR	2.2–2.3
Porous MSQ	Zirkon	Shipley	2.3

Thin film processing leads to the formation of an inorganic polymer, a polysilsesquioxane. To deposit SSQ films the SSQ oligomer is dissolved in a solvent. Precursor materials are available from different manufacturers (see Table 8.1). The precursor solution is spun onto the silicon substrate to form a film accompanied by continuous solvent evaporation. Furthermore, baking and finally curing steps are necessary to promote the three-dimensional (3D) glassy structure. Baking is usually done at hot plates for a few minutes at lower temperatures (e.g. 180–250°C for MSQ and 150–350°C for HSQ), whereas curing takes place as furnace anneal at higher temperatures (e.g. 400°C for MSQ) according to Liu *et al.* [2] and Liou and Pretzer [3]. After spin-on, the film has the properties of a liquid gel. During baking the residual solvent will be removed. The curing provides the oligomeric condensation and bulk polymerisation reactions which generate the 3D glassy structure bonded via a siloxane (–Si–O–Si–) backbone [4]. This backbone is very similar to SiO_2 but contains a large portion ($>25\%$) of non-bridging Si–R bonds, which leads to a lower density material compared to SiO_2. This is the main reason why the SSQ materials exhibit low dielectric constants in the range of 2.5–3.3.

The two main materials for low-*k* dielectric applications are HSQ and MSQ. HSQ with *k*-values between 2.9 and 3.2 shows several processing issues like thermal stability (the structure can be changed into a network structure during thermal processing above 400°C due to disassociation of Si–H bonds, for example, reported by Liou and Pretzer [5]) and integration problems.

MSQ materials have higher thermal stability, but suffer from degradation during O_2 plasma resist stripping [2] like many other low-k materials. Alternative resist stripping options or specially treated MSQ films (for example, by H_2 plasma treatment [2]) could be a solution for this challenge.

Further expansion of the SSQ materials has taken place over the recent years by introducing additional porosity into HSQ and MSQ (see also Table 8.1). This can be achieved by either using 'templating' or two-phase hybrid systems, as described in Section 8.2.

8.2 Porous SiO_2

8.2.1 Fundamentals

Currently used SiO_2 dielectric films deposited by PECVD exhibit relative dielectric constants k of 4.2–5.5, which is higher than that of thermally oxidised SiO_2 (3.9). The lowest known k-values are those of air and vacuum which equal 1.0. Porous dielectrics combine both dense dielectric material properties and those of air/gas achieving substantially lower k-values compared to the respective dense material. The volume fraction of pores in the material, porosity π, is related to the material density of the skeleton ρ_{skeleton} by the following equation:

$$\pi = 1 - \rho = 1 - (\rho_{\text{film}}/\rho_{\text{skeleton}}) \tag{8.1}$$

where ρ is the volume fraction of solid material in the porous film and ρ_{film} the overall porous film density. The actual permittivity depends strongly on the porosity of the material. To describe the dependency of permittivity versus porosity different models can be used. The application of a two-layer model is the simplest approach giving the lower and upper limits of the achievable k-value by using a serial and parallel capacitance equation, respectively:

$$k_{\text{porous, serial}} = 1/(\pi/k_{\text{gas}} + \rho/k_{\text{solid}}) \tag{8.2}$$

$$k_{\text{porous, parallel}} = \pi \cdot k_{\text{gas}} + \rho \cdot k_{\text{solid}} \tag{8.3}$$

The effective medium consisting of two components with a given volume fraction (in our case π and ρ) and distinct properties (e.g. k-value) is a more real model, which can be described by the effective medium approximation (EMA) proposed by Bruggeman [6]:

$$\pi(k_{\text{gas}} - k_{\text{e}})/(k_{\text{gas}} + 2k_{\text{e}}) + \rho(k_{\text{solid}} - k_{\text{e}})/(k_{\text{solid}} + 2k_{\text{e}}) = 0 \tag{8.4}$$

The resulting curves for the permittivity of a porous SiO_2 film versus its porosity are depicted in Fig. 8.2 for a dense material permittivity of 3.9 (SiO_2 grown by thermal oxidation).

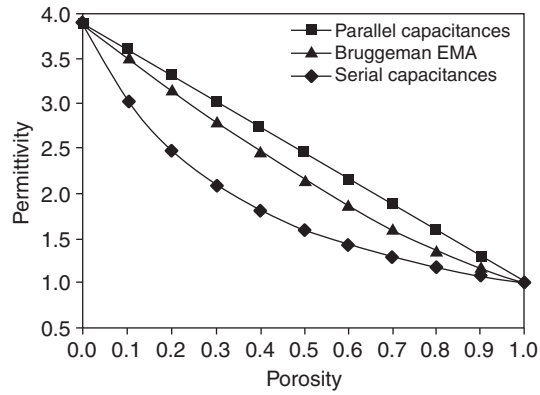

Fig. 8.2 Permittivity of porous SiO_2 versus porosity.

8.2.2 Spin-on deposition process

8.2.2.1 Approaches for porous SiO_2 deposition

Different deposition routes exist to realise porous inorganic thin films. A classification can be made by distinguishing between how the porosity is introduced into the material:

1. Gelation in the presence of liquids and careful drying of the so-formed porous network (*conventional sol-gel processing* using special solvent(s) and/or special drying).
2. Supramolecular arrays of self-assembled surfactants can combine with a molecular source of silica to form periodic porous materials (*surfactant templated mesoporous silica*).
3. Controlled templated polymerisation of *organic–inorganic two-phase systems* with sacrificial removal of the organic phase.

Examples for the different approaches are given in Fig. 8.3. The principle of the porous inorganic dielectric deposition and the process flows are briefly discussed for some of them in the following.

Aerogels and xerogels

Both aerogels and xerogels are derived from conventional sol–gel processing extensively and basically described by Brinker and Scherer [7]. A sol consisting of a silica source, water, a solvent and a catalyst is allowed to gel, that is, hydrolysis of the silica source and condensation reactions take place forming silica chains and 3D silica networks until the gel point is reached. The gel point is difficult to measure, and according to Brinker and Scherer [7], can be the point at which the sol viscosity abruptly increases as shown in Fig. 8.4. It corresponds to the formation of a single 3D network in the precursor container. Further strengthening of the network takes place as smaller clusters join the larger network during what is known as ageing. The pores of this network contain a mixture of water, catalyst, ethanol, original solvent and partially reacted

Conventional sol–gel processing using special solvent(s) and/or special drying	**Surfactant-templated mesoporous silica**	Controlled templated polymerisation of **organic–inorganic two-phase systems** with sacrificial removal of the organic phase
• Aerogels, Xerogels (Honeywell, TI, AMD, Lucent, TU Chemnitz, Seoul University) • Porous HSQ (Dow Corning: XLK)	(Sandia Nat. Labs, Univ. New Mexico, UC Santa Barabara, Pacific Northwest Nat. Lab.)	• MSQ with macro molecular pore generator (porogen) (IBM) • TEOS sol–gel process in presence of polymers (Asahi: ALCAP-S)

Fig. 8.3 Porous silica deposition routes including material examples and respective research institutes and companies.

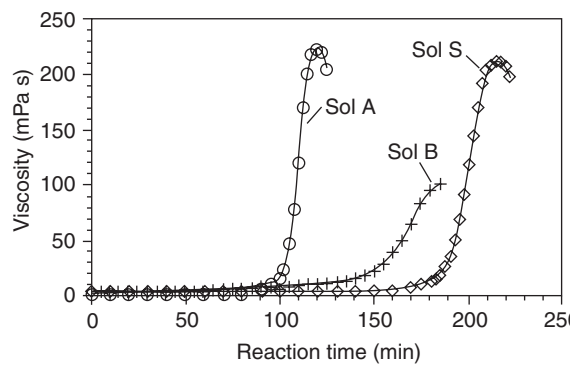

Fig. 8.4 Viscosity evolution over time during sol–gel processing for different sols (composition see Section 8.2.2.2).

species. The coating of the wafers is done by means of a spin-on process in the sol state before reaching the gelation point. Usually, a solvent atmosphere is maintained during spin-on and further gelation and ageing to prevent solvent evaporation and thus premature drying of the gel. To remove the pore liquid the wet gel must be dried without collapse of the porous structure which may happen due to the capillary forces which become effective during simple solvent evaporation. Therefore, two approaches described in Fig. 8.5 rely on avoiding the crossing of the direct liquid–gaseous transition during drying. Supercritical drying as described, for instance, by Hrubesh *et al*. [8] has been applied where the gel is treated above the critical point of the pore liquid usually at high temperatures and very high pressures (up to 200 bar). A solvent exchange is often carried out before drying to minimise the pressure required by using a solvent with critical point at moderate pressures. Nevertheless, this technique requires specialised equipment such as an autoclave. Another possibility to circumvent the capillary forces is to prevent the

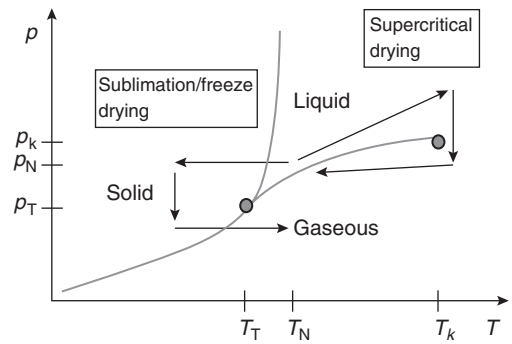

Fig. 8.5 Phase diagram showing two gel drying approaches for avoiding the liquid–gaseous transition.

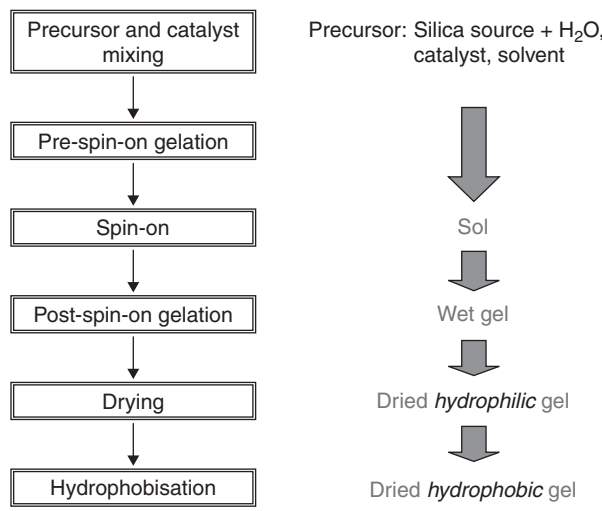

Fig. 8.6 Example of a general process flow to produce aerogel/xerogel films by solvent evaporation drying.

liquid–gaseous transition by sublimation or freeze drying (Fig. 8.5) as shown by Gessner and coworkers [9]. The pore liquid is transferred to the solid phase and then removed by sublimation. A lot of work has been done, for example, by Cho and coworkers [10] to examine the effectiveness of replacing the fluid contained in the pore network with one of lower surface tension and volatility, which is another approach to prevent substantial densification (collapse) of the porous network during drying. By removing the liquid from the pores and replacing it with a liquid of lower surface tension, the capillary forces experienced by the solid network can be reduced as the liquid evaporates leading to reduced film shrinkage. Thus, simpler drying techniques can be used like enhanced evaporation in vacuum. Usually the different drying processes leave a hydrophilic porous SiO_x film, which has to be post-treated to get the desirable hydrophobicity which enables electrical integrity and further processing. An overview of the process flow is given in Fig. 8.6.

Conventionally, a distinction is made between aerogels (dried supercritically) and xerogels (non-supercritically dried). However, this distinction is becoming blurred as non-supercritical drying methods can now achieve low densities previously only obtainable via the supercritical route. In doing so, the term 'aerogel' is becoming synonymous with low-density materials produced by the sol–gel route, regardless of gel drying [11]. In this book, the term 'aerogel' is used to describe all low-density materials prepared by the sol–gel process described in Section 8.2.2.2.

Surfactant templated silica

New approaches by using traditional sol–gel processing with self-assembly strategies allow the formation of highly ordered mesoporous films also called micelle-templated silica. Producing surfactant templated mesoporous silica needs a homogeneous solution of soluble silica and surfactant prepared in an alcohol/water solvent. The surfactants (or block copolymers) consist of a hydrophobic and a hydrophilic part (amphiphilic nature, see Fig. 8.7). Preferential evaporation during spin-coating results in self-assembly of surfactants into micelles. Further self-organisation occurs into liquid crystalline mesophases that organise the soluble silica about their hydrophilic exteriors (Fig. 8.8). This leads to precisely defined pore size and shape depending on the

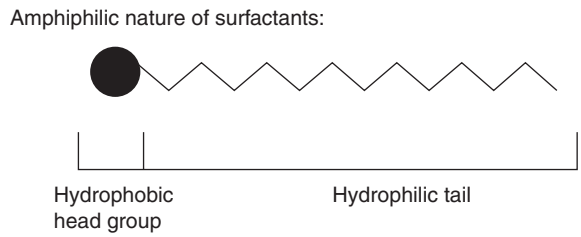

Fig. 8.7 Schematic of the structure of surfactants.

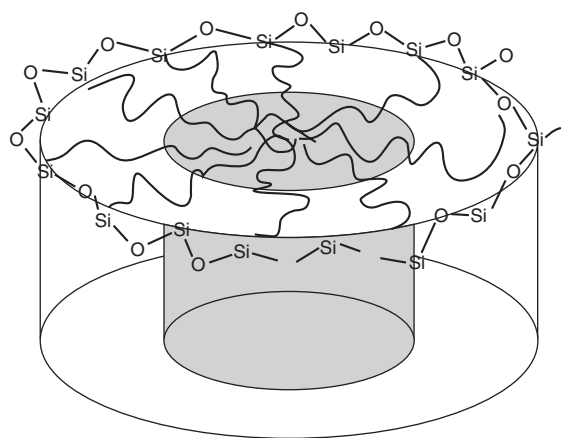

Fig. 8.8 Self-assembly of surfactants and soluble silica.

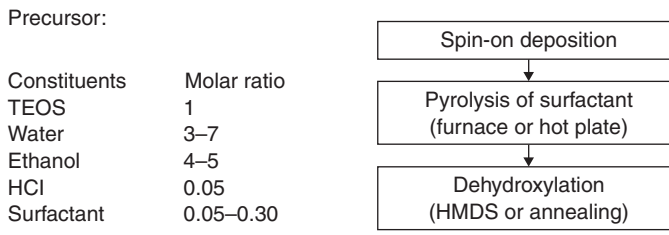

Fig. 8.9 Example of precursor composition and process flow for surfactant-templated silica.

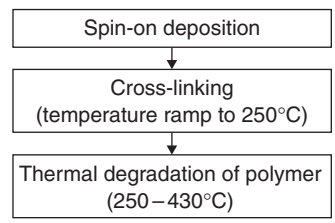

Fig. 8.10 Example for process flow for controlled templated polymerisation of MSQ/PCL two-phase system to produce porous silica.

surfactant array shape. Thus, the pore size of the porous silica can be adjusted by the choice of surfactant. The surfactants usually are high molecular weight organic molecules like:

cationic: CTAC (cetyltrimethyl ammonium chloride, mol. wt. = 320)
non-ionic: PEO (poly(ethyleneoxide), mol. wt. = 300–1100).

Silicate polymerisation completes the formation of the solid network. To obtain a porous silica network the surfactant has to be removed during a thermal treatment. The interior pore surface can be made hydrophobic using organosilane precursors with non-hydrolysable ligands or by post-treatment in hydrophobising agents as described in Section 8.2.2.3. An example of the process flow according to Baskaran *et al*. [12] is shown in Fig. 8.9.

Organic–inorganic two-phase systems

The principle is based on the formation of an organic–inorganic polymer hybrid (inorganic low-*k* material and low molecular weight organic polymer). Upon heating, the glass resin cross-links around the organic polymer templates. This is followed by thermal decomposition and out-diffusion of the organic fragments during annealing and leaves a porous inorganic network. An example of a process flow using MSQ as low-*k* material and poly(caprolactone) (PCL) as organic polymer proposed by Remenar *et al*. [13] is given in Fig. 8.10.

8.2.2.2 Aerogel process using solvent evaporation drying in vacuum

This process relates to class (1) described in the foregoing section. SiO_2 aerogel is prepared by a sol–gel process using tetraethylorthosilicate (TEOS) and water as a precursor. As TEOS is not

Table 8.2 Gel times for a given sol using different catalysts (according to Ref. [7])

Catalyst	Gel time (h)
HF	12
HOAc	72
HCl	92
HNO_3	100
H_2SO_4	106
NH_3	107
HI	400

miscible with water, a low surface tension alcohol is used as a solvent. First TEOS is hydrolysed:

$$Si(OC_2H_5)_4 + H_2O \rightarrow (C_2H_5O)_3Si{-}OH + C_2H_5OH$$

The following water condensation reaction then takes place:

$$(C_2H_5O)_3Si{-}OH + HO{-}Si(OC_2H_5)_3 \rightarrow (C_2H_5O)_3Si{-}O{-}Si(OC_2H_5)_3 + H_2O$$

along with alcohol condensation:

$$(C_2H_5O)_3Si{-}OC_2H_5 + HO{-}Si(OC_2H_5)_3 \rightarrow (C_2H_5O)_3Si{-}O{-}Si(OC_2H_5)_3 + C_2H_5OH$$

As gelation proceeds, water and ethanol are produced upon the formation of siloxane (Si–O–Si) bonds. Oligomers of siloxane grow forming aggregates which become clusters when they impinge upon themselves. The rates of hydrolysis and condensation reactions, as well as the final structure of the gel, can be controlled by means of the amount and type of catalyst used, the ratio of TEOS to water (R), the amount of solvent and the process temperature. Si as the electrophilic and O as the nucleophilic centre allow a basic or an acidic attack of the TEOS molecule. So both an acidic and a basic mechanism of hydrolysis and polycondensation are possible. The gelation time can be very different as shown by Brinker and Scherer [7] (see Table 8.2). Stoichiometrically, the overall reaction requires a molar ratio of water to TEOS of $R = 2$. However, excess water must be added to ensure more complete gelation.

Aerogel films are produced using a spin-on process to deposit the carefully prepared sol onto silicon wafers after a certain time the sol needs to undergo first polymerisation reaction and reaching a viscosity convenient for the spin-on process (see Fig. 8.11). The wet film is allowed to further polymerise and form a gel and finally age both under solvent atmosphere. Afterwards the wet film is exposed to a vacuum. The liquids remaining within the pores (ethanol, water and solvent) leaves the solid SiO_2 network as a film on the wafer. This is then normally baked under vacuum to remove physisorbed water and some hydroxyl surface species. The different steps of this process are briefly described within this chapter showing the main

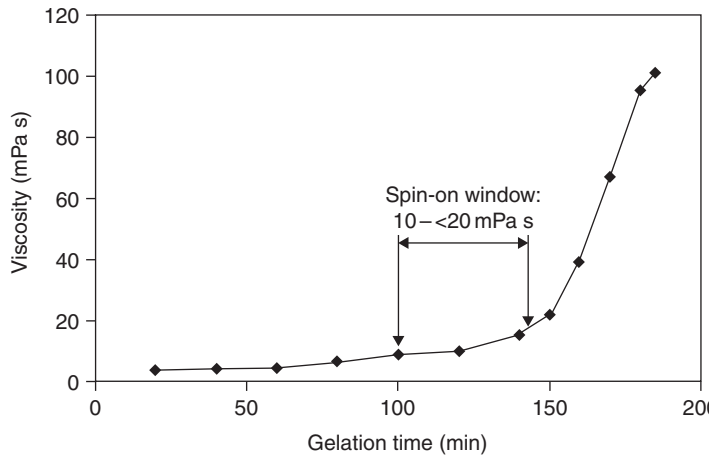

Fig. 8.11 Process window for spin on during gelation period.

parameters influencing the process and film quality. Finally, the samples are exposed to the vapour of a hydrophobising agent, which is able to remove water and –OH groups from the large inner surface and to passivate it with hydrophobic surface groups (see Section 8.2.2.3 for details).

Precursor composition

Besides TEOS and water, the precursor consists of a low surface tension solvent to prevent the solid network from collapsing during the drying step and HF as a catalyst which guarantees the lowest gelation times for a single step catalysis. Further acceleration of the gelation can be achieved by a two-step catalysis starting with acidic catalyst like HF and adding a basic catalyst, for instance, in the gas phase after spin-on as shown by Brinker and Scherer [7] and Smith *et al.* [14]. Figure 8.12 shows the gelation time, that is, the time between catalyst addition and gelation point, for different ratios of the precursor constituents. It is seen that increasing the water to TEOS ratio leads to a decrease in gelation time while increasing the solvent to TEOS ratio produces a longer gelation time (dilution effect by the solvent). The TEOS:water:solvent mixture of 1:13:4 is not completely miscible. Table 8.3 summarises the precursor sols which were investigated in more detail with respect to the effect of process parameters on gelation time and film properties.

The electrical properties (see also Section 8.2.3.3) of the porous films are a good measure for the quality of the porous network. An overview of the results for the three main sols under investigation is shown in Fig. 8.13. This shows the dielectric constant value k obtained for each sol and the corresponding maximum field breakdown (FBD) voltage and leakage current density J_{leak} (at 5 V) for that particular sample. These samples were annealed and HMDS treated for 24 h at room temperature.

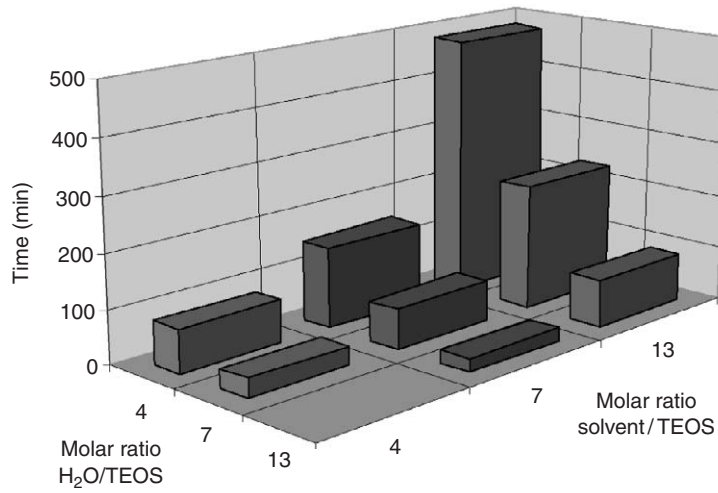

Fig. 8.12 Gelation time dependence on precursor composition.

Table 8.3 Composition of precursor sol examples for aerogel thin film deposition

Sol name	TEOS:water:solvent (molar ratio)	HF concentration (vol%)
Sol S	1:7.4:5.8	0.2–0.6
Sol A	1:13:7	0.2
Sol B	1:7:13	1

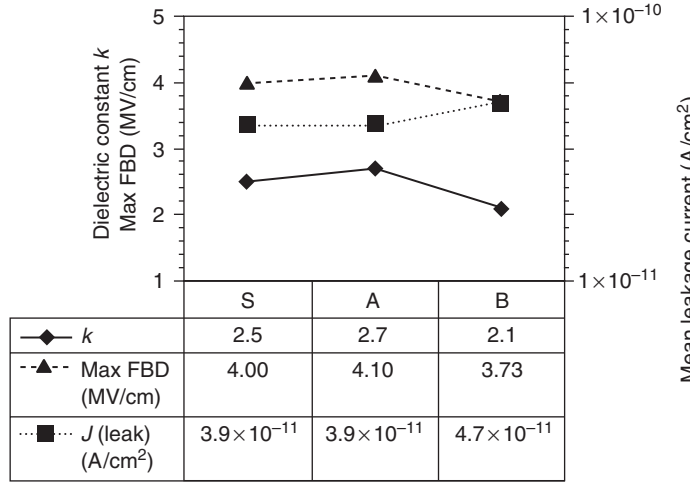

Fig. 8.13 Electrical parameters of aerogel films for application of different sol compositions.

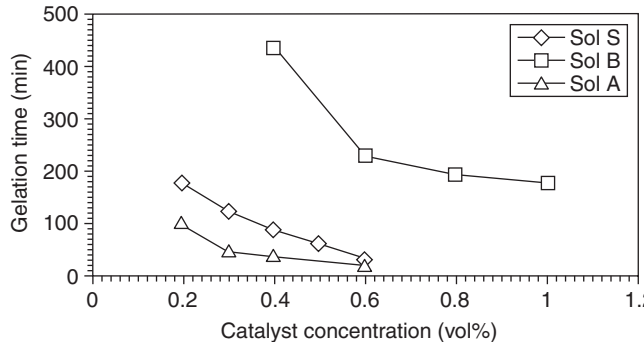

Fig. 8.14 Gelation time versus HF catalyst concentration for low-*k* aerogel.

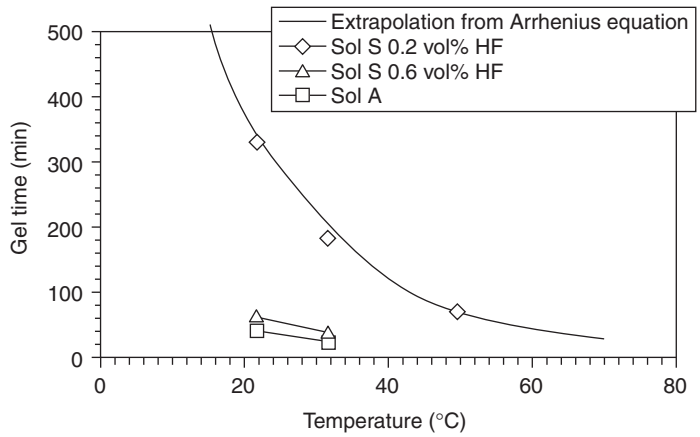

Fig. 8.15 Gelation time versus temperature for different sols.

Type of catalyst and its concentration

Hydrofluoric acid was chosen to yield the lowest gelation times (see Table 8.2). The influence of its concentration in the sol on gelation time is depicted in Fig. 8.14 for different sol types. For the investigated catalyst concentration range the gelation time decreases with increasing catalyst concentration. At higher acid concentrations, the effect of catalyst concentration decreases. A saturation and even increase of gelation time is seen for HF concentrations above 2 vol%.

Temperature

Figure 8.15 shows the dependence of gelation time on process temperature. The result shows that increasing the process temperature decreases the gelation time, that is, accelerates the chemical reaction. This behaviour can be used either to decrease process time during post-spin-on gelation by using elevated temperatures as well as to increase precursor storage time before spin-on by applying cooling.

Spin-on

Film thickness depends on the viscosity of the sol at spin-on and the spin programme (rotation speed, ramp and time) used to deposit it. A range of spin programmes was investigated for sol B. The samples were spun-on starting at 100 min after HF addition at a viscosity of about 10 mPa s (total gelation time 250 min observed at the remaining bulk sol). A wide range of thicknesses from 400 to 1000 nm were found to be possible for sol B, as can be seen in Fig. 8.16.

The dielectric properties of the porous film were also found to be affected by the extent of reaction of the sol at spin-on. After the addition of HF catalyst, sol B was spun-on to each of four identical wafers at 40 min intervals. Due to the gelation, the viscosity of the sol increased over this interval. The results from the first three samples after annealing and 24 h HMDS exposure are shown in Fig. 8.17. An obvious decrease in *k* and leakage current is observed as the gelation

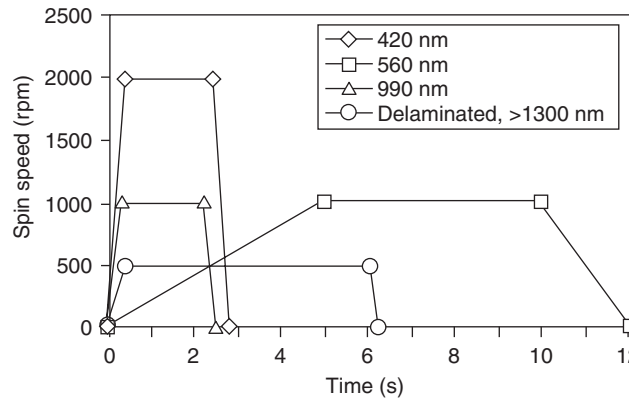

Fig. 8.16 Spin-on regimes and resulting thicknesses for aerogel sol–gel processing.

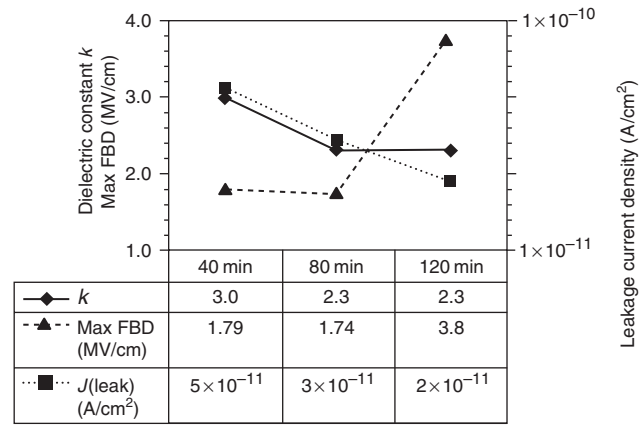

Fig. 8.17 Electrical parameters of aerogel films for different spin-on times after catalyst addition.

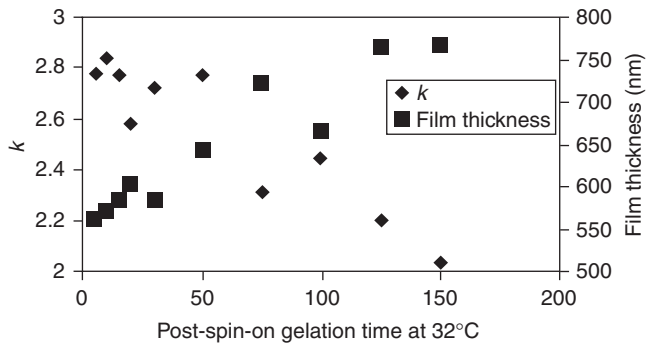

Fig. 8.18 Dielectric constant and film thickness for different post-spin-on gelation times.

proceeds further. The FBD value was highest in the sample spun-on after 120 min. It can be concluded that the longer the precursor is allowed to gelate before spin-on, the better the film qualities.

Post-spin-on gelation and ageing

The films were placed quickly (within a few seconds) in a saturated solvent atmosphere after spin-on. The treatment can be carried out at different temperatures from room temperature up to the liquid boiling temperature. The effect of the post-spin-on gelation and ageing time is seen by evaluating thickness and dielectric constant of films spun-on at the same time after catalyst addition but were allowed different times to gelate before post-treatment (anneal and hydrophobisation). The results are shown in Fig. 8.18. It is seen that film thickness increases and dielectric constant k decreases with increasing post-spin-on gelation time. The minimum k value measured was 2.03 for a sample that was allowed to gelate for $t = 150$ min at 32°C after spin-on. As gelation proceeds on the wafer the liquid containing silica network grows and strengthens. After gelation, the wafers were generally annealed to 450°C under vacuum before hydrophobisation treatment.

8.2.2.3 Post-deposition hydrophobisation

Porous silica aerogel and xerogel layers suffer in the as-deposited state from water adsorption caused by surface silanol groups resulting in insufficient electrical properties like k-value and leakage current. To stabilize electrical properties and to get a sufficient reliability for further integration steps layers have to be made hydrophobic. Many investigations have been done in recent years in the field of hydrophobisation for silica by several mono- and multi-functional silanes, siloxanes and silazanes [15–17]. Especially HMDS is widely employed because of its high reactivity with silica surface silanols due to its basic nitrogen [18]. The surface characteristics of the treated samples influence significantly the hydrophobisation result, not only related with morphology, but also with chemical state depending on production history and pre-treatment at

elevated temperatures. Hydrophobisation is achieved by silylation, that means surface silanol groups are reacted to yield trimethylsilyl (TMS) surface groups. An important condition for application with respect to integration issues is that the silylation process bases on chlorine-free silylating, which is able to react surface silanol groups in short time and liberate only less toxic and hazardous by-products. The next requirement consists in long-term irreversibility of the hydrophobisation effect keeping electrical properties of the layers reliable over several months. Hexamethyldisilazane (HMDS), trimethylsilyldiethylamine (TMSDEA) or trimethylsilylacetate (OTMSA) was applied in the form of saturated vapour over the liquid at room temperature in a closed container. The exposure time and temperature was varied. After gelation the coated wafers were cut and then annealed at 450°C for 1 h under vacuum to drive out organics and water from the pores. The pre-treatment at 450°C causes the loss of adsorbed water and formation of siloxane bridges and free silanol surface groups according to Brinker and Scherer [7]. Hydrophobisation treatment followed immediately after annealing. HMDS, TMSDEA and OTMSA can be adsorbed at the surface.

Following the findings of Gunko *et al*. [18], one of the electrophilic Si on HMDS attacks the nucleophilic oxygen of a free surface silanol to form TMS-surface groups. This reaction mechanism is also believed to be true for TMSDEA and OTMSA. The scheme of the bilance reactions for the different chemicals is seen in Fig. 8.19. The HMDS attack leads to structural and morphological changes in the porous SiO_x films. Using FTIR spectroscopy, the obvious destruction of surface silanols, appearance of methyl in TMS groups and an increase in number of Si–O–Si-bonds due to formation of surface TMS groups was shown by Fruehauf *et al*. [19] to be remarkable even after 1 min exposure. This means that there should be a rapid but not full coverage of surface by TMS groups in a short time (< 1 min). The surface load by TMS groups

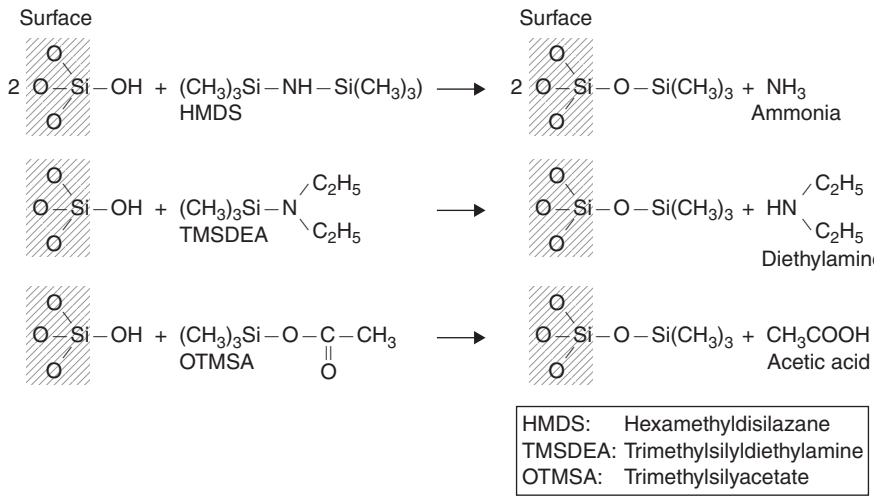

Fig. 8.19 Scheme of the bilance reactions for the different hydrophobisation chemicals (after [19]).

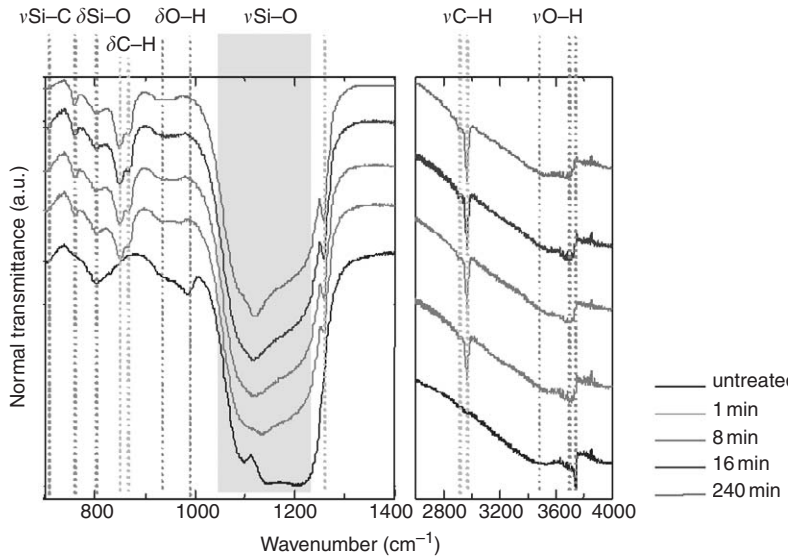

Fig. 8.20 FTIR spectra for HMDS treatment of aerogels for varying exposure times [19].

Table 8.4 Pore volume reduction during application of different hydrophobisation chemicals extracted from [19]

Exposure time (min)	Relative pore volume (after treatment/initial) (%)		
	HMDS	TMSDEA	OTMSA
1	87.9	82.1	95.4
8	81.8	79.0	94.9
16	81.8	79.8	93.4
240	Not determined	77.7	89.1

then increases continuously but more slowly until about 4 h exposure time (Fig. 8.20). The retarded reaction after initial step is also reported by Sindorf *et al.* [20] and is explained by steric hindrance. The loading of the aerogel surface by TMS groups is accompanied by a significant reduction in porosity. Pores smaller than 2 nm are closed during the hydrophobisation treatment and the pore volume shrinks as shown by Himcinschi *et al.* [21]. The porosity calculated from refractive index measured by ellipsometry using an effective medium approximation was used to obtain the summarised data of pore volume reduction for the different hydrophobisation agents in Table 8.4. The porosity decrease with treatment time is assumed to be caused mainly by pore filling or covering by TMS groups in agreement with the results published by Fuji *et al.* [22]. Change in porosity is stronger for TMSDEA than for HMDS and OTMSA. Both FTIR

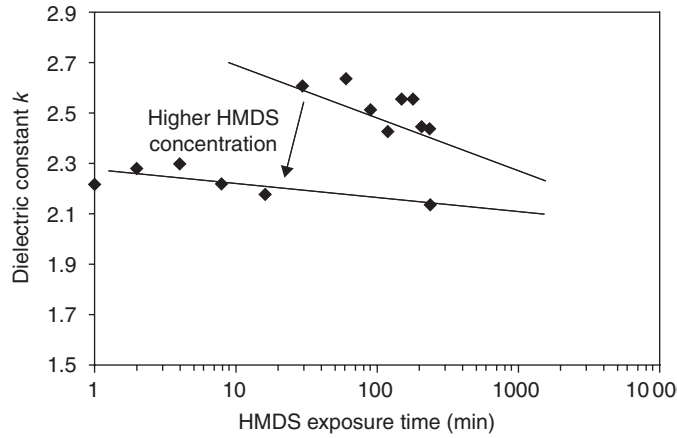

Fig. 8.21 Aerogel dielectric constant versus HMDS exposure time.

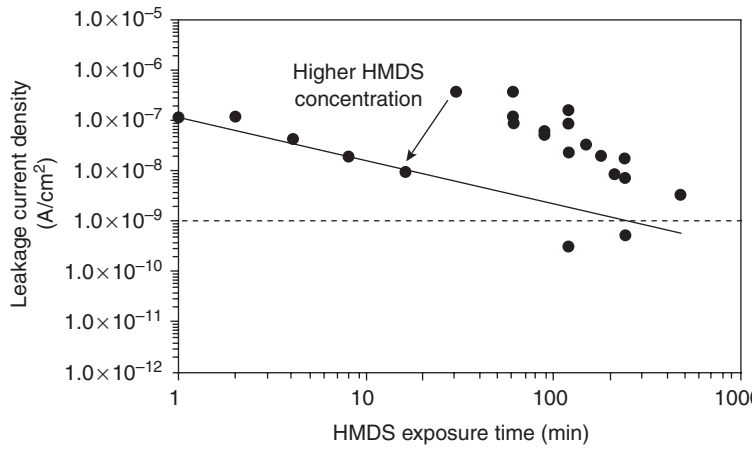

Fig. 8.22 Aerogel leakage current density versus HMDS exposure time.

spectroscopy results reported by Fruehauf *et al.* [19] and the porosity change with time support the higher reactivity of TMSDEA. OTMSA shows the lowest reactivity.

The main film properties influenced by the hydrophobisation are permittivity and leakage current. Silylation leads to a decrease of dielectric constant and of leakage current density with increasing exposure time as shown for HMDS in Figs 8.21 and 8.22.

From the structural investigation, one can conclude that this effect is caused by a continuously increasing number of TMS groups on the aerogel surface and its raised hydrophobicity. Leakage current density follows an exponential time law and is obviously related with silylation rate. *k*-Value change is more difficult to explain, because two opposite tendencies are superposed.

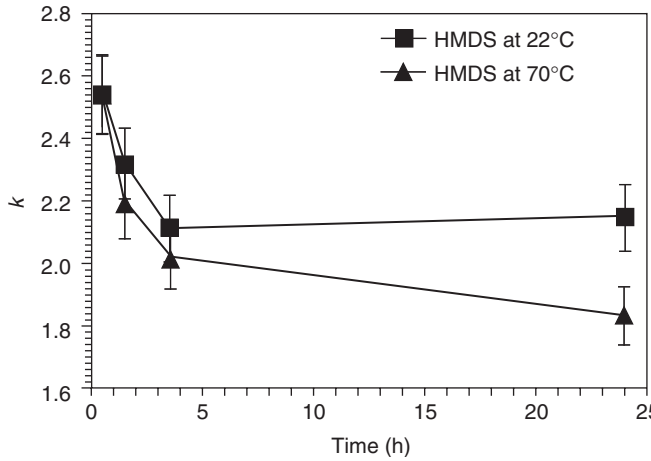

Fig. 8.23 Aerogel dielectric constant versus HMDS exposure time for different temperatures.

Hydrophobization prevents water adsorption. Influence of the high *k*-value of water is thus limited by effective volume of adsorbed water. But *k*-value also depends strongly on absolute initial pore volume of the aerogel layer. Therefore, it would be better to discuss only a relative *k*-value change, but it is not possible to measure the initial value of the untreated samples because of too high leakage currents. Fruehauf *et al.* [19] found that HMDS-treated samples reach the desired limit of 10^{-9} A/cm^2 at shorter exposure times than TMSDEA and OTMSA treated ones. The *k*-value change was reported to be stronger for TMSDEA treatment and scatters for OTMSA without clear trends. Nevertheless, HMDS was found to be the most effective hydrophobising agent reaching low *k*-values and low leakage currents at the same time. An acceleration of the hydrophobisation reaction is achieved by increasing temperature (up to 70°C, see Fig. 8.23 for HMDS) and concentration of hydrophobising agent.

8.2.3 Film properties of porous SiO_x films[1]

8.2.3.1 Film structure and morphology

The structure of the porous material is completely described by the following properties, which are not easy to derive particularly in the nanometer scale pore size materials:

- pore interconnectivity (open/closed porosity)
- pore size and its distribution (PSD)
- skeleton density
- skeleton wall thickness.

[1]The film properties described hereinafter are related to porous SiO_x aerogel films produced with the deposition process introduced in Section 8.2.2.2 using sol B.

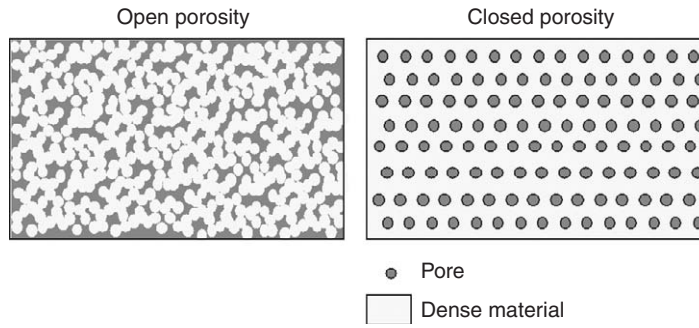

Fig. 8.24 Schematic of the open- and closed-pore structure in a porous material.

The porosity of the films can be distinguished in open porosity resulting from open (interconnected) pores and in full porosity meaning open and closed pores, as visualised in Fig. 8.24. A completely closed pore structure is often discussed to be beneficial for further processing, as process chemicals cannot easily penetrate the material. On the other hand, it allows no inner surface modifications, thus the porous film must be hydrophobic directly after formation. However, most porous films have been shown to have open pores or a mixture of open and closed pores. The porosity of the films can be measured by using very different techniques, like ellipsometric porosimetry (EP) [23], variable angle spectroscopic ellipsometry (VASE) [21], laser-induced surface acoustic wave spectroscopy (LSAW) [24], positron annihilation spectroscopy (PALS) [25], combination of high resolution specular X-ray reflectivity and small-angle neutron scattering (SXR/SANS) [26] or Rutherford backscattering (RBS) [27]. A description of each measurement technique is beyond the scope of this book, the references given in the brackets are related to publications describing or employing the respective technique to porous thin films. Depending on the measurement principle they give different porosities like full porosity, open porosity or a porosity related to a reference density value. Therefore, comparisons have been made between the results of the different techniques by Baklanov and Mogilnikov [28] and Murray *et al.* [27]. Differently processed wafers with SiO_x aerogel were investigated by EP, RBS and LSAW. The resulting porosity is given versus k-value in Fig. 8.25. The measurement by EP proves that the pores are interconnected receiving the same value for open and full porosity. This is also the measurement curve, which fits best to the effective medium approximation (see Section 8.2.1). For both RBS and LSAW, the measured porosity is remarkably higher. In both cases the porosity is calculated using the reference density of SiO_2 (2.26 g/cm^3) to describe the skeleton, which need not be true. Reversibly, that means the skeleton density can be calculated using the different porosities resulting in a skeleton density for this type of aerogel film between 1.39 and 1.46 g/cm^3. A typical pore size distribution (desorption curve) derived from EP for a 55% porosity sample is shown in Fig. 8.26. The desirable pore size is expected to be < 5 nm so that the dielectric behaves as a continuum for the expected interconnect dimensions and does not affect diffusion barriers for copper metallisation. The

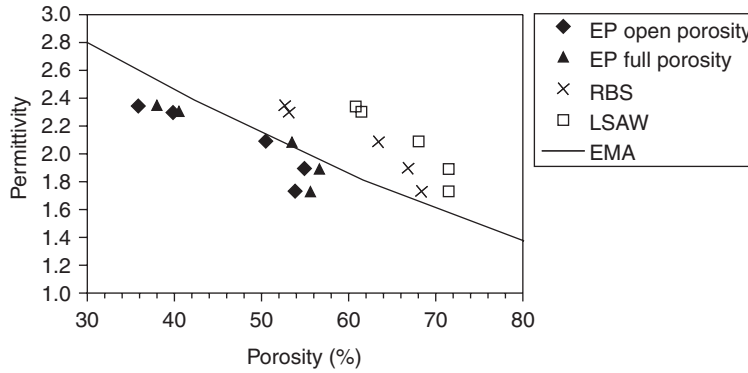

Fig. 8.25 Dielectric constant (permittivity) measured by different techniques for aerogel films of varying porosity.

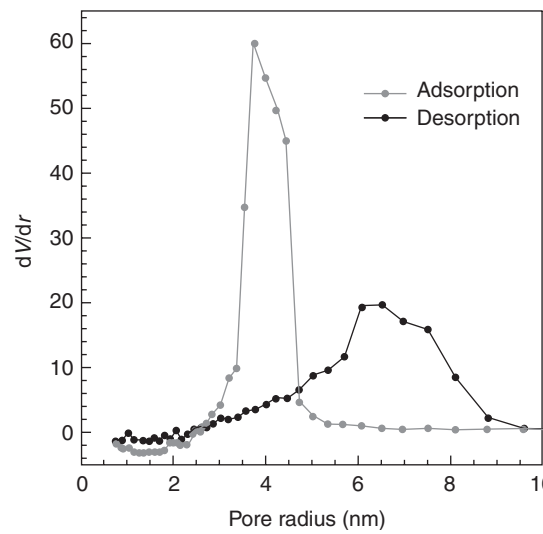

Fig. 8.26 Pore size distribution for porous SiO_2 with 55% porosity measured by EP.

pore size distribution should be tight and show no pores at larger size. For the SiO_x aerogel films described here, the films with increasing porosity have increasing pore size R_{max} in the range of 2.2–3.8 nm and decreasing (inner) surface area as depicted in Fig. 8.27.

8.2.3.2 Chemical composition and structure

The composition of the SiO_x aerogel films was measured by RBS (of particular interest for these films are the concentrations Si, O and C) and elastic recoil detection (ERD) to detect the concentration of lighter elements such as F and H. Table 8.5 gives the RBS/ERD results of two sol B

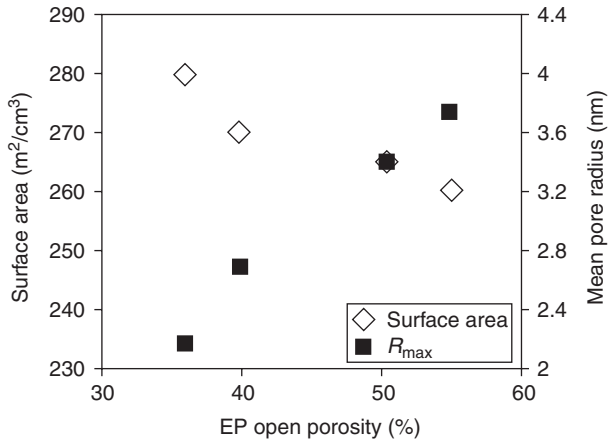

Fig. 8.27 Inner surface area and mean pore radius versus porosity measured by EP [27].

Table 8.5 RBS/ERD chemical composition results for As-deposited and HMDS-treated samples of sol B

Film	O/Si (at)	F/Si (at)	C/Si (at)	H/Si (at)[b]
Sol B as deposited	2.03	0.20	<0.11	0.26–0.13[a]
Sol B HMDS	1.90	0.06	0.24	0.48

[a]Film gradient, first value for the surface share, second value for SiO_2/Si borderline share.
[b]Hydrogen content underestimated by ERD (NRA: ~32 at%).

samples before and after HMDS hydrophobisation treatment. The carbon content in the as-deposited sample is due to the unreacted ethoxy groups. A significant amount of F was found due to a fluorination by the HF catalyst. The carbon and hydrogen content of the HMDS-treated sample is increased due to the silylation of the surface. The hydrogen content is underestimated due to hydrogen release from the porous material during ERD measurement (ion bombardment). Nuclear reaction analysis (NRA) showed a constant hydrogen concentration of ~32 at% over the whole film.

The chemical structure and the surface species of aerogel thin film samples of sol B was obtained with TOF-SIMS. The surface species of the sample sol B as-deposited are identified as Si–OH, Si–F and unreacted $Si–OC_2H_5$. The surface of the sample Sol B after HMDS is mainly covered with methyl groups. A small amount of Si–OH and Si–F as surface species were also found. The combination of both chemical analysis and the results of the RBS measurement show that the chemical structure of presented SiO_2 aerogel is composed of mainly $Si–(CH_3)_3$ for HMDS-treated samples and Si–OH, Si–F, $Si–OC_2H_5$ for unmodified samples as surface species besides the SiO_2 network.

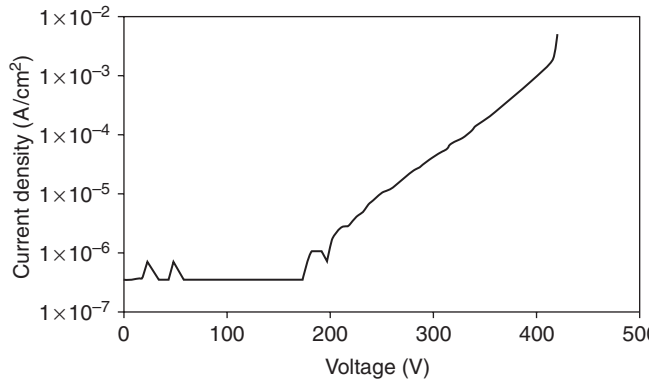

Fig. 8.28 Breakdown behaviour of aerogel thin films measured by mercury probe.

8.2.3.3 Electrical properties

The influence of the processing on the electrical parameters *k*-value, leakage current and field breakdown have already been discussed in Sections 8.2.2.2 and 8.2.2.3. These electrical parameters can be measured without additional preparation by CV-, IV- and breakdown techniques using a mercury probe equipment. Care must be taken if the surface roughness or the pore size is too large, that Hg may penetrate the porous material. Proper process conditions can yield porous SiO_2 films with tunable *k*-values and low leakage and high dielectric strength at the same time. For *k*-values in the range of 1.7–2.8 leakage current densities at 1 MV/cm below 10^{-9} A/cm^2 and electrical field breakdown between 3 and 4 MV/cm are achievable. This is less straightforward compared to thermally grown oxides, but still sufficient for application as interlevel or intermetal dielectric. A significant difference of the electrical behaviour compared to thermally grown SiO_2 was found for the breakdown, which does not show the steep increase of current at breakdown voltage as shown in Fig. 8.28.

8.2.3.4 Mechanical properties

The mechanical properties, mainly the elastic modulus *E*, are important to estimate the ability of the porous dielectrics to withstand the mechanical stress they are exposed to during copper chemical–mechanical polishing (CMP). As the mechanical properties of porous films were shown to scale down following a potential law having an approximate exponent of 3 with porosity [29] it is a critical property with respect to integration of porous dielectrics into IC metallisation. The elastic modulus and hardness were measured using nanoindentation technique for different film porosity. The elastic modulus values obtained are in the range of 1.5–4 GPa as shown in Fig. 8.29. By further optimisation of the process *E*-values of up to 6 GPa were achieved for dielectric constants of about 2.2.

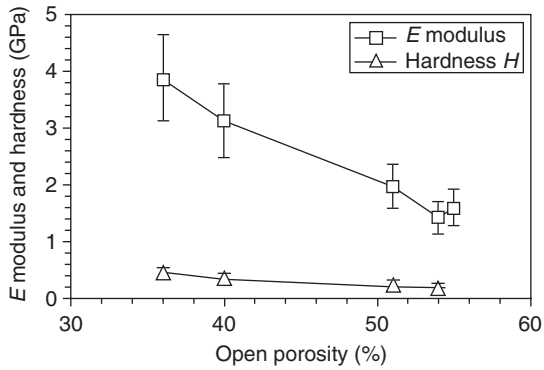

Fig. 8.29 Elastic modulus and hardness for porous SiO_2 aerogel films versus porosity measured by nano-indentation (adapted from [27]).

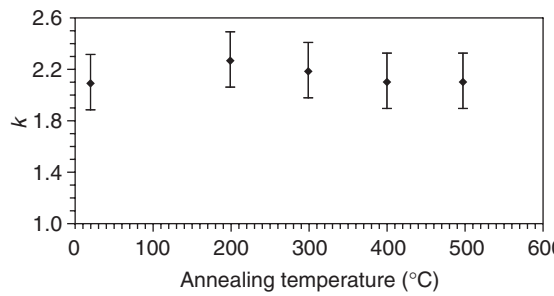

Fig. 8.30 Dielectric constant k of aerogel films at different vacuum annealing temperatures.

8.2.3.5 Thermal properties

FTIR and electrical characterisation indicate that heating HMDS-treated aerogel films to temperatures of up to 500°C for times up to 30 min under vacuum has no serious impact on film surface chemistry or electrical performance. From the FTIR spectra of films treated at 400°C it can be deduced that the amount of surface silanols increases very slightly. The k-value change is not measurable even after 500°C treatment (see Fig. 8.30) and leakage currents stayed below 10^{-11} A/cm^2 (at 5 V) for all samples. Film degassing was evaluated using thermodesorption with gas chromatography and mass spectrometry (TD GC/MS) two times at 400°C for 2 min. The first desorption step led to a film weight loss of 1.3%. Desorbing species were trimethylsilanol, various siloxanes as well as traces of trimethylfluorosilane and aliphatic hydrocarbons. In the second desorption step basically small amounts of trimethylsilanol were detected resulting in a 0.2% weight loss of the porous SiO_2 film. This shows that the material is stable and only small amounts of species related to the HMDS hydrophobisation desorb fast. For further processing of the porous film like cap layer or diffusion barrier deposition, this behaviour is tolerable.

Table 8.6 Thermal conductivity of porous and non-porous silicon oxide films (unless otherwise stated, normal pressure and room temperature)

Material	Thermal conductivity λ (W/m/K)	References
Thermal oxide	1.2	Saxena [32]
PECVD TEOS oxide	0.85	Saxena [32]
O_3/TEOS oxide	0.7	Saxena [32]
Hydrocarbon polymer (SiLK)	0.18	Goldblatt *et al.* [33]
Mesoporous silica (65% porosity)	0.18	Jin *et al.* [31]
Silica xerogel (75% porosity)	0.065	Morgen *et al.* [29]
Silica aerogel (95% porosity, bulk sample)	0.017	Hrubesh and Pekala [34]

Nevertheless, a degas step after hydrophobisation treatment is also possible and minimises outgassing during further process steps.

The reduced thermal conductivity of porous low-*k* dielectrics is a critical parameter which can lead to significant line heating as reported by Streiter *et al.* [30]. The thermal conductivity of a material depends on film thickness, temperature and particularly for porous films on pressure. Compared to conventional intermetal dielectrics (PECVD silicon oxides) the thermal conductivity of highly porous SiO_2 films can be only one-tenth (see Table 8.6), but typically is about 0.18 W/m/K for an integration relevant porosity as shown by Jin *et al.* [31]. Special design may be required to integrate the porous films into interconnect schemes, for example, special heat sinks as proposed by Streiter *et al.* [30].

8.2.4 Integration issues

8.2.4.1 Issues for integration into copper damascene interconnect schemes

Critical issues concerning the integration of porous films into a copper damascene interconnect scheme are shown in Fig. 8.31. The porous structure of that material gives rise to special investigations on compatibility with wet processing, resist processing, deposition of different films onto the porous oxide, etching, CMP and plasma processing. The possible risks with a porous material are penetration of material of adjacent films or process chemicals into the porous film, decreased mechanical stability, sensitivity of surface modified films to plasma processes (loss of hydrophobising TMS surface groups). Furthermore, general compatibility studies have to be performed with respect to outgassing of the film itself, thermal stability and adhesion to adjacent films.

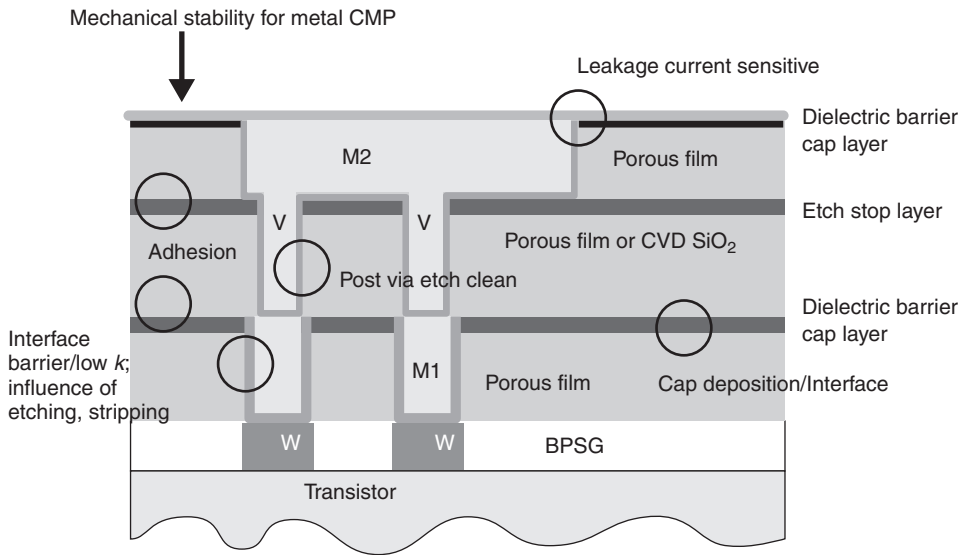

Fig. 8.31 Schematic of a dual damascene copper metallisation scheme using porous low-*k* dielectric.

8.2.4.2 Lithography compatibility

The lithography with resist directly deposited onto the porous oxide showed interactions of the resist with porous silicon oxide. After resist developing using a TMAH-based developer the permittivity increased to undesired values of about 3.6 at the opened areas. The following patterning processes by inductively coupled plasma (ICP) etching using CHF_3/CF_4 chemistry and wet etch by BHF solution were influenced compared to blanket film etch. The dry etch rate for blanket films decreased by a factor of 3 for the same etch conditions, whereas wet etching was impossible at the opened porous silicon oxide areas. These effects can be attributed to the formation of a carbon-rich layer on or in the porous oxide detected by EDX measurements at the opened areas. These results demand a hard mask (cap layer), which usually is deposited by PECVD (see Section 8.2.4.3).

Wet processing of the porous silica is critical due to penetration of the pores with the liquid chemicals. Even if there is no impact on the material itself, evaporation of the liquid is difficult to maintain in penetrated capped areas. Therefore, the effect of the plasma resist stripping process on the aerogel film was investigated. HMDS-treated blanket layers were exposed to an oxygen plasma with different process times to simulate the sidewall of patterned damascene trenches or vias. The influence of such a treatment on the leakage current and the oxide capacitance (permittivity) is depicted in Fig. 8.32. Both leakage current and porous oxide capacitance (and thus permittivity) increase after the oxygen plasma. A repeated HMDS treatment returns both the oxide capacitance and the leakage current to the values before oxygen plasma treatment.

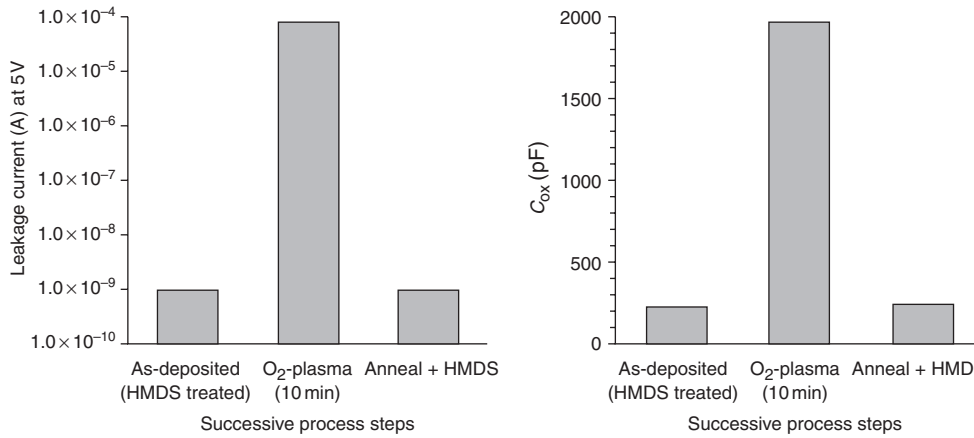

Fig. 8.32 Leakage current (left) and oxide capacitance (right) after deposition and additional O_2 plasma for resist stripping.

Using a 50 nm PECVD SiO_2 cap layer, no impact on the electrical characteristics of the porous silica film has been observed.

8.2.4.3 Capping layer/hard mask deposition

SiO_2 cap layers of 10 and 50 nm were deposited by means of PECVD (SiH_4/N_2O) onto bare wafers and aerogel films. The PECVD process used to deposit the cap layers produces temperatures in the films of about 300°C. The onset of $–CH_3$ thermal oxidation was found by Yang *et al.* [11] to be in the region of 310°C, in correlation with the $–CH_3$ absorption band in the FTIR spectra diminishing to near zero at 500°C. The FTIR transmission spectra of the cap layers on aerogel show no significant variation from the non-capped aerogel layer. The antisymmetrical and symmetrical stretching vibrations of $–CH_3$ reveal that there is no major reduction of the peak intensity after cap layer deposition. This indicates that the deposition process has not removed many of the methyl groups introduced during HMDS treatment and so the hydrophobic nature of the porous aerogels can survive cap layer deposition at these temperatures. The variation of dielectric constant k for various treatments (see Table 8.7) is shown in Fig. 8.33. It can be seen that the only significant impact on the k-value of the films comes with 50 nm SiO_2 deposition and possibly with N_2O exposure. The influence of these treatments on J_{leak} and V_b are shown in Fig. 8.34. The leakage currents for the samples are generally lower than 10^{-11} A/cm^2 (at 5 V) before treatment. Leakage current densities are observed to increase with cap deposition by about an order of magnitude for the 50 nm high power PECVD SiO_2 film. Field breakdown voltages before treatment of 3.1–3.8 mV/cm are slightly reduced after treatment. In general, this cap deposition process does not seriously degrade the electrical qualities of the aerogel films.

Table 8.7 Treatment overview for cap layer evaluation [35]

Sample	Treatment	Temperature (°C)
1, 2	10 nm standard PECVD SiO_2	300+
3, 4	50 nm standard PECVD SiO_2	300+
5, 6	50 nm high power PECVD SiO_2	300+
7, 8	SiH_4 (no plasma)	300
9, 10	N_2O (no plasma)	300

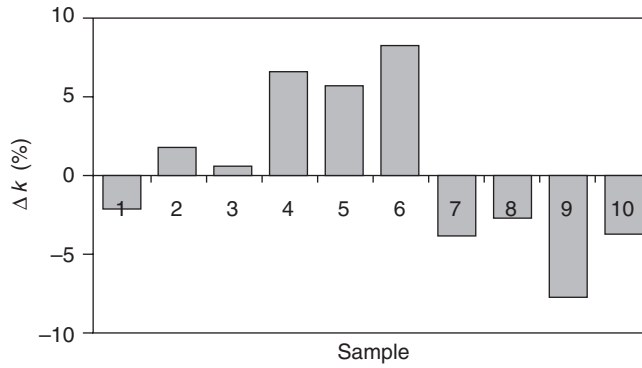

Fig. 8.33 Dielectric constant change after gas treatments or PECVD depositions on aerogel films [35].

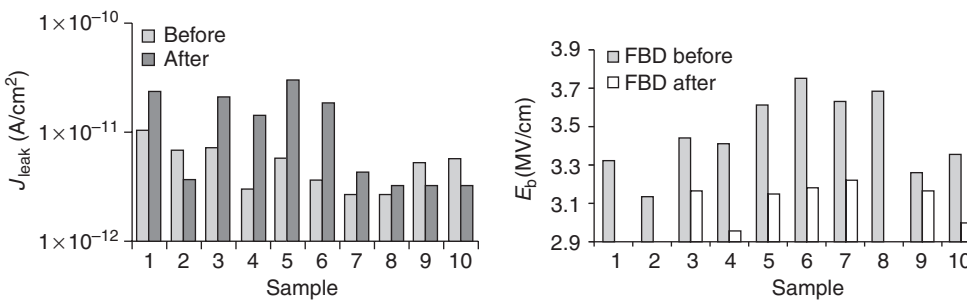

Fig. 8.34 Leakage current density (left) and field breakdown after gas treatments or PECVD depositions on aerogel films adapted from [35].

8.2.4.4 Etching of porous SiO_2 films

In order to integrate this material in the single and dual damascene metallisation, plasma etching processes are indispensable. Competing technologies using conventional etching have recently been developed. Schematics of various single-wafer plasma reactors are described, for instance, by Layadi *et al.* [36]. Recently, reactive ion etching (RIE) systems with ICP for low ion energies are most favourable. Common to all is the use of fluorine containing feed gases (CF_4,

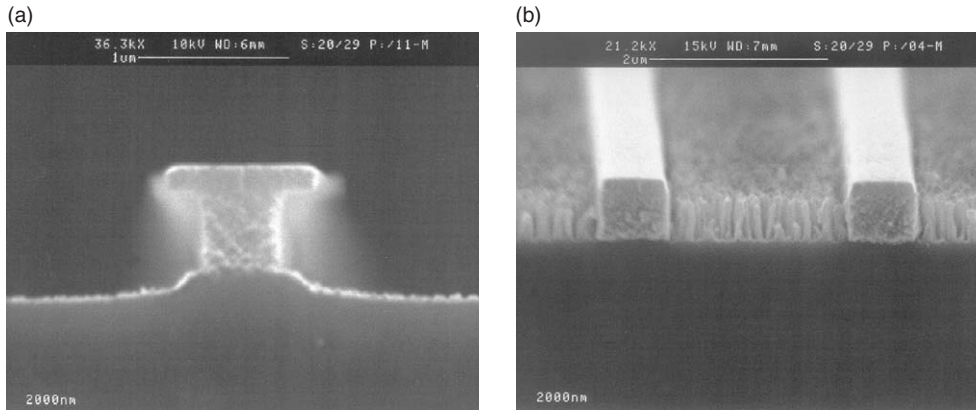

Fig. 8.35 Standard SiO_2 etching: (a) with ICP (b) without ICP.

CHF_3, C_2F_6, C_4F_8 and NF_3) to remove the silica. For instance, Oehrlein *et al.* [37] and Standaert *et al.* [38] described fluorocarbon-based etching processes for porous SiO_2-based low-*k* materials. Following the findings of Wang *et al.* [39], it is possible to achieve both selectivity against other materials and higher etch rates than those of thermal SiO_2. The higher etch rate of porous materials can be understood partly by the fact that the plasma exposed surface increases with the porosity. The advantage of higher etch rates by reason of large surfaces brings at the same time the disadvantage that the chemistry of etching not only occurs on the film surface but also inside. Considering these aspects, several authors [40–42] used mixtures of feed gases (i.e. addition of H_2, O_2 or Ar) in order to overcome this effect and to maintain a flat etch front as well as good sidewall profile with small sidewall roughness.

Details about the process parameters are insufficiently described in literature. Some works were done about the influence of the dc self-bias voltage by Rueger *et al.* [43] and Jain *et al.* [44]. Additionally, our experiments lead us to assume that the ICP conditions strongly influence the undercutting and bowing of porous silica. Figures 8.35(a) and (b) show a standard SiO_2 process with different ICP conditions. Successfully etches single damascene trenches are shown in Fig. 8.36.

At present, efforts are directed towards the integration of porous silicon oxide films with respect to single and dual damascene processes, for example, by Matsuo *et al.* [45] and Mosig *et al.* [46]. Therefore, considerable attention should be paid to the investigation of the impact of hard masks and etch stops.

8.2.4.5 Further requirements for copper damascene integration

Copper diffusion barrier compatibility

TiN barrier layers of 100 nm thickness were deposited on aerogel and PECVD SiO_2 capped aerogel using two methods: (a) DC magnetron sputtering, and (b) MOCVD pyrolysis of

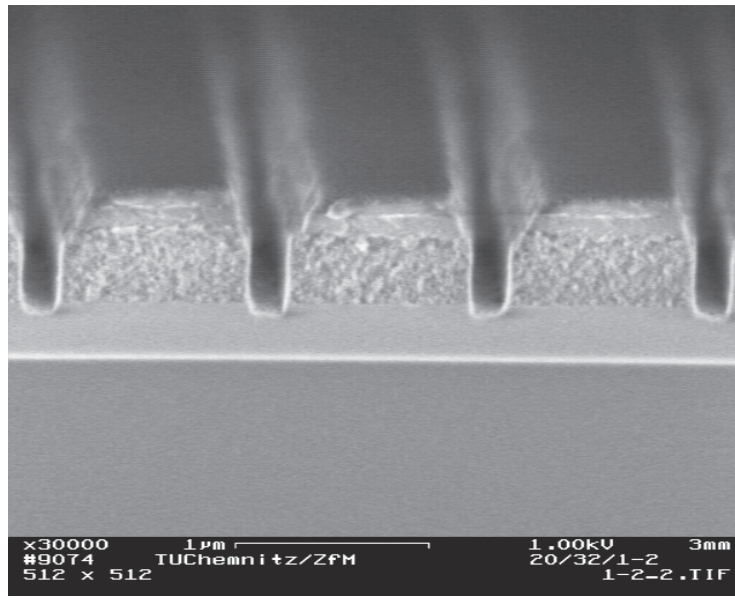

Fig. 8.36 Trenches (200 nm wide) etched into aerogel low-*k* dielectric.

Table 8.8 Processing overview for diffusion barrier evaluation [35]

Sample	Deposition	Substrate	Patterning	Process temperature (°C)
1, 2	Sputtering	50 nm cap on aerogel	Shadow mask	<100
3, 4	Sputtering	Aerogel	Shadow mask	<100
5, 6	Sputtering	Aerogel	Litho/etch	<100
7, 8	MOCVD	50 nm cap on aerogel	Litho/etch	450
9	MOCVD	Aerogel	Litho/etch	450

TDMAT employing an H_2/N_2 densifying plasma for the initial and final 20 nm. The temperature experienced by the films during sputtering and MOCVD were <100 and 450°C, respectively. A shadow mask was used during some sputter depositions to produce dot structures while lithography and etching of blanket films was used for other sputtered and MOCVD TiN samples. After etching the TiN, the photoresist was not removed from the dots to prevent any influence from the resist stripper. This made leakage current measurements at these samples unreliable due to wide variations in the measured values. The effects on the aerogel of each variant described in Table 8.8 were examined.

The variation of *k* for each variant is shown in Fig. 8.37. In general it can be seen that the greatest change in *k* occurred for lithographically processed TiN depositions on bare aerogel (samples 5, 6 and 9). It was thought that TiN etching during the lithographic process

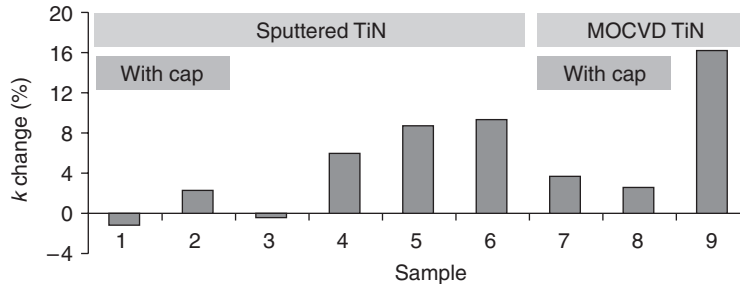

Fig. 8.37 Relative change of dielectric constant k after diffusion barrier deposition using different processes on capped and non-capped aerogel compared to the untreated state [35].

might be responsible for the apparent increase in k. This was tested by exposing an evaporated aluminium dot on aerogel to the TiN etch. This did not produce an appreciable increase in k. Therefore, these effects must be related to the deposition itself. In comparison, deposition onto capped aerogel did not greatly increase the k-value of the aerogel. Leakage current densities for shadow mask samples 1–4 were unchanged with respect to their untreated aerogel reference samples and were in the 10^{-11} A/cm^2 range. From these results it can be concluded, that sputtering and MOCVD TiN deposition onto the capped aerogel does not deteriorate the electrical properties of the low-k dielectric, whereas MOCVD TiN deposition directly onto the porous material might be critical. It is not clear, if the reason for the increased k-value results from the process chemistry or from plasma damage during the TiN plasma densification steps.

Copper CMP on porous SiO_2 dielectric

Copper and barrier CMP requires a protective cap of the porous low-k material to prevent the slurry to penetrate into it. This cap can provide a polish stop (e.g. SiN or SiC:H) or must be of sufficient thickness to provide protection during overpolish (e.g. SiO_2).

Having examined the chemical and electrical interactions of the aerogel material during processing, the next issue to be addressed is its mechanical stability during CMP. The CMP process induces complex mechanical stresses in the aerogel material. As a first attempt, different types of 500 nm thick silica aerogel films with varying porosities ($\pi = 40\%, 55\%$; $k = 2.6, 2.1$) were capped with a 100 nm PECVD SiO_2 layer before being patterned. The features were lined with a 20 nm TiN barrier layer before being filled with 600 nm MOCVD Cu and 500 nm PVD Cu (Fig. 8.38). The copper and TiN were then polished back to the SiO_2 cap layer. The aerogel films with larger dielectric constant (2.6) are less porous and therefore mechanically stronger. In general, the films with lower porosity survived the CMP process very well. However, the more porous films ($k < 2.2$) have somewhat weaker mechanical strength leading to the possibility of cohesive breaking within the porous layer itself. Nevertheless, only in larger non-patterned areas (which are usually avoided by introducing dummy patterns in a CMP-consistent design)

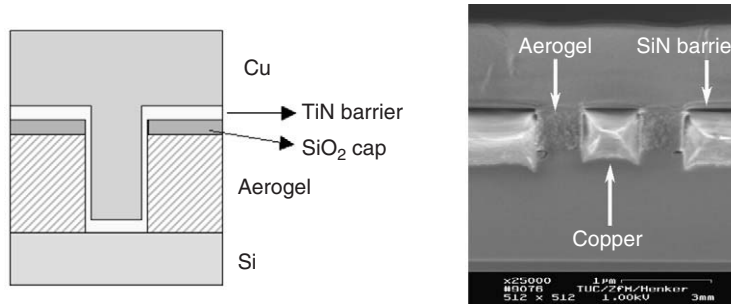

Fig. 8.38 Schematic of the structure before Cu CMP and cross-section SEM of polished single damascene structures in low-*k* aerogel film.

defects due to film delamination were observed. More work is required to optimise the CMP process for lower *k*-value films and to improve the mechanical stability of the porous films.

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Chapter 9
Nanoporous dielectric films: fundamental property relations and microelectronics applications

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Abstract

Porous materials have been proposed to replace dense SiO_2 as the interlayer dielectric in future microelectronic devices. The properties of any porous material depend upon the material's microstructure and process history. For a fully connected material, the elastic modulus should vary with the square of the density and thermal conductivity, like the dielectric constant, should vary linearly with density. Any defects in the structure of the material tend to increase the dependence of the property of interest on the density or porosity. The adhesion between layers, the stability of a layer deposited on a porous material, and interdiffusion between layers depend upon the porosity of the material and the intermolecular forces governing the strength of the interaction between the layers. Adhesion also depends upon intrinsic stresses in the layers and the ambient environment. Adhesion and stability of Cu films are better on xerogel films compared with solid SiO_2. Cu may diffuse into porous materials under electrical bias. We show that diffusion depends upon the surface chemistry of the material as well as its porosity. Leakage currents and *C–V* curve shifts were larger with an Al electrode than with a Cu electrode for silica xerogel-based capacitor structures. When the organic capping groups are removed from the xerogel prior to metal deposition, *C–V* tests indicate Cu ion diffusion at temperatures as low as 100°C. We discuss a model of diffusion through porous solids that successfully simulates the current observed during BTS testing of silica xerogels and may be extended to apply to polymers.

9.1 Need for low-κ materials

The semiconductor industry depends on continually making chips faster and cheaper. As early as 1965, Intel's cofounder Gordon Moore predicted that the speed of chips would keep doubling

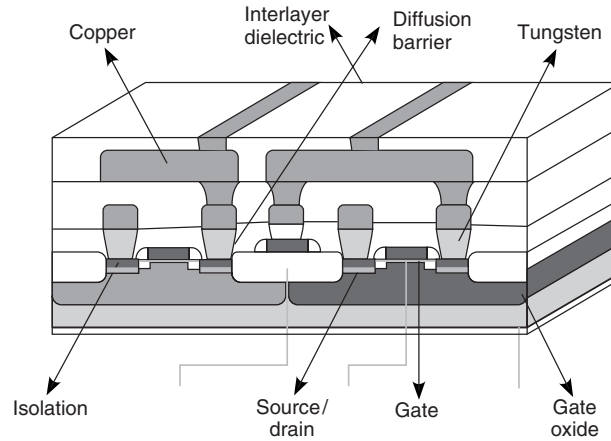

Fig. 9.1 A simplified cross-section of an IC showing the transistor (made up of source, gate, and drain) and the various levels of interconnect [61].

every 2 years in response to the demand. The industry has maintained this kind of growth by a continuous reduction in the gate length of transistors. The gate length determines the device technology generation and as it shrinks, more transistors per unit area are built and more interconnections between those transistors are necessary.

The interconnects between transistors are made up of thin metallic wires (Al or Cu) and have thin dielectric films isolating them from each other to prevent shorts (see Fig. 9.1). Traditional interconnect materials are aluminum (metal) and dense silicon dioxide deposited by chemical vapor deposition (CVD) (dielectric).

For much of microprocessor history, interconnects were not an issue. However, Fig. 9.2 indicates that for future device generations (180 nm and beyond), increase in the speeds gained by the reduction of the gate delay are being offset by the increase in the interconnect delay [1]. Thus, as in all transportation infrastructure systems, as population density increases, travel delays increase. The interconnect delay is represented by the RC time constant where R is the resistance of metal lines and C is the capacitance of the dielectric. Assuming the metal spacing is equal to the metal width (W), and that the interlayer dielectric (ILD) thickness is equal to the metal thickness (T), with a dielectric constant κ and the metal resistivity ρ, then an interconnect of length L will have a product of resistance R, and a capacitance C of

$$RC = 2L^2\kappa\rho\varepsilon_0\left[\frac{1}{W^2} + \frac{1}{T^2}\right] \tag{1}$$

where ε_0 is the permittivity of free space $= 8.85 \times 10^{-12}$ F/m. Reducing the RC constant would help to alleviate the problems of interconnect delay and would also reduce cross-talk, noise, and

power dissipation in the chip. Sakurai [2] has developed closed-form expressions for transition time of *RC* interconnection, coupling capacitance and the crosstalk voltage height. The crosstalk coupling capacitance and the voltage heights are found to be proportional to the dielectric constant of ILD. Power dissipation (P) in VLSI circuits is approximated by

$$P \propto 2\pi f V^2 C \tan(\delta) \tag{2}$$

where V is the voltage, f is the frequency of operation, and tan δ is the dielectric loss tangent. This is only an approximate expression, the actual estimation of power dissipation is much more complex [3] and $\tan(\delta)$ depends on the chip design. To reduce the *RC* delay, one must reduce both the resistivity of the metal and the dielectric constant of the dielectric. Copper has proved to be a viable solution as an alternate metal [4, 5], but no new dielectric material [6–8] has emerged as the clear winner. The predicted minimum feature size and the needed effective dielectric constants for the next decade are shown in Table 9.1.

In this chapter, we will explore a range of low-κ materials currently being developed and tested. We will focus on nanoporous silica xerogels as a benchmark since that material has been the most widely characterized. We will discuss the properties of low-κ materials and consider dielectric and optical properties, mechanical properties, thermal properties, and finally the interactions of these low-κ materials with proposed barrier and metallization layers. Throughout we will also review the models that have been developed to correlate experimental results and eventually to predict the properties and behavior of new low-κ materials.

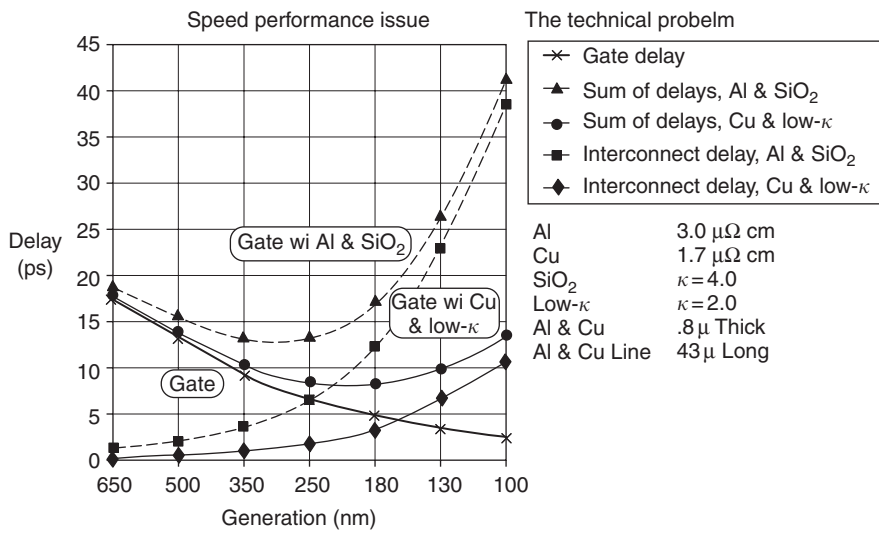

Fig. 9.2 Calculated gate and interconnect delay versus technology generation. (Adopted from the International Technology Roadmap for Semiconductors 1999).

Table 9.1 Dielectric constant requirements

Year of technology generation	1999	2002	2005	2008	2011	2014
Technology node (nm)	180	130	100	70	50	30
ILD dielectric constant	3.5–4.0	2.7–3.5	1.6–2.2	1.5	<1.5	<1.5

9.2 Types of low-κ materials

A summary of some of the leading candidate materials is given in the Table 9.2 [9–12]. We can conveniently separate the candidates into three broad areas: polymeric or organic coatings, inorganic coatings, and hybrid organic/inorganic materials. In each category, we can split the materials into two additional types, porous and non-porous. There are several ways of making a material porous and all involve removing a solvent or other sacrificial material and leaving behind a porous matrix.

9.2.1 Organic materials

Maeir [13] has given an excellent review of all candidate polymeric low-κ materials. A brief description of some of these are given below.

9.2.1.1 Poly(aryleneethers) (PAE) and fluorinated poly(aryleneethers) [14–16]

Several polymers from this class have been studied extensively [14]. Typically, dielectric constants of 2.8 are achieved. Recently, porous PAE films have been prepared where abietic acid is used as sacrificial solvent [15, 16] to make them porous.

9.2.1.2 Parylene N and Parylene F

Parylene N (κ~2.7) is a poly(*p*-xylylene) while Parylene F (κ~2.4) is the fluorinated analog where all the methylene units are replaced with difluoromethylene units. Parylenes are synthesized by thermally cracking the precursor dimers in the vapor phase, followed by condensation and polymerization on a cold substrate (at or below room temperature). Parylene has an exceptional gap filling capability and also gives conformal, pin-hole free films with good moisture barrier properties. However, the complexity of the integration issues, may prohibit its use in future devices.

9.2.1.3 Polyimides and fluorinated polyimides [14]

They have among their advantages, a low-κ (2.6–2.8), fairly high glass transition temperatures ($\geqslant 350$°C), relatively low moisture absorption, and high thermal stability. However, their main

Table 9.2 Leading ILD candidates

Deposition method	Dielectric constant, κ				
	4.0	3.5	3.0	2.5	2.0>
CVD inorganic	SiO_2 (4.1)	SiO_xF_y (3.4–4.1)		Black Diamond/Coral (2.2–2.7) $SiO_x(CH_3)_3$ (2.4–3.0)	
CVD organic				Parylene AF4 (2.25) Amorphous fluorocarbon (2.1–2.5)	PTFE (1.9)
Spin-on inorganic			HSQ/MSQ (2.7–3.1)	Nanoglass (1.8–2.5) Mesoporous silica (1.3–2.5)	Xerogel (1.2–3.9)
			Silicon-based polymer (2.8–3.0)	BCB, SiLK (porous) (<2.65)	PTFE (porous) (<1.9)
Spin-on organic			Polyimides (porous, fluorinated) (<3.1)	Polyarylene ethers(porous) (<2.6–2.8)	Porous organosilicate (<2.2)

drawback is that they exhibit a high degree of anisotropy leading to a large difference in in-plane and out-of-plane dielectric constant, index of refraction, and mechanical properties [14].

9.2.1.4 Bisbenzocyclobutene (BCB) [17, 18]

These polymers are fabricated from thermally induced Diels–Alder polymerization of 1,3-divinyl-1,1,3,3-tetramethyldisiloxane-bisbenzocyclobutene. Nierynck *et al.* [17] have demonstrated integration capability of BCB with copper. However, the thermal stability of BCB is not sufficiently high to withstand the high-temperature process steps encountered in actual chip fabrication. BCB is successfully used in processes with less stringent thermal stability requirements, such as in packaging, and in GaAs integrated circuit interconnects [18].

9.2.1.5 SiLK™

SiLK™ [18, 19] (short for Silicon Application Low-κ Material) is a spin-on aromatic polymer with the good thermal stability (up to 475°C), a wide process window, a high glass transition

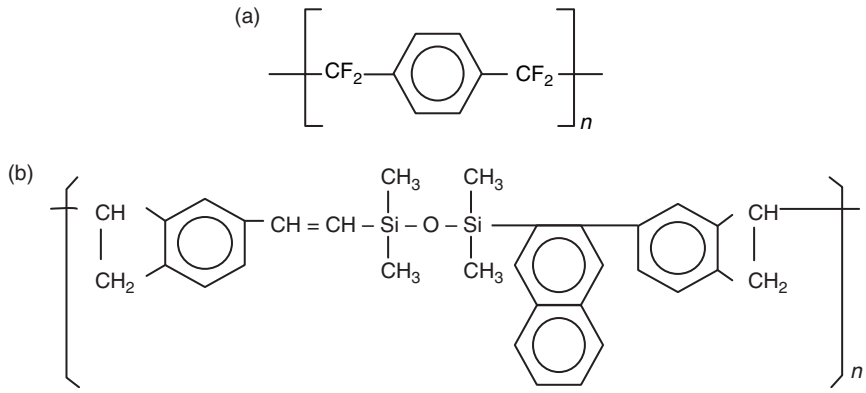

Fig. 9.3 (a) Structure of Parylene-F, (b) Structure of BCB [61].

temperature (490°C), and a low dielectric constant ($\kappa \sim 2.65$). The material has been made porous using a sacrificial material technique, and integrated with Cu in a single Damascene structure [20]. However, the dense material has a rather low thermal conductivity [21] and a low elastic modulus [22].

9.2.1.6 Amorphous fluorocarbons [23, 24]

These materials are deposited by the CVD process using fluoromethanes as precursors [23]. Recently, the porous variety of these films with a very low dielectric constant has been made using a sacrificial technique [24]. The concerns with these materials are the same as fluorinated oxides.

9.2.1.7 Teflon AF [25, 26]

Teflon films can be deposited either by spin coating [25] or CVD [26]. The spin-coated films are deposited from an emulsion containing sub-20-nm polytetrafluoroethylene (PTFE) particles and surfactant. They can also be deposited by CVD using thermal activation of the precursor. The dielectric constant is 1.9; the lowest attained using a non-porous organic material. The drawbacks of Teflon are its poor adhesion to virtually any other material, and low glass transition temperature, which causes the material to slowly creep over time, even at room temperature.

9.2.2 Inorganic materials

9.2.2.1 Fluorinated oxides (SiOF) [27, 28]

These are SiO_2 films deposited by CVD with about 2–10 at% fluorine incorporated in them. The F lowers the dielectric constant to between 3.7 and 3.0, which is related both to the amount of fluorine as well as to the steric positioning of the F atom. Care must be taken to ensure that

fluorine is stable in these materials, that is, it will not segregate or react with the adjacent materials. These issues have been addressed adequately in recent years, and fluorinated oxides are already in production in some of today's microcircuit technologies as an interlayer dielectric.

9.2.2.2 Air gap structures [29]

The formation of air gaps uses a feature of plasma-enhanced chemical vapor deposition (PECVD) processes, namely its bad step coverage. First, a thin liner of SiO_2 is deposited using a standard PECVD process with bad step coverage. For small gap structures, pinching off the top of the gaps forms a void. At wider spacing, the gap stays open. The fill of open gaps and sealing of incompletely closed gaps is done by a planarizing dielectric, for example, HSQ. The subsequent deposition of a capping oxide followed by a CMP polishing step provides [29] the necessary planar structure.

9.2.2.3 Porous silica materials [30–40]

Introducing porosity in the materials is the only approach to achieve dielectric constants much below 2.0. Porous materials are divided into two main types: open and closed-pore structure materials. Open pore structured materials under consideration include silica xerogels (also called Nanoporous Silica™ [30], mesoporous silica films [31–35]). These materials are formed by sol–gel processing of alkoxysilanes, followed by evaporation of the solvent. Usually, the internal surface of porous silica must be chemically modified to render the material hydrophobic. The surface modifier, therefore, gives some organic character to the material, and for this reason, porous silica is sometimes classified as a hybrid material. Porosity can be achieved via a random polymerization approach [30, 36, 37] or templated approaches [31–35]. The templated approaches using surfactants, polymers, or nanoparticles produce a more ordered array of pores but require removal of the templating agent by dissolution or calcination. Closed pore films are synthesized by burning or dissolving an organic component from the silicate matrix [35] but there is a limit (percolation threshold) to the porosity (~20–25%) above which the structure becomes open-pore. Mesoporous films are prepared by the condensation of a silicate network around a surfactant micelle. Pore formation occurs when the surfactant micelle is burnt out leaving the shell of the condensed silicate in place. Bruinsma *et al*. [31], Fan *et al*. [33], and Zhao *et al*. [38] also report on the fabrication of surfactant templated porous silica films. Birdsell *et al*. [39] reported on the fabrication of porous silica films prepared from commercially available colloidal silica and potassium silicate. As prepared films have porosity exceeding 85% and $\kappa < 2.0$. However, it is necessary to leach the films prior to electrical testing in order to remove the alkali ions introduced during fabrication. Recently, porous silica zeolite low-κ dielectric films have also been prepared [40]. These films are claimed to have ordered structures and very high modulus and hardness.

9.2.3 Hybrid materials

Hybrid (organic–inorganic) materials offer the promise of tailoring properties between those of organic and inorganic materials. If the organic is added as a non-hydrolyzable, pendant group (network modifying), the mechanical properties of an inorganic material and the chemical properties of an organic material are achieved. Thus, the material can be made hydrophobic, or chemical functionality can be added, without changing the matrix or other essential material properties. By incorporating organic material carrying reactive groups into an inorganic, usually silica-based, matrix (network-forming), the properties can be tailored between those of organic materials and ceramics [41]. Some synonyms used for these materials are ormosils (organically modified silicates), nanocomposites, and ceramers (ceramic polymers). Organic components reduce the dielectric constant by virtue of their chemical nature, but also by creating some free volume in the dielectric material. They also promise a low-κ dielectric with less porosity than would be needed with inorganic materials since the dense material has a lower dielectric constant than silica.

9.2.3.1 Organosilicate glasses (OSG) [42, 43]

Hybrid materials can be deposited from the gas phase by CVD. These are generally non-porous, carbon- or methylene-doped SiO_x films (SiOC), such as Applied Material's Black Diamond™ or Novellus's Coral™ dielectric, with κ in the vicinity of 2.7. These are deposited by CVD using tetramethylsilane or trimethylsilane as precursors. As-deposited OSG films are hydrophobic, and etching, stripping, and cleaning processes must be precisely tuned to keep the material hydrophobic [42]. These films can be made porous if two chemical constituents are vapor deposited and one of them is later burnt out to leave behind porosity in the film [43].

More common is the deposition of hybrid materials by wet sol–gel processing. *Sol–gel materials* are usually porous, although they can be made dense as well. The internal surface of the porous materials can easily be chemically modified.

Researchers at IBM Almaden Research Center [35, 44, 45] have investigated the use of nanophase-separated, closed pore, inorganic–organic hybrid polymers with κ below 3.0 for use as ILD materials. These materials were prepared from reactively functionalized poly(amic ester) derivatives and substituted oligomeric silsesquioxanes. These hybrid materials are reported to be thermally stable to at least 400°C and comparatively tougher than organically modified spin-on glasses without significantly affecting other important polymer properties of the silicates. To prevent phase separation on a macroscopic scale, the thermoplastic polymer (a three-dimensional dendritic molecule) is chemically incorporated into a growing silicate, during condensation. This approach toughens the silicate network and prevents shrinkage and cracking during drying [46]. After burning out the dendritic polymer, it is claimed that small (< 5 nm) closed pores (till about 20–25% porosity) are generated (Fig. 9.4) These films are also called Dendriglass™ for this reason. Recently, Yang *et al.* [47] have formed porous silsesquioxanes with

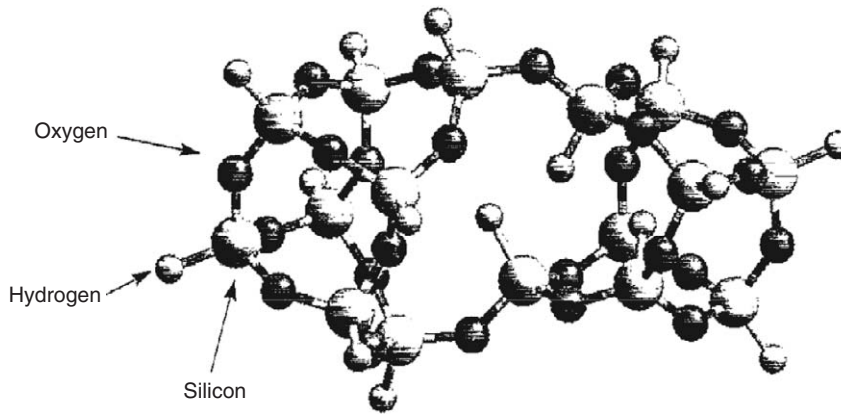

Fig. 9.4 A proposed structure of porous MSQ, *DendriGlass*™ [46] (reprinted with permission).

ultralow dielectric constants (≈1.5) by using triblock copolymers as templates and tailoring their microphase separation.

9.2.3.2 Silsesquioxanes (T-resins) [48–50]

These are sol–gel materials with stoichiometry $(RSiO_{1.5})_n$. They are obtained by hydrolytic condensation of trifunctional silanes, such as $RSiCl_3$, or $RSi(OMe)_3$. These materials can be conveniently divided into two categories depending on their carbon content. Hydrogen silsesquioxanes (HSQ) contain little or no carbon and are derived trialkoxysilanes with $\kappa \approx 3$, and high glass transition temperature. An example is FOX™ dielectric by Dow Chemical. Methyl silsesquioxanes (MSQ, spin-on glass) contain carbon and are prepared from methyltrialkoxysilanes. The structure after cure has a methyl atom covalently bonded to each silicon atom. These materials exhibit $\kappa < 2.7$, good gap fill, high thermal stability, and a good resistance to the type of harsh chemical environments encountered in post-etch cleaning and CMP [49]. An example is HOSP™ by Honeywell, with $k = 2.6$. Porous silsesquioxanes are now available, with lower κ, but compromised mechanical strength. JSR XLK™ is an example of porous HSQ with $\kappa \sim 2.2$. Aoi [50] reports on the synthesis of porous films by addition of a triphenylsilanol (TPS) moiety to a commercially available spin-on glass. Pore formation occurs due to the steric hindrance of the TPS moieties. The TPS moieties are burnt out to leave pores about 80 nm in diameter and $\kappa \sim 2.3$.

9.2.3.3 Bridged polysilsesquioxanes [51]

These materials are porous or non-porous and contain an organic group between two trialkoxy groups in each monomer unit [51] (See Fig. 9.5). Faster gelation (due to six reactive groups in the monomer unit), and better control of organic incorporation (in the monomer) make them a

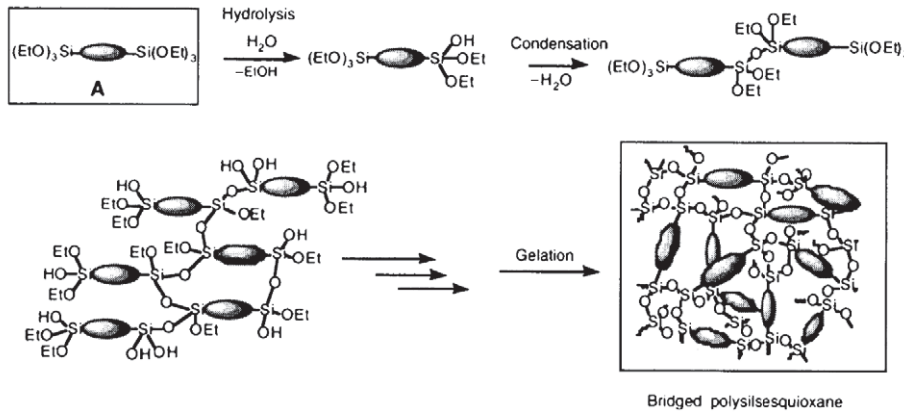

Fig. 9.5 Formation of bridged polysilsesquioxanes [51] (reprinted with permission).

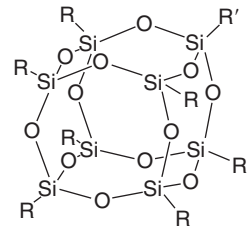

Fig. 9.6 An example of POSS monomer [52] (reprinted with permission).

particularly attractive option, not only as dielectrics. Bridged sisesquioxanes containing organic dyes have been prepared for waveguide, non-linear optics, laser applications, and optical storage (photochromism) [41, 51].

9.2.3.4 Polyhedral oligomeric silsesquioxanes (POSS) [52]

These are a new class of materials with rigid, cage-like cyclic siloxane monomer units. Monomers with various functional groups are now commercially available [52]. Incorporation as pendant units to polymer chains has been suggested to reinforce the polymer thermo-mechanically or improve processability (See Fig. 9.6).

9.3 Electrical and optical properties of nanoporous dielectric films

The chief electrical properties of interest for interlayer dielectrics are the (i) dielectric constant, (ii) dielectric loss tangent, and (iii) the dielectric breakdown strength. For transparent dielectrics, the dielectric constant appears to be linearly related to the refractive index via the

density or porosity of the material and correlations developed for bulk dielectric materials appear to hold for films too [36]. Hrubesh *et al.* [53] obtained the following empirical correlation relating the dielectric properties of bulk silica aerogels (porous silica, with solvent removed by supercritical drying) to their density, ρ, and their refractive index, η, in the microwave frequency range (2–40 GHz).

$$K_{\text{gel}} = 1 + 1.48\rho_{\text{gel}}(\text{g/cm}^3) = 1 + 7.1(\eta_{\text{gel}} - 1) \tag{3}$$

Da Silva *et al.* [54] have measured the dielectric constants of bulk gels prepared with tetramethoxysilane (TMOS) as the precursor. They report a value of 2.0 for samples with a porosity $> 80\%$. Bresch *et al.* [55] measured κ on bulk samples at 1 kHz and also found a linear dependence on the density of the films.

9.3.1 Electrical properties

The dielectric constant of a porous material is dependent on its porosity and water content (chemistry). Several investigators have measured the dielectric constant of nanoporous silica films. Jo *et al.* [56] reported a dielectric constant value of 2.15 for a supercritically dried, aerogel film with a porosity of 67.5%. Annealing to remove bound water decreased this value to 2.07. Yang *et al.* [57] reported that the dielectric constant of their silica xerogel film made by ambient drying using surface modification showed a minimum of 2.2 for an annealing temperature of 300°C. Chow *et al.* [58] processed an organic–inorganic hybrid silica xerogel without surface modification and report high κ values that range from 5.7 for an unbaked sample to about 3.8 for a sample baked at 200°C for 2.5 h in N_2. Ramos *et al.* [59] calculated that the presence of a few weight percent water in a xerogel film dramatically increases the dielectric constant for a hydrophilic film. Figure 9.7 shows the measured κ as a function of film porosity for silica xerogel materials from Jain *et al.* [60]. The values agree with the correlation given in Eq. (3). In fact, after fitting the data the correlation obtained is $\kappa = 1 + 7(\eta - 1)$. This suggests negligible levels of free or bound moisture in the xerogel films. The dielectric constant range for other films are given in Table 9.2.

When an alternating voltage is applied to a 'perfect' dielectric, current flows 90° out of phase with the voltage. No insulating material is perfect, so the current lags behind the voltage by more than 90°. The loss tangent (or dissipation factor) is the tangent of the angle by which the current deviates from the ideal of 90°. It is equivalent to the ratio of the current dissipated in heat to the current transmitted. Thus, loss tangent determines the quality of the dielectric in terms of the dissipation of the signal into heat. Good dielectric materials have small loss tangent. The loss tangent depends on temperature, frequency, and the moisture content.

Hrubesh *et al.* [54] reported loss tangent values for bulk silica aerogels in the range of 0.0005–0.07 and a dramatic effect of the adsorbed water on loss. Birdsell *et al.* [62] measured κ and loss for 85% porosity films made from colloidal silica as a function of frequency and found

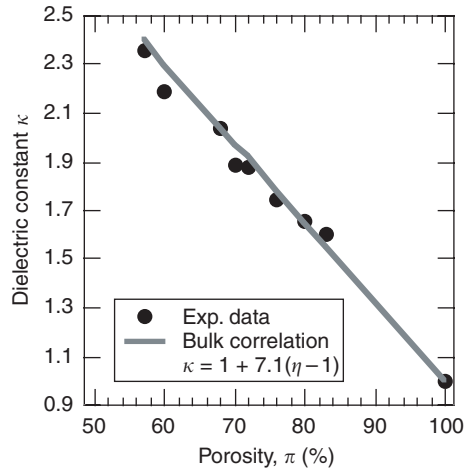

Fig. 9.7 Porosity correlation for xerogel film and comparison with Hrubesh correlation [60] (reprinted with permission).

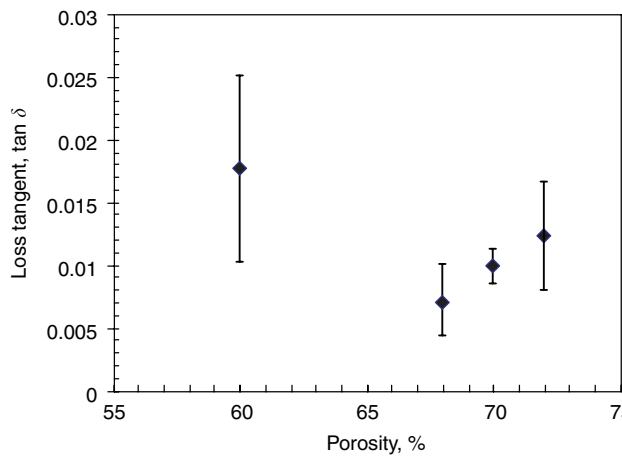

Fig. 9.8 Loss tangent measurements at 1 MHz for xerogel films of different porosity measured under ambient conditions [61] (reprinted with permission).

the loss to be 0.04–0.16. These high values suggest that they have moisture absorption in their films. Figure 9.8 shows average values of the loss as a function of porosity from Jain [61]. The complete set of values lay in the range 0.0004–0.06, suggesting low dissipation factors and high quality factors (the inverse of the loss tangent).

The breakdown strength measurement of bulk xerogels has been reported by Bresch *et al.* [55] to be greater than 0.5 MV/cm. Warren *et al.* [63] report on the measurement of the breakdown strength of dense films prepared without surface modification, with hydrolysis ratios

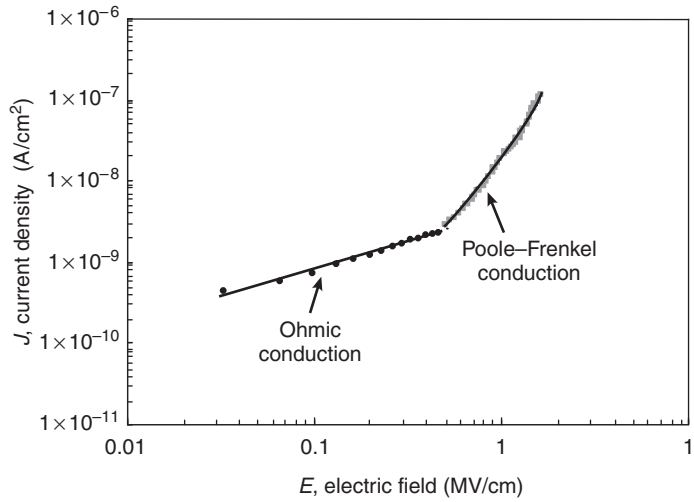

Fig. 9.9 J versus E characteristics of a 60% xerogel film. The leakage current shows Ohmic conduction behavior at low fields [61] (reprinted with permission).

(moles H_2O to moles TEOS) varying from 2 to 20. They found that the breakdown strength increased from a value of 0.1 MV/cm for an R of 2 to about 3.5 MV/cm for an R of 12.5. Chow *et al*. [58] measured the breakdown strength of their hybrid organic–inorganic films and found that it was on the order of 3.4 MV/cm. Jo and Park [64] studied breakdown behavior of supercritically dried silica aerogel films of 70% porosity. The dielectric strength was found to increase after annealing to 450°C. The breakdown strength was >1 MV/cm for most of the capacitors. However, there have been no studies detailing the breakdown behavior of surface-modified xerogel films. Jo and Park [64] studied leakage current behavior. They found that conduction was Ohmic, that is, the current/electric field relationship followed Ohm's law, for low applied fields and that a Poole–Frenkel or breakdown mechanism existed at high fields [65, 66]. Figure 9.9 shows the leakage current characteristics (J versus E) of a 60% xerogel film [56]. These show that for low fields (<1 MV/cm), the behavior is Ohmic since a log–log plot of J versus E gives a straight line. For high fields (>1 MV/cm), $\log(J/E)$ versus $\sqrt{E}$ gave a straight line indicating Poole–Frenkel conduction where $J/E \propto \exp(\sqrt{E})$ [65] for high fields.

9.3.2 Optical properties

Porous materials can also be used as cladding for optical waveguides and waveguide sensors [60, 67, 68]. In these applications, absorption and scattering losses are important. The prism coupling technique [69] was used to measure planar waveguide losses at 650 and 830 nm and catalog the number of waveguide modes. Table 9.3 lists the various waveguide structures that were made

Table 9.3 Parameters for planar waveguides on xerogel with 40% porosity [60]

Core material	Core thickness (μm)	Δn	No. of modes, predicted/observed
Oxide at 150°C	0.94	0.19	2/1
Oxide at 175°C	0.78	0.18	2/1
Oxide at 200°C	0.94	0.19	2/1
Oxide at 225°C	0.88	0.18	2/1
Oxide at 250°C	0.94	0.18	2/1
Oxide at 300°C	0.94	0.19	2/1
Alkoxysiloxane	2	0.23	5/3

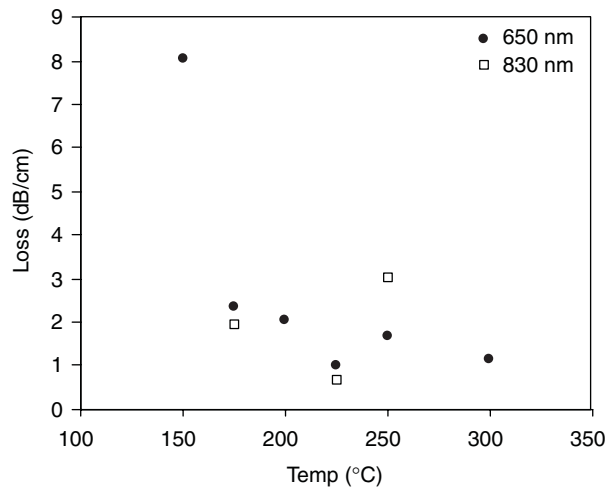

Fig. 9.10 Losses for oxide–40% porous xerogel planar waveguides at 650 and 830 nm [60] (reprinted with permission).

using a 40% porous xerogel as the cladding and Fig. 9.10 shows the planar waveguide loss measurements for the oxide–40% porous xerogel waveguides at 650 and 830 nm. It was found that the oxide deposited at higher temperature gave films with less loss. This implies that the oxide deposited at lower temperatures is of poorer optical quality, most likely due to moisture absorption at unsaturated Si sites. Losses were also dependent upon the adhesion of the core material to the xerogel cladding. Higher porosity xerogels had fewer attachment points for adhesion of the core layer and hence higher losses or complete failure of the waveguide. The planar waveguide losses for the polymer-xerogel waveguides were less than 0.5 dB/cm, 0.5 dB/cm being the current limit of the loss measurement setup. Adhesion of the polymer was better to the xerogel perhaps due to the low intrinsic stress of the as-deposited polymer.

9.4 Mechanical properties of nanoporous dielectric films

The mechanical properties of porous materials depend on their microstructure and overall degree of porosity, Π. Strength is normally correlated with Young's modulus (E) though many different mechanical characteristics are important including hardness, toughness, and abrasion resistance.

Measurement techniques for Young's modulus, E, are generally of three types: (i) bending methods [70–72], (ii) indentation methods [73, 74], and (iii) acoustic methods [75–77]. Ashkin *et al*. [75] measured E as a function of Π for monolithic (bulk) aerogels from wave velocity experiments using ultrasonic transducers. Adachi and Sakka [76] measured E as a function of heating temperature and Π using resonance tests performed on monoliths. Woignier *et al*. [70] determined the influence of Π on rupture strength and E of bulk aerogels using three-point bending tests. All showed a power law dependence of E on density that follows $E \propto \rho^{3.7 \pm 0.3}$. Moner–Girona *et al*. [73] measured E and hardness (H) of highly porous bulk gels by micro-indentation. They also observed power law variation with exponent close to 3.

Data on the mechanical properties of porous films and their variation with Π are scarce because complex instrumentation is needed to accurately measure the properties of thin films and because of the scarcity of films of varying Π with controllable and sufficient thickness. In nanoindentation the typical indentation depths needed to obtain accurate data on porous films are, ~50–100 nm depending upon the sensitivity. E and H can be measured without interference from the substrate provided the indentation depths are only 1/10th of film's thickness. Hence, a process to make thicker xerogel films (preferably $> 1\,\mu$m) is required. Fabes and Oliver [74] characterized H and E of dense silica gel coatings (thickness 66–184 nm) on sapphire using a nanoindenter but obtained ambiguous properties. Chiang *et al*. [78] measured the hardness and elastic modulus of various low dielectric constant films using nanoindentation. They report that Parylene has hardness of 0.3 GPa and aerogel between 0.01 and 0.06 GPa. Chow *et al*. [71] measured the biaxial modulus of a dense hybrid (but only 5% of methyltriethoxysilane used) xerogel film using the Flexus stress measurement tool by measuring stress on two different substrates. However, the porosity/density was not reported. Flannery *et al*. [77] have characterized ρ, Π, and E values of xerogel films via dispersion of laser-generated, wide-band, surface acoustic waves. They have observed power law variation of E with ρ but their data are scattered and limited in the range of $\rho(\Pi = 60\text{–}70\%)$. Recent surface acoustic wave results [79] suggest a linear dependence of modulus on density for mesoporous MSQ films. A list of modulus data for a variety of low-κ films is given in Table 9.4.

9.4.1 Models for generic porous materials

There have been three main types of modeling approaches used to describe porous materials: *cellular models* (for foam type solids); *minimum solid area models* for porous materials with defined shape pores; and the *finite element models*.

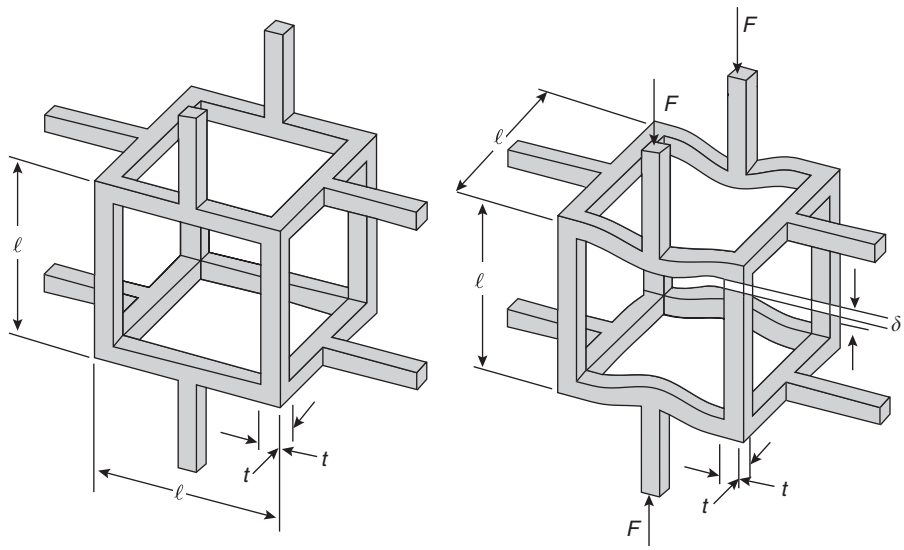

Fig. 9.11 Unit cell for an open-cell foam of cubic symmetry [80] (reprinted with permission).

9.4.1.1 Cellular models [80]

The materials are pictured as being made up of thin walls forming the surfaces of a hollow cell such as in a foam. Figure 9.11 shows the unit cell for an open-cell cubic foam (e.g. xerogels). The cells are staggered so that the corners of one cell rest upon the midpoint of adjacent cells. Such a structure neither corresponds to the actual geometric characteristics of a real foam nor can it be reproduced to fill space. This 'unit cell' does, however, capture the critical physical processes that govern the deformation and structural stability of cellular solids. The cell-shapes in real foams are more complex but if they deform and fail by the same mechanism, their properties can be understood by dimensional arguments that omit all constants arising from a specific cell geometry [80]. Young's modulus of a cellular material, relative to a bulk material is:

$$E/E_s = C(\rho/\rho_s)^2 \tag{4}$$

where ρ/ρ_s is the relative density, C is constant. Since a foam is not composed of a completely uniform cell geometry and size, it is more appropriate to determine the value of C by fitting it to data, instead of solving it analytically. Gibson and Ashby [80] fit Eq. (4) to the modulus measurements of a variety of materials and found $C \approx 1$.

In the above analysis, the predominant mechanism of deformation considered is bending, which gives a square dependence of the modulus with density. When the primary deformation is by axial extension, a linear dependence is predicted. Equation (4) describes the density dependence of the elastic modulus of an open-cell foam only at small displacements. The power-law exponent can be less than 2 for the case of closed-cell foams (Fig. 9.12). In a closed-cell

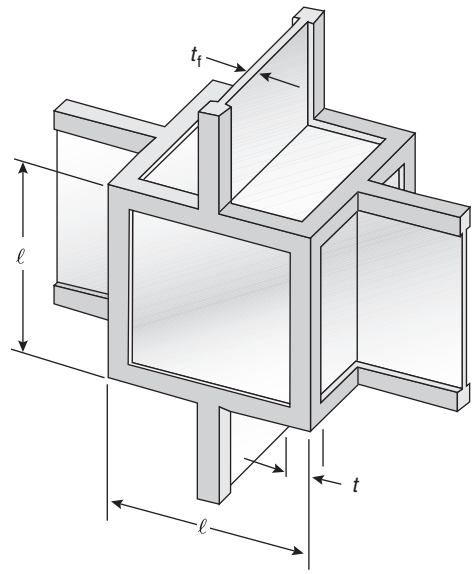

Fig. 9.12 Unit cell structure of a closed cell foam material [80] (reprinted with permission).

foam, some fraction of the material resides in the cell walls or faces rather than in the struts. If the fraction of material contained in the cell struts having thickness t is ϕ, then the fraction contained in the cell walls of thickness t_f is $(1-\phi)$. The stiffness of a closed-cell foam results then from three contributions: the first component is strut bending, as for open-cell foams. The second component is membrane (cell face) stretching that arises as the result of strut flexure causing the cell walls to deform. The final component is the internal gas pressure of the closed cells. The exact derivation of the modulus variation with density is too complicated to be given here. The final result is

$$E/E_s \approx \phi^2(\rho/\rho_s)^2 + (1-\phi)(\rho/\rho_s) \tag{5}$$

Here the contribution of the internal gas pressure is neglected, which is negligible for small gas pressures. Equation (5) yields a power-law relationship, which can describe the functional dependence of the modulus on density with an exponent of 1.6. At any given density the closed-cell foam would have higher modulus than the open-cell counterpart.

9.4.1.2 Minimum solid area (MSA) models [81–83]

In this approach, purely geometrical reasoning is used to predict the elastic moduli based on the weakest points within the structure. The minimum solid area represents that fraction of two-dimensional space occupied contiguously by solid in a packed particle or packed pore array (Fig. 9.13). This model assumes that the different properties have the same dependence on

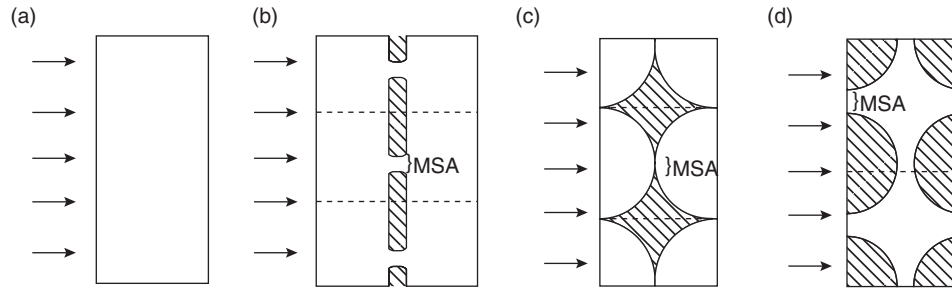

Fig. 9.13 Concept of minimum solid area. (a) shows a uniform body on which uniform stress is impinging. (b) Shows a body with isolated pores (hatched), MSA is the major factor controlling the transmittal of stress. (c) and (d) show, respectively, the idealized bodies, respectively, of bonded uniform spherical particles or an idealized foam [81] (reprinted with permission).

porosity. For the porosity range 0 to 1/3–1/2Π_c, the variation of the MSA (or property) with porosity can be described by Eq. (6):

$$S/S_0 = \exp(-b\Pi) \quad 0 \leqslant \Pi \leqslant 1/3 \text{ to } \Pi_c/2 \tag{6}$$

where S (e.g. modulus, toughness, or thermal conductivity) is the property of the porous material and S_0 is the corresponding property for the dense material. The MSA falls dramatically when the volume fraction of porosity reaches the critical value of porosity Π_c, which corresponds to the percolation limit of the solid phase and is characteristic of the porous material (see Fig. 9.14).

MSA models are empirical fits and cannot represent the entire porosity range with a single type of stacking geometry. The transition from one kind of packing to other is not well defined and so the phase inversion cannot be accounted for directly. The 0% porosity (dense) property must be known accurately. The axial extension is the only form of deformation mechanism, which is not justified as Wang [84] has shown that bending and shear effects are also important and tend to reduce the modulus in these materials.

Mizusaki *et al.* [85] proposed a model similar to MSA models to describe the variation in properties with densification during sintering of an as-pressed, porous ceramic. The gradual thickening of the neck area between neighboring particles for a three-dimensional cubic array of equivalent spheres was calculated by approximating the neck area by two sine-wave functions and the elastic–mechanical properties were determined using the minimum solid area of contact at the neck between the particles along the direction of the externally applied stress. The results were qualitatively similar to those in Fig. 9.14.

9.4.1.3 Finite element models [86–88]

These involve solving the equations of elasticity, numerically, for digital models of microstructure. Garboczi and Day [86], Roberts and Garboczi [87], and Garboczi [88] employ three different microstructural models that broadly cover the types of morphology observed in porous materials.

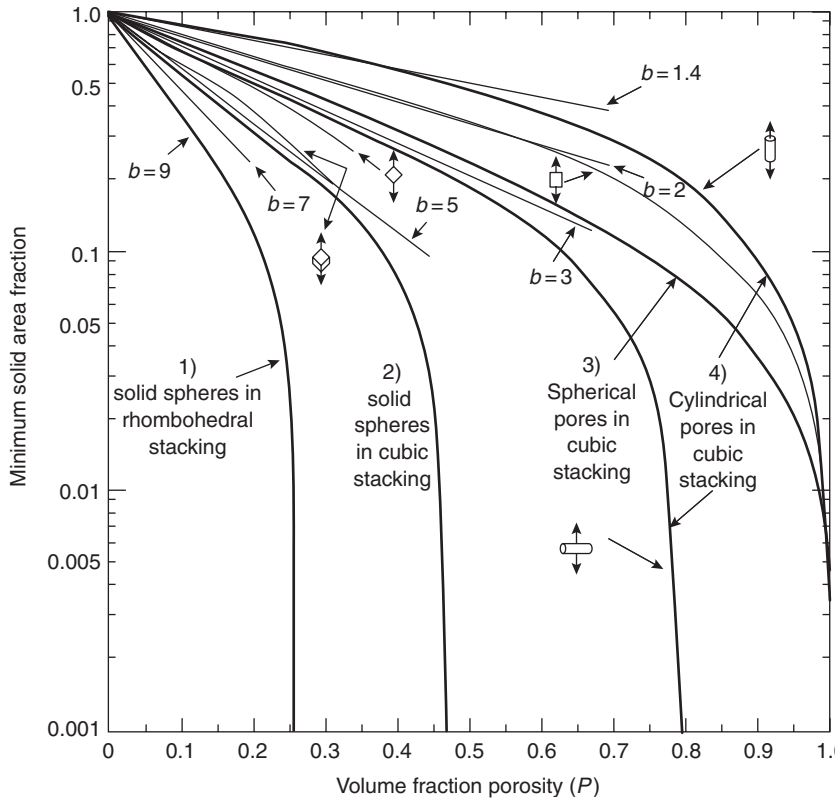

Fig. 9.14 Variation of the minimum solid area with porosity for idealized pores cubic stacking, Rice [82] (reprinted with permission).

The models are based on randomly placed spherical pores, solid spheres, and ellipsoidal pores (See Fig. 9.15). The centers of the pores or solid particles are uncorrelated, which leads to realistic microstructures in which both the pore and solid phases are interconnected. The results, which can be expressed simply by two (or sometimes three) parameter relations, correspond to a particular microstructure and explicitly show how the properties depend on the nature of the porosity. The results of their calculations are similar to those presented in Fig. 9.14 but show that for a given porosity, a material that has spherical pores has better properties than the one with ellipsoidal pores.

9.4.1.4 Percolation theory [89]

Percolation theory can be used to describe the flow of fluid, mass, heat, charge, force, etc., through a random medium (percolation cluster). Simple percolation theory predicts a power-law functional form:

$$E \propto (P - P_c)^{\tau} \tag{7}$$

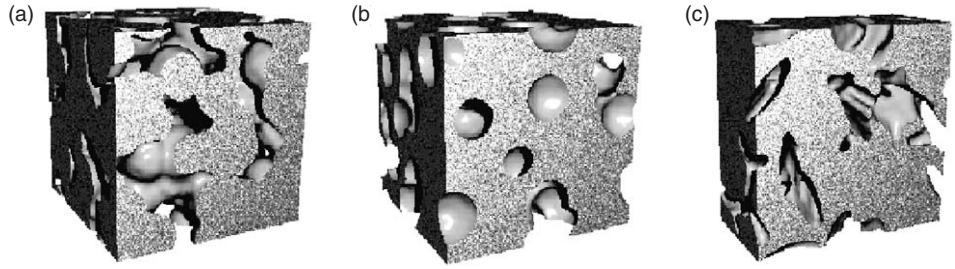

Fig. 9.15 Pieces of the various models studied by Roberts and Garboczi *et al*. [87]: (a) overlapping solid spheres; (b) overlapping spherical pores; and (c) overlapping ellipsoidal pores (reprinted with permission).

where P is the probability for a site to be occupied (or a bond to be created), P_c is the percolation threshold (defined as the magnitude of P above which an infinite cluster exists), and τ is a critical exponent that is characteristic of the physical property (e.g. elastic modulus). The choice of a physical variable that can replace the unknown mathematical variable P_c is difficult. In the straightforward gelation/percolation analogy, the gel fraction (and thus the density) is associated with the percolation probability (the probability for a site to belong to the infinite cluster) and scales with an exponent, β. Therefore, $E \propto \rho^{\tau/\beta}$ or $E \propto \rho^m$. The exponent m has been found from literature and computer simulation to be ~9 and is largely overestimated. Experiments have shown the exponent to be much less, between 3.2 and 3.6 for high-porosity aerogel materials [70].

9.4.1.5 Fractal structure models [70]

There were some arguments in the literature that the exponent m could be related to the fractal dimension D_f of xerogel. The proposed relation is

$$m = (5 - D_f)/(3 - D_f) \tag{8}$$

However, Woignier *et al*. [70] showed that modulus of three kinds of aerogels made with acid, base, and neutral catalyst conditions (which have different fractal dimension D_f of a xerogel) are the same for a large density range. Also the fractal dimension of a sintered gel approaches 3 but experimentally they observed a decrease in the exponent, m, with sintering. Thus, the fractal approach is also incorrect in describing the behavior of the modulus over a wide range of density.

9.4.1.6 Computer simulations [90]

Recently, Ma *et al*. [90] generated computer models of aerogels of low densities (0.026–0.18 g/cm^3) by diffusion-limited cluster–cluster aggregation (DLCA) algorithms and their elastic properties were evaluated by a FEM, assuming that the stiffness of each interparticle bond can be represented by a beam element. The simulation yields $m \approx 3.6$ for perfectly connected

structures, contradicting the consensus that the dangling mass on the gel gives rise to a high exponent. The high exponent is largely due to the reduction in the connectivity of the material with decreasing density.

9.4.2 Modulus measurements

The thin film modulus and hardness are often measured by nanoindentation [91] but other techniques exist including beam bending, surface acoustic wave, and Brillouin scattering. Discrepancies between the techniques are common [92] and published data over a full range of porosity is rare. The results for elastic modulus (from nanoindentation, after correction for Poisson's ratio) of silica xerogel material from Jain *et al*. [22] are shown in Fig. 9.16. They are plotted as a function of density, $\rho = \rho_s\ (1 - \Pi)$ where ρ_s is the density of the solid material. $\rho_s = 2.15\,\text{g/cm}^3$ for cases (a) and (b) where a single or dual solvent approach was used, and $\rho_s = 2.2\,\text{g/cm}^3$ for case (c) where the film was sintered.

The solid lines in Fig. 9.16 are power law fits to the data. The power-law fits suggest that over the porosity range studied (25–75%), the xerogel structure can be modeled as open-cell foams and bending of cell edges is the dominant form of deformation. The films made with a mixture of ethylene glycol (EG) and ethanol as the solvent have a higher E than the films made

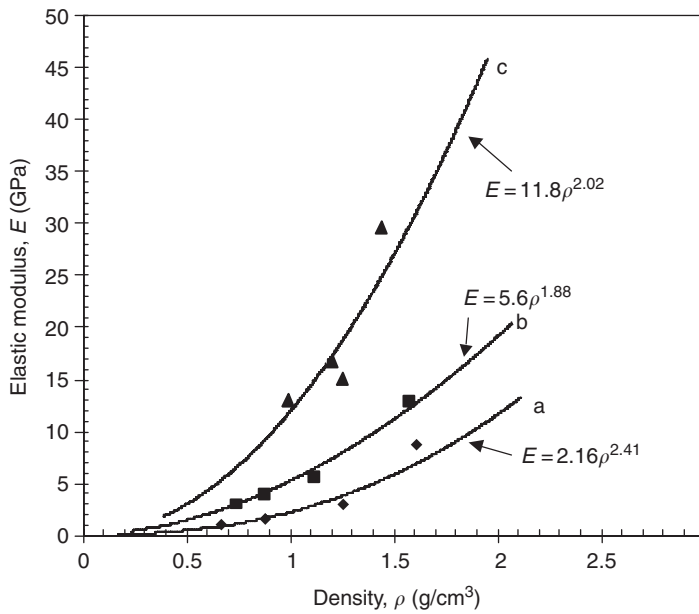

Fig. 9.16 Elastic modulus of films measured by nanoindentation; (a) films made with ethanol as the solvent; (b) films made with ethanol and ethylene glycol co-solvent mixture; (c) sintered films. Solid lines are power law fits [22] (reprinted with permission).

using only ethanol as the solvent. This behavior can be attributed to a narrower pore size distribution obtained using EG, a phenomenon first observed for bulk gels [93, 94]. Sintered xerogel films show the highest modulus with a power-law exponent close to 2. The data also suggest that for films of higher densities the connectivity between particles, a major determinant of mechanical properties, remains unchanged. In the process used to make these films, the connectivity is established by aging the films in a solution under conditions of high silica solubility [36] to insure dissolution and reprecipitation of silica and hence, the growth of connecting neck regions between particles. Exponents greater than 3 were observed before [70, 73, 79] for high porosity gels. These higher values may result from inadequate aging and insufficient neck formation.

If a large fraction of the solid material is non-load bearing at low density, as it transitions to load bearing at higher densities, the dependence of modulus on density should increase and lead to exponents higher than 2. For films made with EG, the exponent of 1.88 suggests that some closed pores might be present but the exponent is too close to 2 to tell conclusively. The constant of proportionality, C, assuming the open cell foam model [Eq. (4)] is ~0.35 for the glycol films. Fitting the data to Eq. (5), a value of $C = 0.38$ and $\phi = 0.98$ was obtained for EG formed films, which suggests that 2% of material is contained in cell walls. For films made with ethanol, C in Eq. (4) = 0.22. The low values of C and a slightly higher value of the exponent for ethanol-based films (2.4) [60] are due to the random structure (presence of a broad pore size distribution) and the presence of flaws in the solid matrix of xerogel. The spherical particles making up the matrix are also not completely fused together. As shown in Fig. 9.16, sintering is an effective way to improve E and the constant, $C = 0.97$, for the sintered films. The morphology of the sintered xerogel closely approaches that of a cellular solid with rectangular struts, as the spherical particles in the matrix fuse together to form a beam-like morphology of fused silica (glass) [95].

A number of investigators have reported on the measurement of E for several silica based, hybrid and polymeric materials, which are in contention as low-κ materials. Figure 9.17 shows the reported E values for a variety of these low-κ materials compared with data for xerogel films processed in three different ways. The relationship between the optical properties (refractive index which is related to Π) and mechanical properties (E) is direct for xerogels but not for polymeric materials. Since we have measured values of κ for xerogels [36] and κ data for low-κ polymers are readily available (while density is not), Fig. 9.17 uses κ for comparisons. The important points to note from this graph are: (i) the modulus of porous silica is the highest in the group and E of sintered xerogel extrapolated to $\Pi = 0$ approaches that of dense oxides (CVD or thermal), (ii) the modulus of sintered xerogels, templated silica ($\kappa = 2.4, \Pi = 55\%$) [32] and Vycor glass [96] obey the same power-law relationship. This supports the hypothesis that all these materials have continuous solid matrices. Bone, another material with a continuous solid matrix also obeys a power-law relationship with an exponent of nearly 2 [97, 98]. (iii) E of our xerogel films made with EG at the same κ is comparable to E of methyl-silsesquioxane (MSQ) and bridged hybrid silsesquioxane materials [79, 99, 99a]. (iv) E of our xerogel films made with ethanol

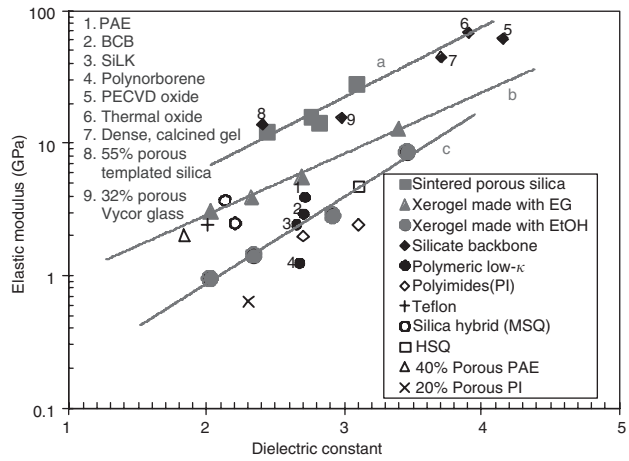

Fig. 9.17 Elastic modulus of various low-κ materials. Solid lines are exponential best fits for xerogel films made with (curve b) and without ethylene glycol (curve c) and sintered films (curve a) [22] (reprinted with permission).

is similar to hydrogen silsesquioxane (HSQ) [100]. HSQ also has a random structure made of cages and ladders. (v) Moduli of dense polymeric low-κ materials such as benzocyclobutene (BCB), SiLK, polyarylene ether (PAE), and polynorbornene are scattered and depend on the crosslink density, the free volume of the polymer, etc. (vi) One set of data on porous PAE [101] gives the ratio of E of 40% porous to dense film as 0.51, which according to Eq. (4) gives $C = 1.31$. With $C = 1$, the exponent is 1.35 and $\phi = 0.167$, suggesting the presence of closed pores. Thus, Fig. 9.17 shows clearly that porous silica films (either sintered or templated) have a higher elastic modulus than any other amorphous low-κ materials. Sintered xerogel materials can thus be used as model materials for describing the mechanical behavior of other low-κ materials.

To conclude, the moduli of amorphous porous dielectric materials depend on the process history and the properties of the solid phase. The dependence on process history is probably true for all materials exhibiting glass transition.

9.4.3 Fracture toughness

Maintaining the mechanical integrity of multilayer coatings in case of adhesion failure is an important requirement for successful integration in back-end-of-the-line (BEOL) processing. The materials must possess both cohesive and adhesive fracture toughness. The modified-edge lift off (m-ELT) test [112–114] can be used to quantify the adhesion of multilayer coatings in case of failure governed by adhesion failure. For cohesive failure, a measure of the material's cohesive toughness is obtained.

Table 9.4 Modulus mesurements for low-κ materials

Low-κ dielectric	Dielectric constant	Modulus (GPa)	Measurement technique used	Source
Plasma deposited oxide	4.1–4.2	59	Biaxial modulus ($E/1-\nu$) Bending beam (BB) method	[100]
		64 ± 2	($\nu = 0.24$) Brillouin light scattering ($\nu = 0.25$)	[101]
Thermal oxide	3.9	72	BB ($\nu = 0.20$)	[102]
Dense hybrid xerogel	3.7	44.8	BB ($\nu = 0.20$)	[58]
Hydrogen silsesquioxane (HSQ)	3–3.2	4.74	BB ($\nu = 0.33$)	[100]
59% Porous HSQ	2.2 ± 0.1	2.5	Nanoindentation	[103]
56% Mesoporous hybrid silsesquioxane (25%) (MHS)	2.15	3.5	Nanoindentation	[99]
53% Porous MHS (50%)	2.13	3.7	Nanoindentation	[99]
56% Porous MHS (75%)	1.98	4.3	Nanoindentation	[99]
55% Porous templated silica	2.4	14 ± 1	Nanoindentation	[32]
Methylsilsesquioxane	2.9	1.65	Surface acoustic wave	[79]
	2.35	1.53		
	2.2	1.34		
	2.15	1.02		
	1.9	0.76		
Dense poly-arylene ether (PAE)	2.71 ± 0.05	3.96 ± 0.45	Membrane bulge test ($\nu = 0.42$)	[104, 105]
		3.91 ± 0.41	Nanoindentation	
40% Porous PAE	1.83 ± 0.05	2.04 ± 0.41	Membrane bulge test ($\nu = 0.42$)	[105]
		3.91 ± 0.41	Nanoindentation	
SiLK	2.65	2.45 ± 0.04	Nanoindentation	[18]
BCB	2.7	2.9 ± 0.2	Tensile testing	[106]
		3.06 ± 0.38	Dual Capacitor technique	[107]
Polynorbornene	2.67	1.3 ± 0.7	Dynamic mechanical analyzer (DMA)	[108]
		1.15–1.4	BB ($\nu = 0.35$)	
Polyimide (PI)	2.7	2.0	Tensile testing	[109]
BPDA-PDA PI	3.1	6.66 (out of plane)	BB ($\nu = 0.4$)	[100]
BPDA-PDA PI	3.1	2.45 ± 0.64 (average)	Dual Capacitor technique	[107]
20% Porous fluorinated PI	2.3	0.636	DMA	[110]
Teflon	2.0	2.45	Nanoindentation	[111]

The dielectric and the substrate materials have different coefficient of thermal expansion. This thermal mismatch generates residual stresses after thermal processing. In the simplest case, the residual stress field is characterized by the in-plane stress that develops due to thermal expansion mismatches with the substrate. This residual stress, σ_0, for linear-elastic materials is given by

$$\sigma_0 = \frac{E\Delta\alpha\Delta T}{(1-n)} \tag{9}$$

where E is the coating's Young modulus, ν is its Poisson ratio, $\Delta\alpha$ is the difference in the coefficient of thermal expansion with the substrate and ΔT is the difference between the temperature and the zero-stress temperature. The value of G has been determined analytically for many crack geometries related to microelectronic devices [115]. In general, for biaxially stressed, thin-film coatings, G is described by

$$G = \phi\frac{\sigma_0^2 h}{E'} \tag{10}$$

where h is the film thickness, E' is the plane-stress modulus, $E/(1-\nu^2)$; and ϕ is a geometry prefactor. The value of ϕ for the case of an interfacial crack in a very thin film is 0.5.

Figure 9.18 shows the fracture toughness of xerogel films aged for different times at 60°C from Jain [61]. The toughness first increases with increasing aging time, reaches a maximum, and then decreases for long aging times (24 h). The film aged for 17 h shows the maximum fracture toughness. These observations are in agreement with the results of some other researchers on bulk aerogel materials. Haereid *et al.* [116] observed a decrease in the modulus of rupture of the wet bulk gels aged in water for long times at 70–100°C. The modulus of rupture is determined using a three-point bending test and basically measures the tensile strength of a brittle material.

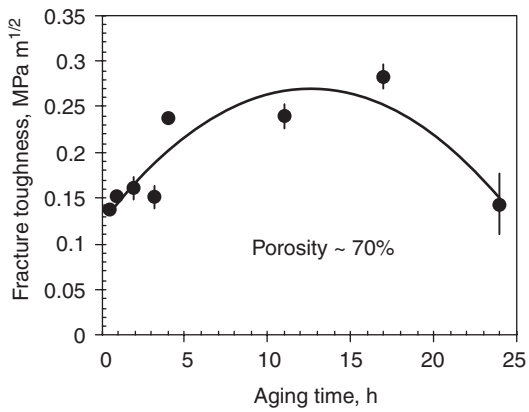

Fig. 9.18 Fracture toughness of xerogel films as a function of aging time [61] (reprinted with permission).

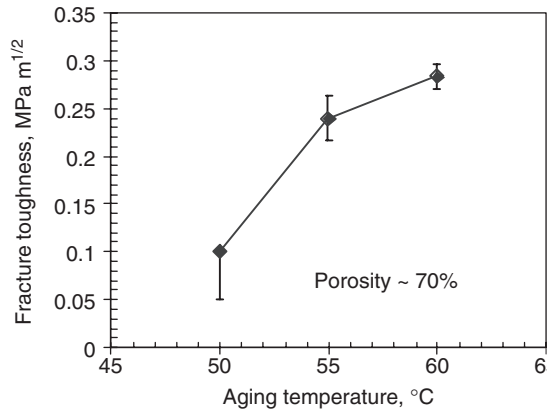

Fig. 9.19 Fracture toughness of xerogel films as a function of aging temperature [61] (reprinted with permission).

The edge lift-off test gives equivalent information for a thin film. Figure 9.19 shows the fracture toughness versus aging temperature of the films. The results show that the toughness increases almost three times with an increase in the aging temperature by just 10°C. Thus, the higher the aging temperature the higher the film's strength. This observation is in agreement with Smith *et al.*'s findings [117] that at temperatures in the range 100–150°C the aging time required to achieve significant mechanical strength is of the order of few minutes. However, high temperature aging conditions can only be achieved in super-saturated ambient (in pressurized vessels).

The results from Figs. 9.18 and 9.19 suggest that the optimum aging conditions for the experiments done are the aging temperature of 60°C and the aging time of 15 h. However, as shown by Smith *et al.* [117], aging at higher temperatures can significantly reduce the required aging time. The locus of failure for the xerogel samples testing in Figs. 9.18 and 9.19 was the silicon–xerogel interface, which means that the measured fracture toughness could be the adhesive fracture toughness, rather than the cohesive fracture toughness [61]. Since the mechanical properties depend nonlinearly on the porosity of the xerogels [118], fracture toughness measurements must be made as a function of porosity. For this purpose, the toughness of the films made with the binary ethylene glycol/ethanol solvent method was measured. As with modulus, fracture toughness is also process history dependent. Three different xerogel films (~53%, 63%, and 72% porous) aged for different times (7, 15, 20 h) at 60°C and made using the binary solvent approach were used for fracture toughness measurements. The results are shown in Fig. 9.20 [61]. The toughness values are much higher than those obtained with xerogels made using the single solvent (ethanol) method. Adhesion can be improved by using adhesion promoters and so, for these films, γ-aminopropyltriethoxysilane was used in an attempt to insure the observation of cohesive failure. The use of the adhesion promoter does improve the adhesion and it was observed that the 63 and 72% porous films failed cohesively during testing.

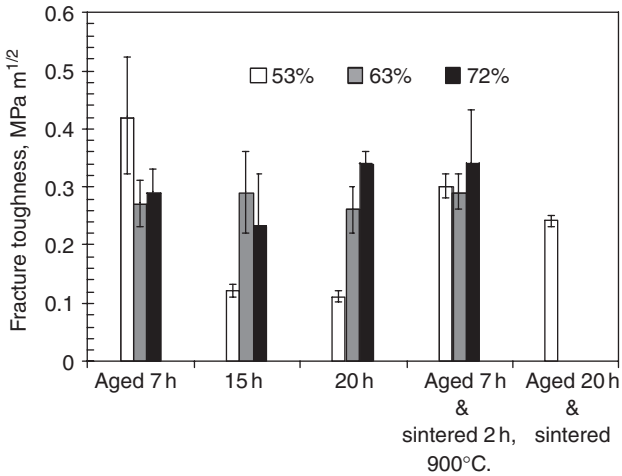

Fig. 9.20 Fracture toughness for xerogel films as a function of process history [61] (reprinted with permission).

Also, it is seen in Figure 9.20 that aging time does not have much influence on the toughness of the 63 and 72% porous films, though a decrease in the toughness is seen with the aging time for the 53% porous films. This suggests that the behavior of the films processed with lower amounts of ethylene glycol (higher-density films) is similar to the film made with only ethanol as the solvent. Sintering these films did not improve toughness as compared to the as-prepared films and adhesive failures were also seen. This may be related to the delinking of the bonds formed between the adhesion promoter and the xerogel coating at the high sintering temperature. In addition, all the organic components in the films are burnt off during sintering allowing for more moisture absorption and moisture-related defects. Thus, even though the sintered films have reduced defects and ordered and connected structure, their toughness does not increase after sintering most likely due to increased moisture absorption and an increase in moisture-related defects.

Im *et al.* [119] measured toughness (and fracture energy) of photosensitive benzocyclobutene (BCB) on various substrates such as Al, Cu, Si, SiN. Shaffer *et al.* [120] have measured the toughness of dense and porous SiLK (a Dow Chemical specialty polymer resin) and silicate materials that include high and low dielectric constant organosilicate (OSG) made by CVD and HSQ. These data have been plotted in Fig. 9.21 by Jain [61] as a function of the dielectric constant along with the highest fracture toughness of the films processed using the binary solvent method. Cohesive failures were achieved for both BCB and SiLK films. However, the adhesion of BCB and SiLK to silicon is well controlled by using adhesion promoters. The highest fracture toughness values for the xerogel films made using the ethylene glycol/ethanol binary solvent are comparable to SiLK at the same value of dielectric constant. Thus, by controlling the chemistry and processing, low-κ materials with both high modulus and toughness can be

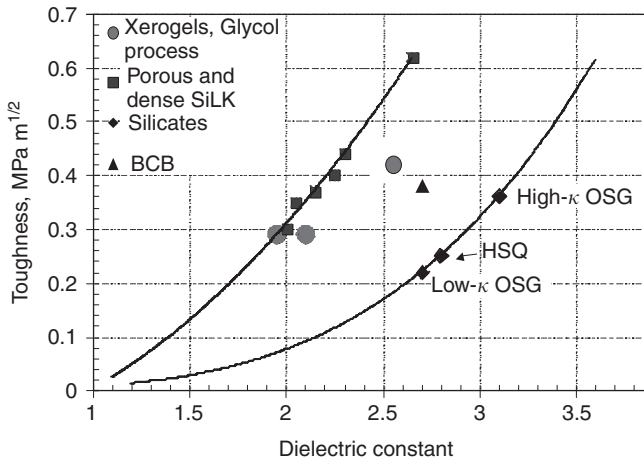

Fig. 9.21 Fracture toughness of various low-κ dielectric films measured by modified edge-lift-off test [61] (reprinted with permission).

obtained. Another point to notice is that for the same dielectric constant dense organosilicates and silsesquioxanes have lower toughness values than both the porous SiLK and porous xerogels made by the binary solvent process. This can again be ascribed to the crack deflection and crack bridging mechanisms caused by the presence of pores. Similar effects are used to increase the toughness of the polymer blends where one of the components is the crack-deflecting polymer.

9.5 Thermal conductivity of nanoporous dielectric films

Introducing porosity into a material necessarily lowers its thermal conductivity. The increased density of transistors per chip causes more Joule heating [121] and though metals are efficient conductors of heat, the major resistance to heat transfer resides in the interlayer dielectric. Metal lines and vias, as currently used, are not sufficient, nor designed, for heat removal from chips [122]. Thus, a lower conductivity in the dielectric may lead to heat dissipation problems. The low conductivity of dielectrics is also a problem in chemical mechanical planarization (CMP) processes as frictional heating during CMP may give rise to hot spots resulting in localized stress and cap delamination [123]. Small decreases in the thermal conductivity of dielectrics can cause sudden increases in the interconnect temperature [124]. Thus, efficient thermal design of integrated circuits is required and it is essential to understand the heat transport phenomena in thin dielectric films. Goodson and Ju [125], Cahill [126], and Goodson *et al.* [127] have given excellent reviews on this subject. In this section, we present information on the thermal conductivity of porous materials and the relationship between thermal conductivity and elastic modulus. We also compare the thermal conductivity of porous silica xerogel films processed in

different ways with other low-κ (polymeric and silsesquioxanes) dielectrics. The differences are explained qualitatively by disorder in the films that affects phonon transport and scattering.

9.5.1 Thermal transport processes in dielectric films

The total thermal conductivity λ_t of a porous material can be represented as the sum of contributions from several parts: conduction through the solid, λ_s, conduction through the gas, λ_g, and radiation through the particles and voids, λ_r [128, 129]. For integrated circuits, radiation is not an issue and conduction through the gas in the pores is also negligible. Thus, we are concerned primarily with conduction through the solid matrix:

$$\lambda_t = \lambda_s + \lambda_g + \lambda_r \tag{11}$$

The conduction of heat in disordered dielectric solids may be considered as the propagation of anharmonic elastic waves through a continuum. The propagation occurs via interaction between the quanta of thermal energy, or phonons. The frequency (ω) of lattice waves with velocity (v) covers a wide range and the thermal conductivity (k), in general form, can be written in terms of a superposition of these waves:

$$k = \frac{1}{3}\int \rho C_p(\omega) v \ell(\omega)\, \mathrm{d}\omega \tag{12}$$

where $C_p(\omega)$ is the contribution to the specific heat per frequency interval for lattice waves of that frequency and $\ell(\omega)$ is the attenuation length or the mean free path for the lattice waves. At temperatures above 50 K, heat transfer through disordered dielectric films can be considered to be a diffusion process. The phonon mean free paths are very short (approx. few Å) and the temperature (T) dependent thermal diffusivity (α) can be written as:

$$\alpha(T) = k(T)/(\rho C_p) = (1/3) v \ell(T) \tag{13}$$

where the macroscopic density, ρ, specific heat, C_p, of the material, the transport velocity, v, of the lattice waves (or phonons) and the phonon mean free path, ℓ, are the factors that determine the thermal conductivity. For dielectric films, the temperature dependence is very weak for ρ, C_p, and v, and so the mean free path is the main factor that affects the conductivity. If ℓ is equal to the separation distance between constituent atoms, the resulting conductivity is referred to as the *minimum thermal conductivity* [126]. Conductivities in excess of the minimum arise from additional mechanisms for transport through the solid. For amorphous disordered solids like glasses, the mean free path is almost constant at room temperature [130] and is limited to several interatomic spacings. The mean free path of fused silica at room temperature is 5.6 Å [131], which is about the size of an elementary silicate ring in the disordered structure of glass [132]. The maximum wavelength of a phonon that could exist in a thin film dielectric is equal to the film's thickness.

There are two regimes of heat transport governed by lattice vibrations. At low vibrational energies the lattice vibrations are wave-like, and phonons exist with well defined wavelengths (λ), wave vectors ($\mathbf{k}$) $= 2\pi/\lambda$ and velocities (ν). In this regime, the kinetic theory equation, similar to Eq. (12) is applicable:

$$k(\omega) = \rho C_p(\omega)\nu\ell(\omega)/3 \tag{14}$$

This provides the minimum thermal conductivity. If τ_i is the average time between the collisions of the phonons with the imperfections in the material, then:

$$\tau_i = \frac{1}{\beta\sigma\rho_d\nu} \tag{15}$$

where σ is the scattering cross section, β is a constant on the order of unity, ρ_d is the defect density per unit volume, and ν is the velocity of lattice waves (phonons). A shorter τ_i implies a shorter ℓ and, hence, a lower thermal conductivity. As the vibrational energy of the lattice waves increases, the scattering cross-section (σ), which is inversely proportional to ℓ and depends on the size of imperfections, approaches zero [133], and Rayleigh scattering occurs. Rayleigh scattering increases as ω^4 until $\ell^{-1} \approx \mathbf{k}/\pi(2/\lambda)$.

The phonon mean free path is affected by a number of factors. The dominant factor in most solids is inelastic phonon–phonon scattering (Umklapp processes). Such scattering is absent in amorphous materials with no long-range order such as silica glass. However, various other factors cause anharmonicities and scattering. These factors include interactions between phonons and any defects or imperfections in the films such as interfaces, microvoids, microcracks, particles, pores etc. [127–129]. This factor is also evident from Eq. (15), where increasing the defect density, ρ_d, decreases τ_i and hence ℓ. The presence of different size atoms and impurities leads to increased phonon scattering. The increased scattering is due to differences in the mass of the elements, differences in the binding force of the substituted atom, and the elastic strain field around the substituted atom. Thus, organic–inorganic silica hybrid dielectric materials (silsesquioxanes) are expected to have lower conductivities than pure silica films. Polymeric low-κ materials with their inherently low density and specific heat have inherently lower thermal conductivity than inorganic materials. The thermal conductivity of organic films also depends on additional factors such as the degree of orientation of crystalline regions and of molecular strands in the amorphous regions [127]. We expect nanoporous silica to have a higher thermal conductivity than other low-κ dielectrics in the same way that dense silica has a higher thermal conductivity than dense hybrid or organic materials.

The effective mean free path is found by adding the contribution of each of the above effects as a sum of resistances in parallel (i.e. adding $1/\ell$ for each mechanism). Thus, the more factors that cause anharmonicities, or the more disorder in the films, the shorter the effective mean free path and the lower the conductivity of the material. At sufficiently high temperatures, generally above room temperature, scattering due to imperfections is independent of the

temperature and frequency. If imperfections are reduced or eliminated, the thermal conductivity will increase. Although it is difficult to determine accurately the mean free path for an amorphous dielectric (with or without porosity) material, the concept is very useful in explaining the results we have obtained with porous silica or hybrid films.

The disorder in a film and hence its thermal conductivity can be radically altered by changes in process conditions. This is particularly important for disordered materials with a glass transition temperature. In porous materials with a broad pore size distribution like xerogels, the dominant phonon scattering mechanism would be from the pores of smallest sizes and the maximum phonon wavelength would be limited to the largest pore size. If these long wavelength phonons dominate the transport of heat, then effective medium theories should yield good estimates of the thermal conductivity. A material with uniformly sized 10-nm spherical pores such as porous Vycor glass (porosity ~ 30%) is found to have a thermal conductivity [134] predicted by the effective medium theory given by Landauer [135]. This suggests that the maximum wavelength of phonons is limited to the pore size, ~ 10 nm, and that those long-wavelength phonons are transporting most of the heat.

Beyond fundamental phonon-based theories of thermal conduction in solids, there are various geometry-based models available in the literature to predict and correlate the thermal conductivity of porous media [136–140]. These models are solely based on the geometrical packing arrangement of particles or pores similar to the MSA models proposed by Rice [81] or the models proposed by Mizusaki *et al*. [85] for mechanical properties. Thus, they are useful for correlation purposes, but offer little in terms of fundamental understanding. Since the microstructures of most porous materials are very complex, these geometrical models fail to adequately predict the thermal conductivity.

9.5.2 Thermal conductivity measurements

There have been various techniques reported to measure the thermal conductivity of thin dielectric films [127, 128, 141–143]. Two that appear to be finding the most widespread use are the 3ω and photothermal deflection techniques. The details of 3ω technique can be found in the literature [144–150]. The photothermal deflection technique is based on the periodic heating of a sample by a modulated laser pump beam. There are various configurations of this method [151–154]. The absorption of the pump laser beam caused a local-temperature rise, which, in turn, leads to a local surface deformation, the magnitude of which could be less than 0.1 nm. The surface deflection signal was detected by the probe beam and was related to the thermal conductivity of the sample. This detection method of thermal waves is called the photothermal deformation technique.

The measurements of both the 3ω and the photothermal method are frequency dependent. It is important that the frequency of measurement is such that the measured thermal conductivity is independent of the film thickness. This is ensured by choosing the thickness of the films

and the frequency in such a way that the thermal diffusion length $\sqrt{2\alpha/\omega}$ for the energy pulse is much greater than the film thickness, where α is the thermal diffusivity. This ensures that the dielectric does not store any thermal energy and that a one-dimensional quasi-steady state thermal heat conduction situation occurs.

Figure 9.22 shows the thermal conductivity measurements of the three different types of porous silica xerogel films by Jain *et al.* [21] plotted as a function of increasing density (or reducing porosity). The *as-prepared* films made with ethanol as the solvent have the lowest conductivity of the three types of films. This is because these films have a very broad pore size distribution (including microporosity), microcracks, impurities (unreacted ethoxy groups), defects, and hanging and loose ended silica chains, all of which contribute to significant phonon scattering and limit the mean free path. The thermal conductivity of these films varies with density as a power–law relationship with an exponent of 1.65. This is close to what has been reported for bulk aerogels (1.88) prepared by a similar process [155]. The mean free path of fused dense silica at room temperature is comparable to the size of the micropores present in the xerogel. Hence, phonon-scattering would be predominant compared to microporosity. For films made with the ethylene glycol/ethanol, binary solvent technique, the pore size distribution is narrower than for films made with the single solvent (ethanol) process [156]. This may explain their higher conductivity since the anharmonicities due to scattering from a broad pore size distribution are reduced in the binary solvent method. The power-law fit with an exponent of 1.0 is only valid for the density range for which the thermal conductivity data of these films are available.

The sintering process heals the microstructure, removes microcracks, microporosity [157], and residual organics, and causes the structure to become more uniform and beam-like [22]. Thus, phonon scattering is reduced and the thermal conductivity of sintered porous silica films

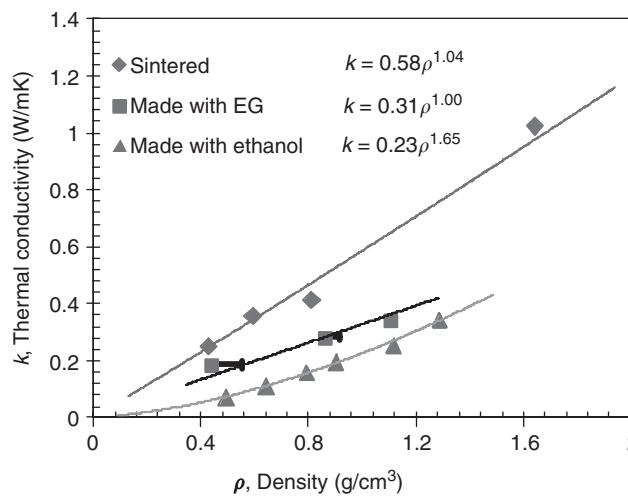

Fig. 9.22 Thermal conductivity of silica xerogel films as a function of density and process history [21] (reprinted with permission).

is the highest by far and essentially a linear function of the film density. Zeng *et al.* [140] formulated geometrical models for xerogels and found that for models where the microstructure consists of cylindrical or square cross-section rods, the thermal conductivity varies linearly with density. The linear dependence of the thermal conductivity for sintered films is consistent with Zeng *et al.*'s model.

Another way to compare process effects on the thermal conductivity of xerogel films is to plot the thermal conductivity as a function of dielectric constant. This is shown in Fig. 9.23. The dielectric constant was measured for all three different kinds of xerogel films. The thermal conductivity of the sintered porous xerogel films when extrapolated to the dielectric constant of pure silica (~4.0) has the value of ~1.35 W/(m K), which is close to that of thermally grown oxide films. On the other hand, the thermal conductivity of xerogel films made with single and binary solvent processes extrapolated to $k = 4.0$ is lower than that of sintered films but higher than 1.1 W/(m K), the thermal conductivity of PECVD oxide [125] films.

Figure 9.24 displays a comparison of the thermal conductivity for xerogel films with that of polymeric, hydrogen silsesquioxane (HSQ), and methylsilsesquioxane MSQ low-κ materials [158–160]. The thermal conductivity of porous and dense MSQ ($k_{\text{dense}} = 2.75$) and dense HSQ ($k = 3.1$) was measured by Lu *et al.* [161]. The thermal conductivity of the sintered porous xerogel film is much higher than other comparable low-κ materials. Figure 9.24 also shows that for a given dielectric constant, the inorganic xerogel materials have better thermal conductivity than dense SiLK™, BCB, or polyimide materials. Polymeric materials have inherently lower thermal conductivity due to the flexibility of their chains and the corresponding low speed of sound in the material. Crystalline polymeric materials have higher conductivities than amorphous materials. Making either of these classes of materials porous would only further reduce their

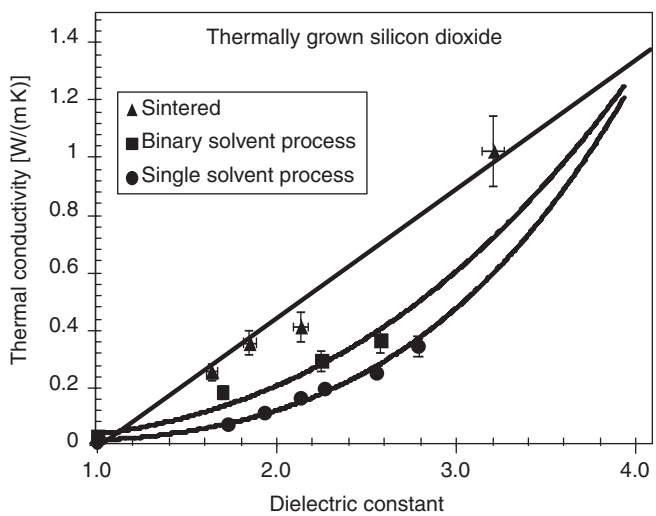

Fig. 9.23 Silica xerogel thermal conductivity as a function of dielectric constant [21] (reprinted with permission).

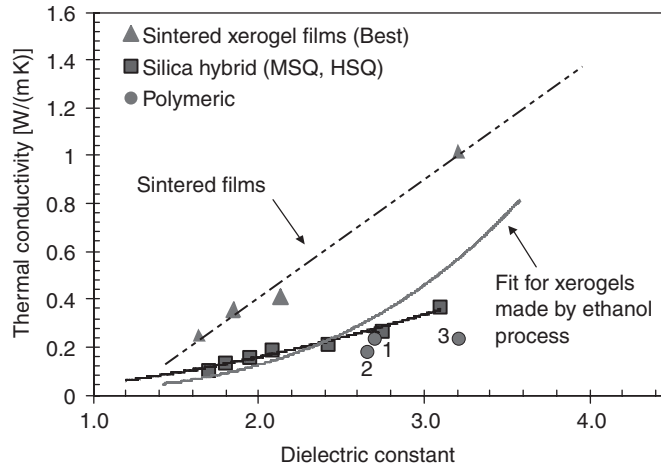

Fig. 9.24 A comparison of the thermal conductivity for low-κ materials [21] (reprinted with permission).

thermal conductivity. The hybrid organo-silicates (or silsesquioxanes) have conductivities comparable to xerogel films made using the single solvent (ethanol) method. In these hybrid materials, the presence of organic–inorganic chemical species interfaces contributes to additional phonon scattering and reduces their conductivity. As the ratio of organic to inorganic constituents increases, the thermal conductivity approaches that for polymeric materials.

For dense SiO_2 films, the measured thermal conductivity is also process dependent [125] and increases in the following order: evaporated, LPCVD, phosphosilicate glass (PSG, 7%), sputtered, PECVD, and thermal oxide. This sequence correlates with the increased temperature of deposition for the different kinds of silicate films. For films deposited by LPCVD or PECVD, a high-temperature anneal increases the thermal conductivity. There is also a progressive increase in the thermal conductivity with annealing temperature. This behavior is similar to the increased thermal conductivity of sintered xerogel films as compared to as-prepared xerogel films. Thus, the degree of disorder is reduced after high-temperature annealing and the thermal conductivity approaches those of thermally grown silicon dioxide films. Any material with a glass transition temperature would benefit from annealing.

9.5.3 Relationship between the properties of nanoporous dielectric films

The same processes used to improve the mechanical strength of porous materials should also improve the heat transfer characteristics of the films. If true, this provides a way to determine a relationship between the two for any given material.

We take, as an example, the data collected for silica xerogel materials by Jain *et al.* [21]. Using the relationships between the elastic modulus and density for xerogels and the results for

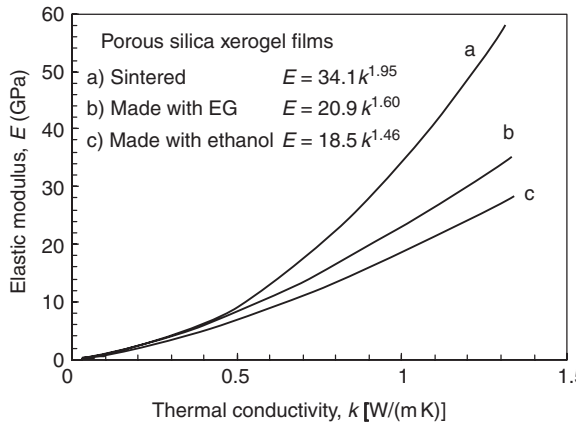

Fig. 9.25 Relationship between the thermal conductivity and elastic modulus for xerogel materials as a function of their processing history [21] (reprinted with permission).

thermal conductivity versus density for xerogels from Fig. 9.22, scaling relationships between the elastic modulus and thermal conductivity are plotted in Fig. 9.25. The sintered films show a scaling exponent of 1.95 for the variation of modulus (E) versus thermal conductivity. This value is close to that obtained by Lu *et al*. (1.8 ± 0.2), for bulk carbon aerogels [162] and Emmerling and Fricke (1.87 and 2.03) for bulk silica and carbon aerogels, respectively [163]. The higher value of the scaling exponent of the modulus variation with the density as compared to that for the thermal conductivity variation with density is explained on the basis of the higher tensorial order of the force transmission process as compared to the thermal conduction process [164]. This means that any factor that influences the modulus would affect all the elastic constants isotropically in all three directions and would affect both the elastic and shear modulus [165].

A fundamental analogy can be drawn between the force transmission problem and the heat or energy transmission problem. Heat transmission in dielectrics is governed by phonon scattering processes and similarly, force transmission is governed by the elastic (acoustic) wave scattering processes. The difference between the two lies in the wavelength of the transmitting waves. Elastic waves are long-wavelength acoustic waves and not scattered by small imperfections such as the pores of a nanoporous material. This effect is used to measure the elastic modulus of polycrystalline [166] and porous solids [167, 168] by acoustic methods where a relationship of the form $E \propto \rho v^2$ is used. In this technique, the mean free path of elastic waves is much larger than any defects or imperfections in the material to make sure that the measurements are not affected by scattering. If we substitute $E \propto \rho v^2$ in Eq. (13) we can derive a relationship between the thermal conductivity of a material and its elastic modulus.

$$E \propto \left(\frac{9}{\rho \ell^2 C_p^2}\right) k^2 \tag{16}$$

This equation shows that for the same density (and same specific heat), if the material is free of defects (totally interconnected) so that the mean free paths for the phonons and acoustic waves are similar, $E \propto k^2$. Since the majority of heat carriers should be low-frequency acoustic phonons [128, 129] in a relatively defect-free material like the sintered xerogel, we should expect this relationship to hold as shown in Fig.9.25. There is other evidence in the literature that supports Eq. (16). Emmerling and Fricke [163] used a simulation procedure to produce three-dimensional gel structures, from which two important parameters can be extracted: (i) the fraction α of interconnected mass of the gel network and (ii) the ratio γ of Pythagorean distance to the minimum path length on the gel backbone. The product $\alpha\gamma$, which enters into important macroscopic parameters such as modulus or solid thermal (and electrical) conductivity, was found to scale with an exponent that is only a function of the mass fractal dimension, a factor that can be largely influenced by processing. Young's modulus is predicted to vary as the square of the thermal conductivity according to this concept, which is the relation we have observed with our sintered films.

Other properties of nanoporous films such as the dielectric constant and refractive index measurements are found, like the thermal conductivity, to be linearly related to density (or porosity) [36]. This points to a frequency dependence to the measurements. The dielectric constant is normally measured at 1 MHz using metal–dielectric–metal capacitors and the refractive index is normally measured at optical wavelengths. Surface acoustic wave measurements of Young's modulus and both photothermal and 3ω measurements of thermal conductivity occur using disturbances whose wavelengths are much larger than the scale of the microstructural features of the film and often, much larger than the film thickness. Hence, these techniques are not sensitive to microstructure but only to the overall measure of porosity, so the linear dependence is observed. Nanoindentation probes the material at all length scales since it has to penetrate the material and penetration cannot exceed more than 10% of the film's thickness. Thus, it can see 'beam bending' in porous films whereas a surface acoustic wave cannot. This can be readily seen in the data of Baklanov *et al.* [79] and Jain *et al.* [22] (Fig. 9.26) where porous MSQ modulus scales linearly with porosity whereas porous xerogel modulus scales with the square of the porosity.

9.6 Interaction of porous materials with metals and barrier materials

In an interconnect structure, the dielectric is in contact with other materials, such as a metal (copper), a diffusion barrier (e.g. Ta or Ta nitride), or a hard mask (Si nitride). It is important to minimize the interactions between these different materials to insure long-term device stability though some minimal interaction is necessary to provide bonding and good adhesion between layers. These interactions, such as interdiffusion or interfacial reaction, should be limited to a few nanometers beneath the interface.

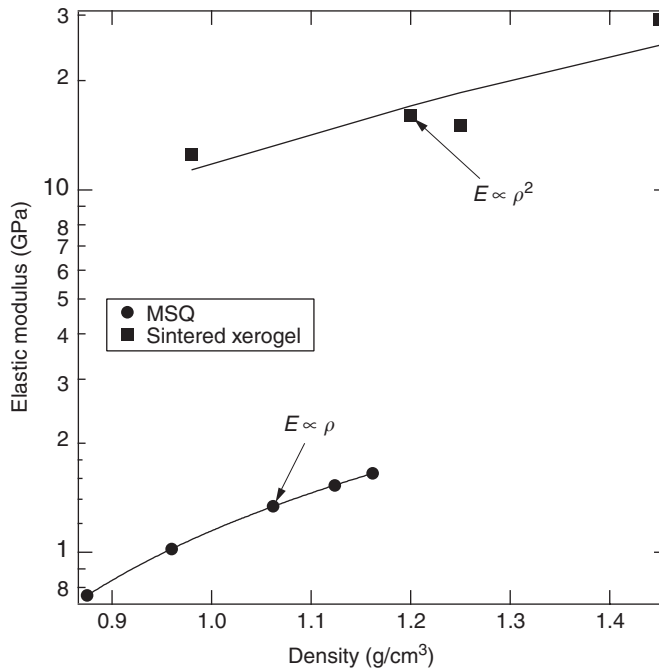

Fig. 9.26 Elastic modulus of MSQ and sintered xerogel materials as a function of density. Data measured using surface acoustic wave (MSQ) [79] and nanoindentation (xerogel) [61] techniques.

Copper, the material of choice for IC metallization, is known to be a fast diffuser through both dense SiO_2 and Si. This indicates the need for an effective diffusion barrier if silica-based low-κ dielectrics are used. The bulk of the semiconductor diffusion barrier literature is concerned with investigating barriers between copper and solid Si or SiO_2. Most of the reported work is concentrated on Cu/barrier interactions and barrier failure mechanisms and not on barrier/dielectric interactions. In this section, we concentrate on barrier/dielectric interactions because there is a concern that the porosity and very large internal surface area of porous dielectrics may enhance the diffusion of barrier materials through them, thereby rendering them ineffective as a dielectric. Since the activation energy for diffusion along extended defects tends to scale with the melting point of the material [169], copper diffusion barriers currently under investigation include refractory metals and their compounds TiW, TiN, TiN_x, $TiSi_2$, Ta, TaN, Ta_2N, W, WN, W_2N, WN_x [170], and Al [171]. Currently, it appears that Ta-based barriers are most likely to be used, but organic barriers may also prove effective [172].

In this section, we will consider the adhesion, stability, and thermal and electric field assisted diffusion interactions between metals, barriers, and low-κ dielectrics, especially porous low-κ materials. All are important interactions and will eventually dictate which types of low-κ materials will prove suitable for future generations of integrated circuits.

9.6.1 Adhesion and stability

Adhesion is a complicated phenomenon depending on many factors including the strength of intermolecular forces between adjacent layers, the presence of any interfacial reactions or interdiffusion between layers, any residual stress present in the substrate or deposited layers, and the porosity of the materials making up the layers [173, 174]. There are several ways to test the adhesion and stability of a thin film on a substrate. Classical methods like the Scotch Tape test or stud-pull test are done at room temperature and are semi-quantitative. Methods like high-temperature annealing use thermal energy to fuel the rearrangement of the material on the surface and hence the amount of thermal energy required for rearrangement is a measure of stability and adhesion. The surface forces apparatus [175] can also be used to measure adhesion. In any of these schemes, the testing environment also plays a role in stability.

9.6.1.1 Copper

The adhesion and stability of copper films has been studied since copper is the metal of choice for future interconnects. It has been reported [176] that as-deposited copper adheres well to SiO_2, but after annealing at temperatures above 200°C, the copper occasionally lifts from the substrate, indicating thermal-stress-related adhesion failures. We have looked at copper interaction with xerogel materials in an attempt to determine whether Cu will adhere and diffuse within the xerogel material. As a baseline, we considered the stability of Cu films on dense SiO_2. Rogojevic *et al*. [177] observe that upon annealing at 450°C, Cu tends to dewet and form islands on solid SiO_2 surfaces due to poor wetting (high interfacial energy). Nicolet [178] also reports that copper does not stick to SiO_2 and tends to ball up during annealing. Thus, any diffusion barrier used with copper metallization should act as an adhesion promoter too, regardless of whether the dielectric is silica, organic, or hybrid based. In contrast, when Cu was deposited on nanoporous xerogel films, holes and hillocks are formed in the Cu film, which may indicate an initial stage of dewetting. This occurred only upon annealing at 548°C, Fig. 9.27. Thus, since dewetting occurs at a higher temperature, Cu films appear to be more stable on nanoporous silica xerogel surfaces even at high porosities (70%) than on dense SiO_2. A 500-Å Si_3N_4 layer deposited on top of the Cu layer prevents oxidation and Cu dewetting at temperatures as high as 640°C.

9.6.1.2 Tantalum

Tantalum has been investigated as an adhesion layer/diffusion barrier between copper and SiO_2 or Si substrates. Gallais *et al*. [179] have found that Ta layers deposited on SiO_2/Si substrates showed the presence of tantalum oxide and/or tantalum silicide in the interface region. However, Buchwalter [180] points out that the peel strength of a Ta film deposited on SiO_2 is about 30 J/m^2, which is extremely poor, indicating that Ta films are close to delaminating spontaneously. It is also suggested that Ta does not seem to form a silicide with SiO_2 under given

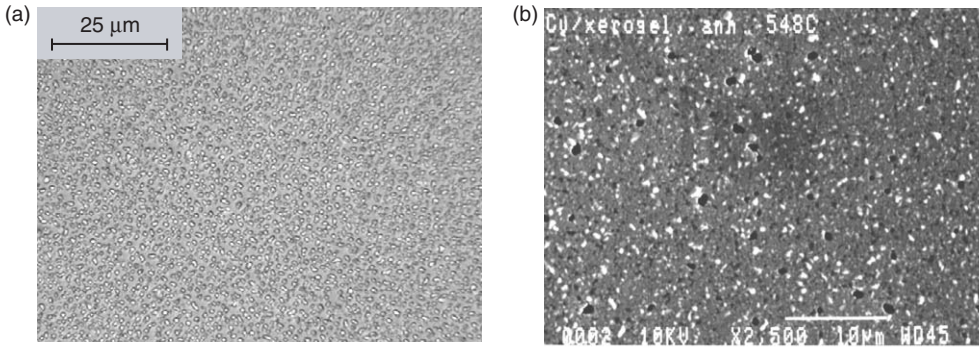

Fig. 9.27 Micrographs showing the morphology of Cu on solid SiO_2 and on xerogel upon annealing: (a) Cu on SiO_2 annealed at 450°C in N_2; (b) Cu on 70% porous xerogel annealed at 548°C in N_2 [177] (reprinted with permission).

conditions. Although thermodynamic considerations show that Ta is able to chemically react with SiO_2 [181, 182], kinetic limitations and surface impurities may prevent the reaction from occurring, and thus the adhesion may not be as good as expected. An initial investigation of Ta, TaN, and TiN as possible diffusion barriers for porous SiO_2 has been reported in Kumar *et al.* [183]. Data on interactions of metals with organic dielectrics is scarce, but we may speculate that since the metal cannot react with the organic surface, adhesion should be even more of a problem.

In an inert environment such as N_2, Ta remains stable on the surface of nanoporous silica xerogel when annealed at temperatures up to 450°C as shown by Rogojevic *et al.* [184]. However, the presence of even trace amounts of oxygen in the annealing environment promotes the oxidation of Ta thin films. The Ta films buckle and the extent of buckling increases with increased annealing time, temperature, and oxygen partial pressure. The buckles have a classic telephone cord (sinusoidal) morphology shown in Fig. 9.28. A 500-Å Si_3N_4 layer deposited on the Ta is enough to prevent the oxidation of Ta at temperatures up to 640°C and provides an additional frictional surface so that buckling of Ta does not occur [184]. Under these conditions, Ta was not found to diffuse into the xerogel (beyond the RBS threshold). RBS microbeam analysis shows that the diffusion-like RBS spectra in uncapped annealed samples are entirely due to the laterally nonuniform surface morphology (analogous to roughness). The RBS spectra of the xerogel surface, collected from the samples after the Ta film peeled off the xerogel surface, also show no Ta diffusion through xerogel up to 640°C. The porosity of the xerogel eventually reduces the adhesion of Ta due to the reduced contact area between the materials. An additional adhesion promoter or a strategy for improved adhesion (by densifying the surface layer) is necessary if Ta is to be used as a diffusion barrier for Cu.

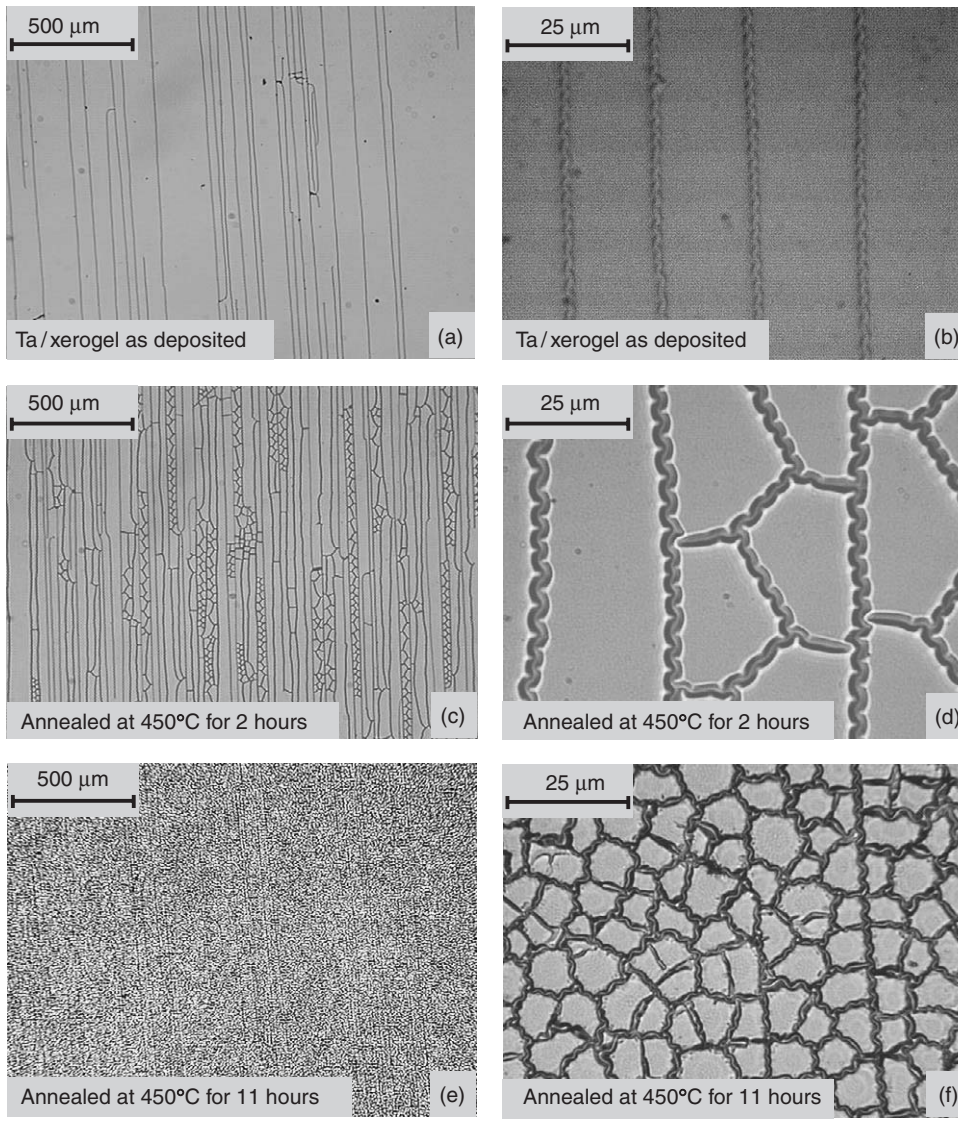

Fig. 9.28 Ta instability on xerogel surface [184] showing the classic telephone cord morphology.

9.6.2 Diffusion in the absence of an electric field

The issue of interdiffusion of metals and barriers with low-κ dielectrics has received considerable attention with reports of diffusion of metals in silica-based xerogel materials occurring even at room temperature [183]. However, we have demonstrated that neither Cu nor Ta diffuse into a silica xerogel material via a thermally activated process alone [184]. The reports of pure thermal

diffusion relied on Rutherford backscattering spectroscopy (RBS) detection. We determined that what was taken as diffusion was actually a distortion of the RBS spectrum due to agglomeration or dewetting of the metal or barrier material on the surface [184]. Stabilization of the surface by strict removal of oxygen from the annealing environment and by capping with a barrier of silicon nitride showed that thermal diffusion would not occur at the tantalum/xerogel interface even at temperatures as high as 640°C.

9.6.3 Field-assisted diffusion

Field-assisted diffusion of metals into dielectrics is faster than thermal diffusion since the electric field provides a strong driving force for movement of the metal. Here, we must distinguish between several mechanisms for metal movement including bulk versus surface diffusion and motion through the material as a neutral versus an ionic species. The electric field only augments the transport of charged species and so has little effect on neutral species. The presence of porosity in a material enhances the surface area and so can enhance or retard diffusion depending on the types of interactions that exist between the diffusing species and the matrix material. For silicate-based materials, an increase in the surface area increases the number of defects in the material and so can enhance the diffusion of metal species along the surface. It can also enhance the conversion of neutral metal species to ions that can then diffuse in the bulk, or can retard the diffusion of metal species within the silicate matrix due to a decrease in the contact area between the materials. In polymers the same effects may or may not occur depending on the surface chemistry of the polymer. The elucidation of how porous materials behave is still an open area of research. In the next few paragraphs we will present some of the work done on low-κ materials with special emphasis placed on silica-based xerogel materials. We will try and highlight the differences and similarities between diffusion in those materials and diffusion in other forms of low-κ dielectrics.

The field-assisted diffusion experiments on silica xerogel materials were conducted using a 1-MV/cm field and temperatures between 100 and 300°C. MIS (metal–insulator–silicon) capacitor structures like those used by Loke *et al.* [185] were used in these studies. Xerogel results were referenced to diffusion through PECVD oxide and Cu diffusion experiments were referenced to corresponding Al experiments since Al has a negligible diffusion rate through silicate materials. In general, the leakage currents through xerogel and SiO_2 capacitors were found to be very small, approaching the noise level of the instrumentation in a number of cases (10^{-11}–10^{-9} A, depending on the temperature). The representative results of *I–t* measurements on Al/xerogel/Al/SiO_2/Si and Cu/xerogel/Al/SiO_2/Si samples are shown in Jain *et al.* [60] and discussed below.

9.6.3.1 Solid conventional and low-κ materials

A number of investigators have looked at copper diffusion in a variety of dielectric materials ranging from conventional silicon-based materials [186–188], to a variety of polymeric materials

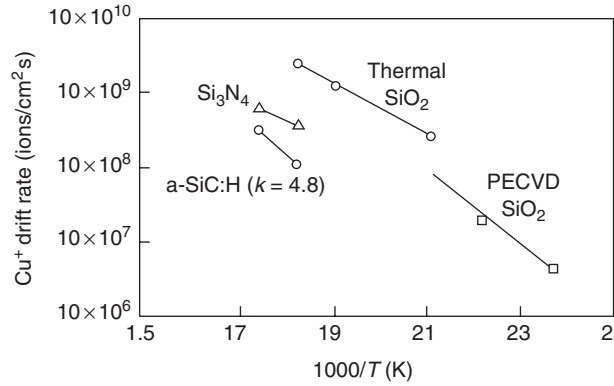

Fig. 9.29 Initial copper drift rate in a variety of inorganic, silicon-based dielectrics. Nitride and carbide dielectrics were stressed at a field strength of 2.8 MV/cm; thermal oxide was stressed at a field strength of 2 MV/cm and PECVD oxide at a field strength of 1 MV/cm (adapted with permission from Ref. [186]).

[189–195], and finally in silsesquioxanes [196, 197]. Figure 9.29 is adapted from a paper by Lanckmans *et al*. [186] showing the drift rate of copper ions through a variety of inorganic dielectrics as a function of temperature. Notice that the slopes of these lines are all fairly similar indicated a similar activation energy barrier for diffusion in each.

Abdul-Hak *et al*. [187] measured Cu diffusion into SiOF, TEOS-PECVD SiO_2, and thermal oxide. Though not reporting actual values for the diffusivity or activation energy, they do discuss their results in terms of time to failure analysis. They attribute trends they see in the mean time to failure to moisture absorption in the dielectric. The absorption of moisture is a big problem because the moisture can oxidize the Cu allowing it to easily penetrate into the oxide matrix.

Some of the most comprehensive data on Cu ion drift rate in low-κ dielectrics was presented by Loke *et al*. [185]. Figure 9.30 is taken from their work. Interestingly enough, most activation energies for these materials are fairly similar. Drift rates for the various materials increase in the order nitrides < polymers < oxides. This ordering depends upon a number of factors including the glass transition temperature of the polymer, the amount of moisture absorption, the propensity of the material or defects within the material to provide oxidation sources for the Cu metal, and whether Cu can diffuse into the material as an ion or as a neutral atom. Thus, oxides that absorb water and can provide species to oxidize Cu on its surface have higher drift rates than polymers or nitrides. The latter absorb little moisture and do not have many species within them that can oxidize the Cu metal and allow the high electric field to drive the ions into the dielectric.

The effect of the glass transition temperature of the polymer on Cu diffusion can be seen in Fig. 9.31. Cu concentration profiles and calculated diffusivities for Flare^{TM} low-κ dielectric are shown as a function of heating time at 200°C [189]. Note the sharp increase in diffusivity at 400°C.

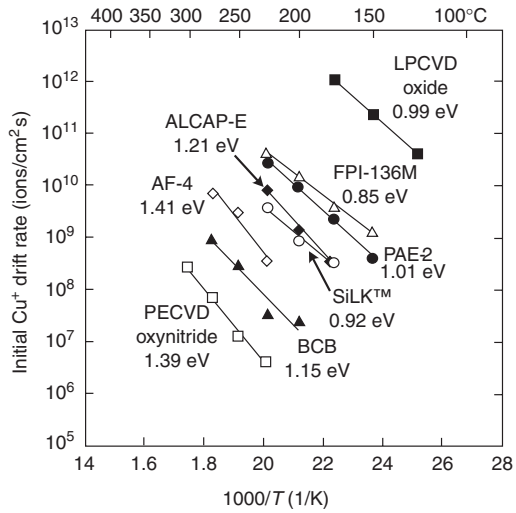

Fig. 9.30 Cu ion drift rate through a number of low-κ and conventional dielectrics as a function of temperature. All were subjected to bias temperature stressing at a field strength of 1 MV/cm. The activation energies for each material are also given in the figure (adapted from Loke *et al*. [185] with permission). (© 1999 IEEE)

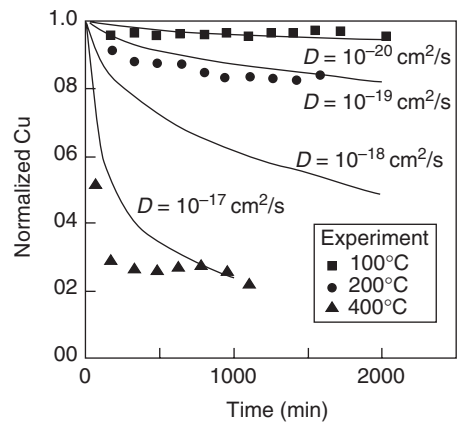

Fig. 9.31 Cu ion concentrations in a Flare™ low-κ dielectric film upon heating at 200°C for 12 h. Notice the great change in diffusivity when the heated polymer passed its glass transition temperature (redrawn from data presented in [189] with permission).

The glass transition temperature for Flare™ is reported to be 250°C and one can see the abrupt change in both the rate and shape of the concentration profile within the polymer. Transition electron microscopy clearly showed the clustering of Cu metal atoms in the polymer that mirrors clustering on the surface (Fig. 9.32). Thus, both bulk and surface diffusion occur. Similar observations were made for Cu on polyimides [189, 190].

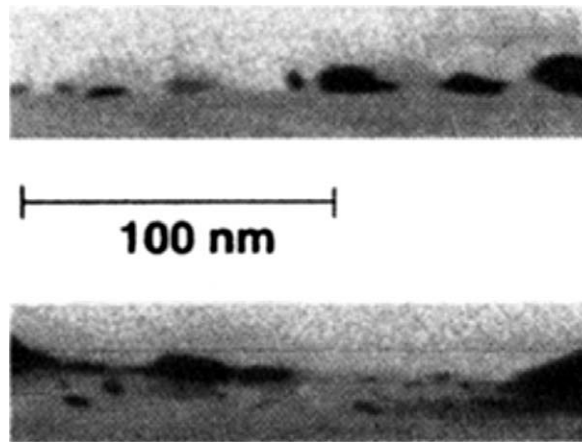

Fig. 9.32 TEM micrographs of Cu in Flare™. The upper figure shows clusters of Cu atoms on the surface of the polymer and the second shows Cu clusters within the polymer after heating for 12 h at 200°C (adapted from [189] with permission).

Table 9.5 Diffusion coefficients for Cu in various dielectric materials

Material	Diffusion coefficient (cm^2/s)	Temperature range (°C)	Reference
Flare™	10^{-17}–10^{-18}	200–300	[189]
Polyimide	5×10^{-18}–5×10^{-16}	200–460	[191]
Kapton™	10^{-18}–10^{-15}	27–350	[190]
Teflon™	3.86×10^{-18}	330	[192]
SiO_2	10^{-20}	300	[200]
Phosphosilicate glass (PSG)	10^{-15}	300	[212, 213]

Finally, diffusion of Cu into silsesquioxanes has also been investigated [196, 197]. Liu *et al.* [196] found that copper diffuses rapidly into hydrogen silsesquioxane (HSQ) due primarily to moisture absorption by the dielectric. Treating the material in a NH_3 plasma nitrided the surface and provided a passivation layer that effectively blocked Cu diffusion. In a related study, Chang *et al.* [197] studied Cu diffusion into methyl silsesquioxane (MSQ). Here, they also found Cu diffusion related to moisture absorption and that Cu diffusion could be effectively blocked in this material by exposure to a hydrogen plasma. Both these studies and others [194, 195] show the profound effect that surface chemistry has on the diffusion of Cu (see Table 9.5).

9.6.3.2 Porous materials

Little, if any, quantitative work has been done with porous dielectrics. The following sections will report on initial work the authors have been conducting looking at metal, and barrier material

diffusion into silica xerogel films. These films have been chosen as a prototypical material since the porosity and surface chemistry are easily controlled.

9.6.3.2.1 Current–time measurements

All of the *I–t* curves, for xerogel or SiO_2 samples, made with either Cu or Al electrodes, show that an initial decrease in current with time occurs [177]. The results for samples made with inert Au electrodes were essentially the same as for those with Al electrodes. This behavior is attributed to space charge accumulation that reduces the effective electric field across the dielectric and thus slows down the further drift rate [185]. Some of the observed current decrease may also be caused by the capacitance inherent in the switch relays and cables of the testing equipment [198]. The current levels for xerogel capacitors are 1–2 orders of magnitude higher than for PECVD SiO_2 capacitor structures. This result suggests that the high internal surface area of the xerogel material promotes diffusion or at least charge migration along a surface path. The nanoporous xerogel can be viewed as an amorphous SiO_2 (with some C and H), but with a higher defect density than dense SiO_2 due to its highly branched microstructure. These defects (broken or dangling bonds, –OH groups) can cause higher leakage currents. Moisture absorption due to the high surface area also leads to higher currents and if the ambient environment is not purged with N_2 during testing, the measured currents are 1–2 orders of magnitude higher in the porous xerogel material.

Since Cu is known to diffuse easily through a range of materials when biased [185], the current measured from Cu capacitors should be significantly augmented by Cu ion drift from the electrode into the dielectric. However, we find that currents from Cu/xerogel capacitors are unexpectedly about an order of magnitude lower than from Al/xerogel or Au/xerogel capacitors [177, 199]. It is unclear what the causes of this effect are since such behavior is not observed for pure, dense silica substrates. Since neither Au nor Al are expected to diffuse into the xerogel substrate as ions, we speculate that there is no significant Cu ion drift into the xerogel. The low current indicates that there is also less electron–hole injection from the Cu/xerogel than from the Al/xerogel interface. The Al/SiO_2 interface is known to be stable due to the good chemical bonding of Al, which forms a silicate at the interface. We find that Cu adhesion to xerogel is moderate – Cu passes the Scotch tape test on about half the surface, while Al fails easily. This suggests that Cu could also form chemical bonds at the xerogel interface, which at the same time reduces the charge injection levels.

The *I–t* data can be used to find the activation energy for the capacitor current. An Arrhenius-type plot of these data is shown in Fig. 9.33. Data are plotted for both the initial current and the current reached after 10 min of bias. The activation energies range from 0.42 to 0.55 eV, which is less than that for most other low-κ dielectrics (except Kapton™ [190]) or for Cu motion through solid SiO_2, according to the literature values for Cu mobilities [200].

Copper behavior on dense SiO_2 is different from that on the xerogel surface. For dense SiO_2, Cu/SiO_2 samples show higher leakage currents than Al/SiO_2 samples, as expected [185]. In addition, the Cu/SiO_2 capacitor leakage current at 300°C shows a distinctly different behavior

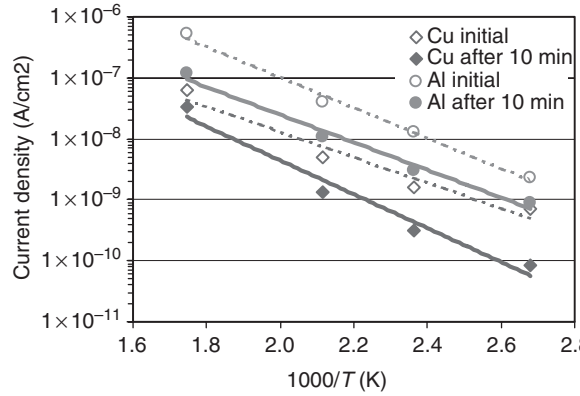

Fig. 9.33 Activation energy for copper and aluminum drift current through silica xerogel materials [177] (reprinted with permission).

from all the other *I–t* curves. The current increases with time with occasional spiking. Current spiking has been observed before in Cu/SiO_2 [201] and Al/soda-lime glass samples [202]. It is attributed to a 'self-healing' phenomenon. It is postulated that metal diffusion damages the dielectric, which causes the current to increase rapidly, but the damage is repaired after a while by restructuring, and the current returns to the base value [202]. A more gradual increase in the base value of the current is consistent with the theory of Kapila and Plawsky [203, 204] that postulates for the metal to diffuse through the glass, it must be oxidized first. The oxide is formed at the anode/glass interface, and serves as a source of positive metal ions. Since the oxide thickness increases with time (logarithmic, corrosion-like dependence), more metal ions become available for diffusion and therefore, the current increases too. The results of Rogojevic *et al.* [177] with the Cu/SiO_2 sample at 300°C are reproducible, although the shape of the current fluctuations is random, and there may be a short period (up to 5 min) before the fluctuations appear. The lag period, during which the current may decrease, is also consistent with the observation of Kapila and Plawsky [203, 204]. Therefore, we conclude that slight Cu oxidation may occur at 300°C by the reaction with the SiO_2 substrate, which leads to increased Cu diffusion and accelerated dielectric breakdown.

Several Cu/xerogel samples tested showed smooth, declining, *I–t* curves in the 10–15 min tests at 300°C. However, if the same test is repeated with the same capacitor, Cu/xerogel samples exhibit current fluctuations and increasing current with time. An example is shown in Fig. 9.34. The same capacitor was tested repeatedly up to 300°C. The order of the tests was: 150°C, 150°C repeated, 200°C, 200°C repeated, 300°C, 300°C repeated, 200°C repeated. The current increase can be observed after testing at 300°C, similar to that in Cu/SiO_2 capacitors. Thus, we have an indication that copper could diffuse into xerogel at 300°C, but only after a delay period of at least 10 min.

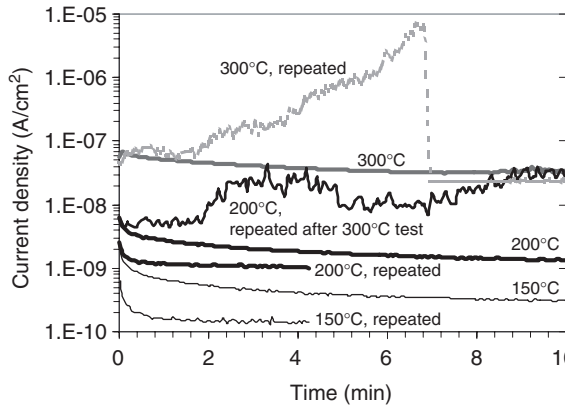

Fig. 9.34 Leakage currents for Cu on xerogel substrate [177] (reprinted with permission).

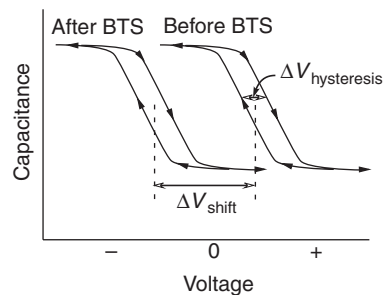

Fig. 9.35 Schematic diagram of a typical capacitance–voltage curve before and after bias-temperature-stressing injects ions into the dielectric.

Several Cu/xerogel/SiO_2 and Al/xerogel MIS structures also were used to measure the current. The results were consistent with those of the MIM capacitors. The MIS capacitor samples were subjected to the BTS test for 1 h up to 300°C, and were subsequently tested by RBS. RBS microbeam was used in order to limit the area probed by the beam within the 1.5-mm diameter Cu dot. RBS showed no visible Cu diffusion into xerogel after the BTS test. It is possible that Cu diffusion occurs, but Cu concentration levels in xerogel may be below the RBS sensitivity (~1×10^{20} atoms per cm^3 of dense silica).

9.6.3.2.2 Capacitance–voltage measurements

C–V measurements on capacitor structures are sensitive tests for detecting charge in a dielectric and have been used to gauge the injection and drift of charge in low-κ materials. In a *C–V* test, the voltage applied to the capacitor is swept from negative to positive values and back again while measuring the capacitance of the structure. Hysteresis effects upon forward–backward sweep and wholesale shifts in the curves themselves after bias-temperature stressing indicate the presence of accumulated charge in the dielectric (see Fig. 9.35). *C–V* testing of xerogel samples

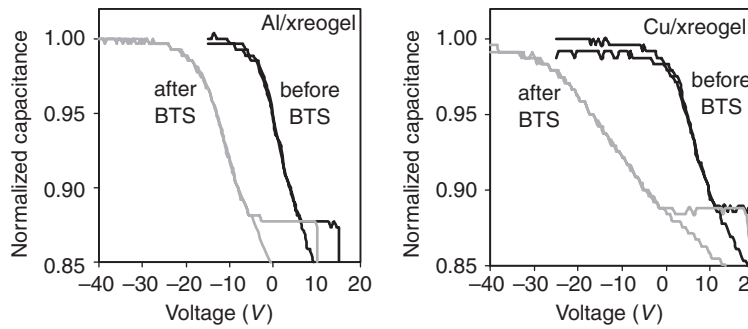

Fig. 9.36 CV curve for xerogel capacitors [177]: (a) Al–xerogel capacitors measured at a temperature of 100°C; (b) Cu–xerogel capacitors measured at temperature of 150°C (reprinted with permission).

was performed in a N_2 purged environment to avoid hysteresis effects due to moisture absorption in the high surface area material. *C–V* testing was done before and after bias-temperature stressing at 1 MV/cm. Though sensitive, the conventional *C–V* shift experiment cannot readily distinguish between injected charge due to electrons or holes and charge due to the diffusion of copper ions into the dielectric. Regardless, it is a good gauge of what may happen, especially as the porosity and surface chemistry of the dielectric change.

Figure 9.36 shows the results of a *C–V* test for Al and Cu xerogel capacitors. Each curve in these figures represents one *C–V* sweep and sweeps were made both before and after bias-temperature stressing. The lack of hysteresis in these curves indicates no mobile charges (metal or hydroxyl ions) are present in the dielectric either before or after the stressing. The *C–V* curves show an overall negative shift (toward negative voltages) after biasing indicating positive charge accumulation in the dielectric. An Al/xerogel/SiO_2/Si/Al sample shows a *C–V* shift of ~ −12 V when stressed at only 100°C for 3 min. Cu/xerogel/SiO_2/Si/Al capacitors showed no *C–V* shift when stressed under the same conditions, but when stressed at 150°C for 3 min, Cu capacitors showed a negative shift (positive charge) of ~ −12 to −15 V. These results are unexpectedly high for such mild conditions. Al should not diffuse under bias, since Al would have to be triply ionized at the interface to enter into the silicate lattice. Therefore, the observed *C–V* shift for the aluminum structure can be assigned to positive charge (hole) injection and accumulation in the dielectric. Large *C–V* shifts after mild stressing conditions have been observed before for direct metal/polymer or Si/polymer contact [185], but no explanation of this phenomenon exists in the literature. We found that stressing Al/xerogel samples at 100°C and Cu/xerogel at 150°C resulted in the same levels of leakage current: 5×10^{-10} A/cm^2. This supports the hypothesis that the *C–V* shift is caused by charge accumulation in the dielectric, due to the electron leakage current (since it is proportional to the charge passed), and not due to the metal ion drift of copper.

Xerogel materials are rendered hydrophobic by a surface treatment during their processing. This may affect both the leakage current and the drift of ions from the metal layer. To separate

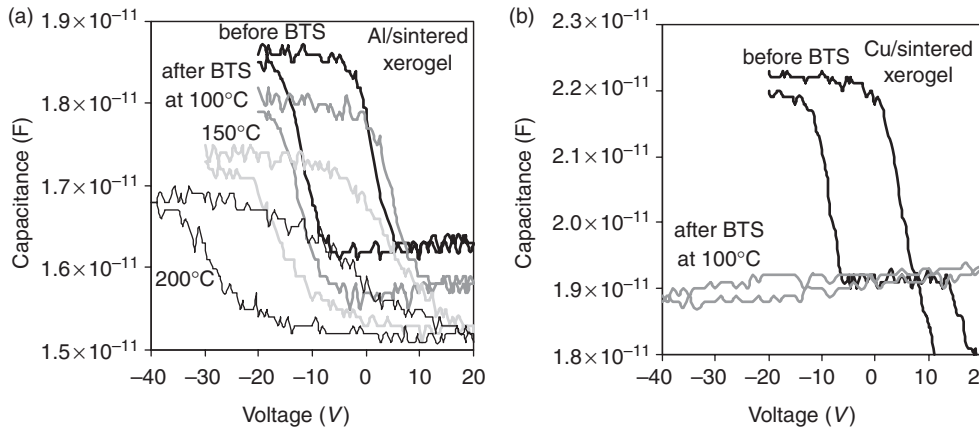

Fig. 9.37 *C–V* curve for xerogel film [177]. The *C–V* curves and their corresponding *I–t* curves during bias-temperature stressing are shown so that the current passed through the dielectric is known (reprinted with permission).

the effect of surface chemistry from the effect of porosity, we prepared xerogel capacitors in which a 40% porous xerogel film was annealed at 650°C (sintered) in air before metal deposition. This process removes the organic groups from the surface of xerogel and destroys its hydrophobicity while leaving the porosity practically unchanged.

Figure 9.37 shows the results of tests on these sintered materials. A *C–V* test was first done on as-deposited samples, prior to bias-temperature stressing. There are two significant differences in the *C–V* curves obtained from capacitors with sintered xerogel from those with regular (surface modified) xerogel. Comparing Figs 9.36 and 9.37, one can see that the most prominent feature of the *C–V* curves of sintered samples (Fig. 9.37) is the hysteresis that occurs during each *C–V* sweep, even though testing was done in a N_2 purged ambient. Thus, mobile charges caused by moisture adsorption in the dielectric are present even in a supposedly 'dry' environment. Moisture is more strongly bound (hydrogen or chemically bonded) in sintered xerogel than in surface-modified xerogel. Simply purging the ambient environment with inert gas eliminated loosely (physically) adsorbed moisture from surface modified xerogels. Removal of water from the sintered xerogel would require high-temperature baking. Upon repeated testing at room temperature, and particularly after the BTS test at elevated temperature, the capacitance of the sample decreased [205]. This indicates that some of the loosely adsorbed moisture was slowly being removed as the ambient was purged by N_2, yet the hysteresis remained.

Figure 9.37(b) shows that Cu/sintered xerogel samples show large *C–V* shifts after stressing at only 100°C for 3 min (*C–V* curve becomes horizontal). Comparing the 100°C curves of Fig. 9.37(b) and (a) shows that Al/sintered xerogel shows much smaller shifts even at temperatures up to 200°C. These trends in *C–V* shifts are the expected behavior for Al and Cu on silica. Al is more stable and does not diffuse and so should show very small *C–V* shifts, while Cu is

expected to diffuse into uncapped silica xerogel and should show a large *C–V* shift as indicated in Fig. 37(b). Similar results were shown for solid SiO_2 that had been modified with a self-assembled monolayer diffusion barrier [172]. In that process, the monolayer inhibited diffusion of the metal into the SiO_2. The xerogel fabrication process uses the same techniques to render the material hydrophobic and so it is possible that surface modification inhibits the injection of charge and the diffusion of ions into the dielectric.

The higher *C–V* shift of Al capacitors, compared to Cu capacitors, has recently been confirmed by one research group using our xerogel films [199], and by another group using a commercial organo-silicate low-κ dielectric [206].

9.7 Diffusion model for porous dielectrics

It is not known if porosity will enhance or retard the diffusion of Cu^+ ions and other impurities in a low-κ dielectric. It can be reasoned that the reduced available cross-sectional area for diffusion, due to porosity, could lead to reduced diffusion through the porous film. Similarly, the tortuosity of the porous structure makes the effective path for the diffusion across the film 1.5–6 times longer than the actual film thickness [207, 208], and thus reduces the apparent diffusivity. However, the existence of a surface path for diffusion, where we expect higher diffusivity, leads to the possibility of enhanced overall diffusion. In the only reference that treats the diffusion of copper through a porous solid that we are aware of [209], Cu diffusivity through porous silicon was found to be seven orders of magnitude lower than Cu diffusivity in bulk Si. Therefore, diffusion through porous materials can be significantly different than through the dense material.

Diffusion of a gaseous species or solute through the pores of a porous material, such as a catalyst pellet, has been investigated in detail [210, 211]. For the purpose of mathematical analysis, the complex pore structure is usually approximated by a simplified one, such as a cylindrical pore. The fact that the path of the diffusing species is longer in the irregular structure than the simplified one is accounted for by a tortuosity factor, τ. A short historical review and early references can be found in Ref. [210]. However, there is almost no literature about the diffusion through or along the solid phase of the porous material. To help in the analysis of field-assisted diffusion or *C–V* tests, a model for diffusion of species in a porous dielectric material is needed.

There are two separate diffusion paths through a porous material; bulk and surface. Three driving forces for mass transfer can be identified: the concentration gradient, the electric field, and the curvature gradient. Modeling of wetting using the Surface Evolver program [205] shows that the latter mechanism of transfer through the pores is negligible if the contact angle of the two materials under consideration is $> 90°$, such as for Cu/SiO_2 [205].

A rigorous mathematical analysis of diffusion and drift phenomena requires knowing the details of the material's microstructure, and solving the three-dimensional mass transfer equations. Even if one had detailed information on the geometry of the microstructure, the simulation process could be extremely time consuming. Alternatively, an idealized microstructure can be

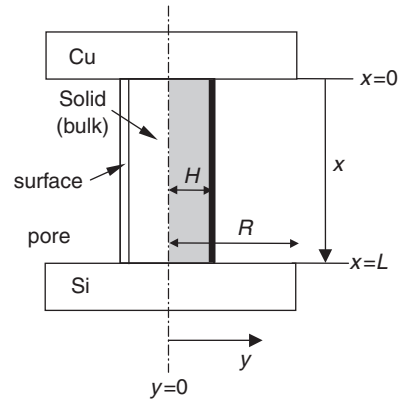

Fig. 9.38 Computational domain for diffusion through porous media [177].

devised, which is easier to analyze mathematically, as in Burganos and Sotirchos [211]. We use the approach of idealizing the network by straightening the solid walls. If the actual dielectric film thickness is L, the straightened representation is of length τL, where τ is network tortuosity. One half of the straight wall can be taken as the computational domain, as shown in Fig. 9.38 by the shaded region. The length of the solid wall in the model is taken to be L, for simplicity, but we recognize that L is the thickness of the film times the tortuosity. H represents the half-wall thickness of the dielectric and R is the pore radius defining the separation distance between solid walls.

The mass transport through the bulk can be considered two-dimensional in the simplified representation (three-dimensional in reality) and governed by the following equation for the bulk concentration:

$$\frac{\partial c_b}{\partial t} = D_b\left[\frac{\partial^2 c_b}{\partial x^2} + \frac{\partial^2 c_b}{\partial y^2}\right] - \mu_b E\frac{\partial c_b}{\partial x} \tag{17}$$

where c_b is the Cu^+ concentration in the bulk of xerogel (in xerogel wall), D_b is Cu^+ diffusivity in the bulk, μ_b is Cu mobility in the bulk, and E is the electric field (assumed constant). μ_b is taken to depend on D_b by the Einstein relationship: $\mu_b = D_b q/k_B T$, where q is the particle charge, k_B is Boltzman's constant, and T is the absolute temperature. The mass transport at the surface is considered two-dimensional. If the concentration is integrated over the surface thickness (y-direction), and if the concentrations in both regions (bulk and surface) are taken equal at $y = H$, then, the two-dimensional problem becomes a one-dimensional problem after integration and from continuity, one obtains the following equation for the surface concentration:

$$\frac{\partial c_s}{\partial t} = D_s\frac{\partial^2 c_s}{\partial x^2} - \mu_s E\frac{\partial c_s}{\partial x} - D_b w\frac{\partial c_b}{\partial y}\bigg|_{y=H} \tag{18}$$

Here, c_s is Cu^+ concentration at the surface of xerogel network (per unit volume), D_s is Cu^+ diffusivity at the surface, μ_s is Cu^+ surface mobility (taken to depend on D_s by Einstein's relationship), and w is the surface thickness. The last term of Eq. (18) is the surface–bulk exchange term attributable to Cu^+ being transported from the surface into the bulk by diffusion.

The concentration at the surface of the film, $x = 0$, is c_e, the equilibrium concentration. Furthermore, the initial concentration in the bulk and at the surface in the interior of the film, $x > 0$, is zero. Also, at the Cu/xerogel interface the concentrations on the surface and in the bulk of the film are equal, as are the fluxes in the y-direction. Symmetry exists at the plane $y = 0$. Therefore, the boundary conditions for Eqs (17) and (18) are

$$c_b(x,0) = c_s(x,0) = c_b(L,y,t) = c_s(L,t) = \frac{\partial c_b}{\partial x}(x,0,t) = 0 \tag{19}$$

$$c_b(x, H, t) = c_s \tag{20}$$

$$c_b(0, y, t) = c_s(0, t) = c_e \tag{21}$$

Equations (17) and (18), together with the boundary conditions (19)–(21), enable us to obtain the concentration profiles $c_b(x, y, t)$ and $c_s(x, t)$. Knowing the concentration profiles, the flux of Cu^+ ions in the bulk, J_b, and the flux of Cu^+ ions at the surface, J_s (ions/cm^2 s), can be obtained as:

$$J_b = -D_b\frac{\partial c_b}{\partial x} + \mu_b E c_b \tag{22}$$

$$J_s = -D_s\frac{\partial c_s}{\partial x} + \mu_s E c_s \tag{23}$$

The total flux of Cu^+ ions through the xerogel film can then be determined as

$$J_t = \frac{J_b H + J_s w}{R} = (1-\varepsilon)\left(J_b + J_s\frac{w}{H}\right) \tag{24}$$

where $\varepsilon = (R-H)/R$ is porosity. The porosity is known and can be controlled. A value of more practical importance is the current density, which can be measured directly in experiments. The current density, I (in A/cm^2), can be calculated as $I = J_t\, q$, where q is the elementary charge (1.60×10^{-19} C) carried by the copper ion, Cu^+.

The time (t), electric field strength (E), temperature (T), film thickness (L), and porosity (ε) can all be easily varied or manipulated during an experiment. The practical range of interest of these variables is $t > 1$ s, $20°C < T < 300°C$, $0.5\,\mu m < L < 10\,\mu m$, and $0 < \varepsilon < 1$. The model results of interest are the concentration profiles $c_b(x, y, t)$ and $c_s(x, t)$, the average concentration, $\bar{c}$, the time to completely fill (saturate) the xerogel with Cu to $0.99c_e$ level, t_{fill}, the Cu^+ current density at the anode, I_{top}, and the substrate, I_{bot}.

The model parameters inherent to the materials system, which need to be estimated before we proceed with the calculations, are: the surface thickness (w), the wall half-thickness (H), the bulk Cu diffusivity (D_b), the surface diffusivity (D_s), and the Cu solubility in xerogel (C_e). The surface region is only up to several atomic diameters thick and is bounded only on one side. Therefore, we take it to be $w = 5$–20 Å in our calculations. The usual particle size for silica gels obtained by the two-step acid–base catalysis, and therefore the wall thickness, is between 5 and 40 nm. We estimate $2.5\,\text{nm} < H < 20\,\text{nm}$ for our samples, and we take $H = 10$ nm in most of the calculations.

The bulk diffusivity of Cu in xerogel can be estimated from RBS data [177], and literature data for SiO_2 and glass [200]. An upper limit of Cu diffusivity based on RBS observations is $10^{-15}\,\text{cm}^2/\text{s}$. The solubility of Cu in xerogel at 650°C is about 1×10^{20} atoms per cm^3 of solid silica. The reported literature values for Cu diffusivity through SiO_2 and 4% PSG glass at 300°C range from 10^{-20} to $10^{-15}\,\text{cm}^2/\text{s}$ [200, 212–213]. The activation energy range is 0.5–1.2 eV.

We do not have data for surface diffusivity of Cu on SiO_2. We can argue that due to the larger extent of defects near the surface, such as broken bonds and local disorder (open volume), we can expect D_s to be larger than D_b. It has been proposed that the activation energy for surface diffusion for tungsten is about half of that for bulk diffusion [214] for this reason. In the absence of data, we explore a range of possible D_s. Finally, we have to estimate the interfacial (equilibrium) concentration of Cu in xerogel. Earlier SIMS analysis of Cu/SiO_2 samples subjected to the BTS test at 250°C for 3.5 and 42 h [200] revealed Cu interfacial concentration in excess of 10^{20} per cm^3. In a more recent study [215], concentrations of 10^{18} per cm^3 are reported. In this analysis, we choose $c_e = 10^{20}\,\text{cm}^{-3}$.

Where not noted otherwise, the calculations are done for ($T = 300$°C, $E = 1$ MeV/cm, $D_b = 10^{-15}\,\text{cm}^2/\text{s}$, $H = 10$ nm, $w = 5$ Å, $c_e = 10^{20}$ per cm^3, $L = 1$ μm, and $\varepsilon = 0.4$). With these parameter values, we can expect the following ionic current density (neglecting the surface transfer):

$$J_b = \left(\frac{D_b q}{kT}\right) E c_e (1 - \varepsilon) = 2 \times 10^{-7}\,\text{A/cm}^2 \tag{25}$$

We typically measured $\sim 10^{-7}\,\text{A/cm}^2$ at 300°C, so the assumed parameters are also consistent with our experimental findings.

Equations (17) and (18) and the associated boundary conditions can be written in dimensionless form, in order to yield the minimum number of model parameters. Thus, one can get four essential model parameters: $Pe = \mu_b EL/D_b$, D_s/D_b, L/H, and H/w. Pe is the equivalent of the Peclet number in the chemical engineering literature, because the $\mu_b E$ term represents the drift velocity.

Before showing the results of the numerical calculations, it is useful to do an order of magnitude estimate of time scales for different mass transport processes in xerogel network. There are two limiting cases: negligible surface diffusion and very fast surface diffusion. We begin our analysis by studying these simple cases first.

For negligible surface diffusion, Eq. (17) becomes one-dimensional (no mass transfer in *y*-direction). This equation is then analogous to the transient one-dimensional diffusion-convection equation. The usual criterion for relative contribution of convective to diffusive mass transfer in this case (in steady state) is the Peclet number: $Pe = vL/D$, where v is the convective (drift) velocity, L is the length scale, and D is the diffusivity. In our case, $\mu_b E$ can be written as v_b, bulk drift velocity, and for $T = 300°C$, $L = 1\,\mu m$ and $E = 1\,MV/cm$, we get

$$Pe = \frac{v_b L}{D_b} = \frac{2LE}{kT} \approx 2000 \tag{26}$$

For large enough time scales, molecular diffusion is negligible compared to the electric-field-induced drift. Based on this result, we can estimate the time necessary for the Cu ions to traverse the 1 μm thick film as:

$$\tau_E \approx \frac{L}{v_b} = \frac{LkT}{eD_b E} = 1\,hr\,20\,min \tag{27}$$

In the absence of the electric field, Cu is transported only by molecular diffusion. The time necessary to traverse the film in this case is approximately

$$\tau_b \approx \frac{L^2}{D_b} \approx 115\,days \tag{28}$$

Obviously, the electric field enhances the transport of Cu significantly. In contrast, in the case of fast surface diffusion, the time scale for the diffusion from the surface into the bulk of xerogel (in the *y*-direction), assuming $H = 10\,nm$, is

$$\tau_{sb} \approx \frac{H^2}{D_b} \approx 16\,min \tag{29}$$

These results tell us that surface-bulk transfer in the *y*-direction can be very fast compared to the processes in *x*-direction, and cannot be neglected.

The effect of faster surface diffusion is to enable *y*-direction diffusion to supply Cu to the bulk of the xerogel, where it is transported predominantly by drift. In effect, the concentration gradient in the *x*-direction is reduced and the profile is smoothed. The most important result of the model simulation is the Cu^+ current at the anode, $x = 0$. Once we have the concentration profile for Cu^+, we can calculate the current using Eqs (21)–(24). The slope of the concentration profile at $x = 0$ is used to represent the concentration derivatives at $x = 0$. The numerical results, shown in Figs 9.39 and 9.40 show that due to the high concentration gradient at small times at the Cu/xerogel interface, the *I–t* curves exhibit decreasing current, which stabilizes after a few minutes. The decrease is very small (~10%) for high values of *Pe* number, as shown in Fig. 9.39 for $Pe = 2000$. As the electric field, and thereby *Pe* number, is decreased, as shown in Fig. 9.40, the initial current decrease becomes more significant (up to 70% for $E = 0.01\,MV/cm$). Therefore,

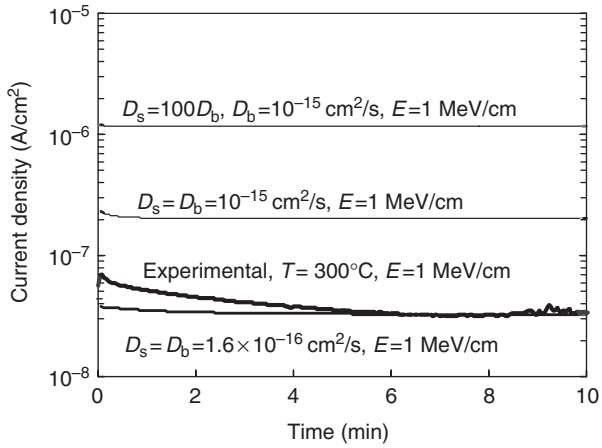

Fig. 9.39 Anode currents as a function of increasing surface diffusivity [177, 205] ($Pe = 2000$) (reprinted with permission).

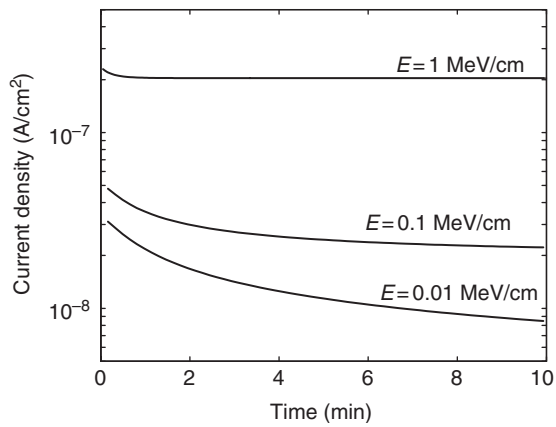

Fig. 9.40 Effect of electric field strength on the anode current for the system [177, 205] (reprinted with permission).

we conclude that the trend of decreasing current that we observed for all our samples, as described in Section 9.6.3, also could be caused by the initially high diffusion rates of ions through the dielectric. Figure 9.41 shows the effect of surface diffusion: higher surface diffusion causes significantly higher Cu^+ current at the anode, and moves the *I–t* curve parallel to the *x*-axis, without changing the slope. Our experimental data for Cu/xerogel samples can be modeled well by taking $D_b = 1.6 \times 10^{-16}\,cm^2/s$, and $D_s = D_b$ as shown in Fig. 9.42.

According to the model, Cu^+ flux at the cathode, $x = L$, shows a time lag in the amount of time necessary for the ions to traverse the dielectric. The ionic flux then increases rapidly, and reaches the value of the current at the anode, as shown in Fig. 9.41. If the Cu^+ current at the

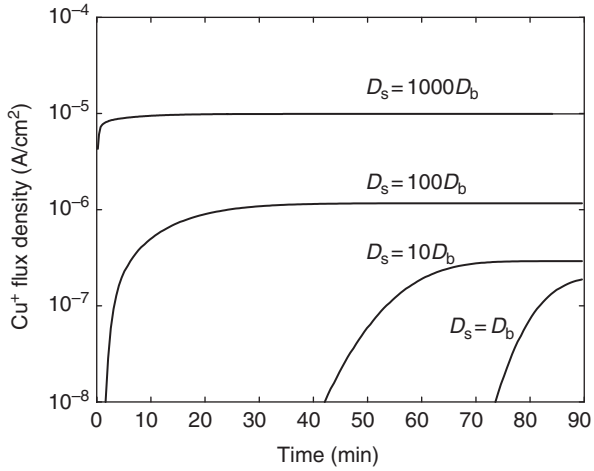

Fig. 9.41 Cu^+ current flux at the cathode ($x = L$) showing breakthrough behavior ($Pe = 2000$) [177, 195] (reprinted with permission).

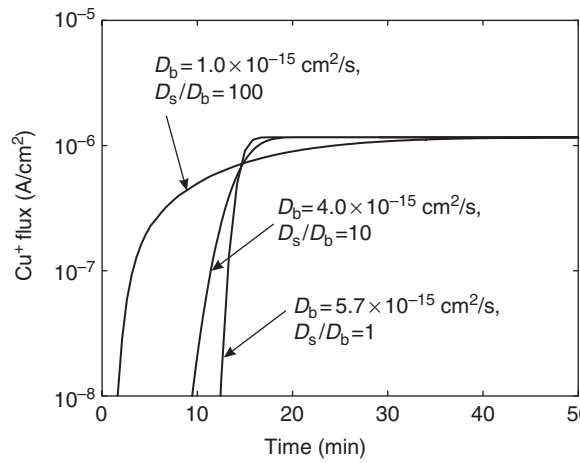

Fig. 9.42 Approach to steady-state of the cathode Cu^+ current flux ($Pe = 2000$) [177, 205] (reprinted with permission).

cathode determines the useful lifetime of the dielectric, the time lag of the ion flux at the cathode should correlate with the time to failure of a capacitor. Also, the area below the *I–t* curve (charge injected in the substrate) correlates with the amount of undesirable Cu diffusion into the substrate, and therefore the extent of degradation of the device. Consequently, time to failure experiments would be useful to confirm the validity of the model. Figure 9.41 shows that the effect of the increasing surface diffusion is to increase the current (for constant D_b), but also

to determine the time lag of the Cu^+ current, and the rate of approach to the steady-state level. For $D_s/D_b = 1$, the current–time curve is almost a sharp step. Figure 9.42 shows that even though the same steady-state level of current can be achieved for various combinations of D_s and D_b, the rate of approach is unique for each D_s/D_b ratio. Therefore, we conclude that the magnitude of surface diffusivity plays an important role in determining the useful lifetime of the dielectric.

9.5 Conclusions

Porous materials have been proposed to replace SiO_2 as the interlayer dielectric in future microelectronic devices. Any new low-κ material has to pass an array of electrical, mechanical, thermal, and chemical tests before it is deemed a potential replacement for dense SiO_2. The properties of any porous material depend upon the material's microstructure and its process history. Thus, meeting industry standards at one porosity does not guarantee meeting them as higher porosity versions of the material become necessary to meet roadmap requirements. In this chapter, we have explored a range of low-κ materials focusing on nanoporous silica xerogels as a benchmark.

- We showed that for a fully connected material like sintered silica xerogels, the elastic modulus should vary with the square of the density and the thermal conductivity, like the dielectric constant, should vary linearly with density. Any defects in the structure of the material tend to increase the dependence of the property of interest on the density or equivalently, porosity of the material. Property measurements are also dependent upon the method used in the measurement process. There is considerable debate about the relative accuracies of the surface acoustic wave and nanoindentation methods for obtaining the elastic modulus of a material. We showed that how the measurement process of the sample material determines whether the material's property depends linearly or nonlinearly on the density of the material. If the sampling occurs at wavelengths larger than the pore size or larger than the film thickness, the property varies linearly with the overall measure of porosity.
- Interactions between the dielectric and adjacent metal or barrier layers are also critically important to the performance of an interconnect. We showed how the measurement of adhesion and stability of adjacent layers depend upon the porosity of the material and the intermolecular forces governing the strength of the Van der Waals interaction between the layers. Adhesion also depends upon intrinsic stresses in the layers and whether the ambient environment is inert or reactive.
- Using silica xerogel as the test material, neither copper nor tantalum, the latter a potential diffusion barrier for copper, diffuse into the porous material via a thermal activation process alone. A 500-Å Si_3N_4 layer between the metal and the environment while retaining the metal/xerogel interface is found to prevent the oxidation and diffusion of Ta and Cu at temperatures up to 640°C (when the samples are annealed in the ambient with nitrogen purge).

The stability and adhesion of a tantalum layer depend upon the porosity of the material and the environment. The presence of even trace amounts of oxygen (about 5×10^{-8} mol/m^3 of O_2) in the ambient environment at temperatures higher than 450°C make that environment reactive and cause oxidation and buckling of Ta thin films. Cu tends to dewet and form islands on solid SiO_2 surfaces due to poor wetting (high interfacial energy). In contrast, when Cu was deposited on xerogels, holes and hillocks are formed in the Cu film, which may indicate an initial stage of dewetting that occurs only at substantially higher annealing temperatures than those that cause dewetting on solid SiO_2. Thus, Cu films appear to be more stable on xerogel surfaces even at high porosities (70%).

- Under an electrical bias, the leakage current of xerogel capacitors is, unexpectedly, lower with a Cu electrode than with an Al electrode. This observation is fundamentally different from tests using dense SiO_2 as the interlayer dielectric. The chemical reaction of the surface capping agent, trimethylchlorosilane (TMCS), with Cu could be responsible for lower electron–hole injection and prevent Cu ion migration. In the absence of surface modification with TMCS, small amount of moisture adsorption causes increased leakage current in xerogel-based capacitors. This can occur in sintered xerogel, from which the organic capping groups are removed, and not replaced to maintain the xerogel's hydrophobicity.
- *C–V* tests indicated Cu diffusion into sintered xerogels at 100°C. When 1 MV/cm field was applied at 100 and 150°C to Al/xerogel and Cu/xerogel capacitors, respectively, significant positive charge accumulation (a negative *C–V* shift) occurs. Similar behavior was observed for metal/polymer contacts. This indicates that although the matrix of our material is silica-based, its electrical behavior could be determined by surface chemistry and so the surface chemistry of porous materials will have strong effect on its electrical behavior and any interdiffusion interactions that may occur.
- A model for the diffusion of metals through porous solids was developed, which takes into account two different transfer paths: through the bulk and along the surface of the solid network. The model considers three driving forces of mass transfer: concentration gradient (causes molecular diffusion), electric field (drift), and curvature gradient (wetting). The most important result of the model calculations is the current density. The model shows good agreement with the experimentally measured anode current in Cu/xerogel samples subjected to bias-temperature stress.
- Of all current low-κ materials tested, fully interconnected, nanoporous silica-based materials appear to have the best mechanical and thermal properties. At the same dielectric constant, such materials exhibit elastic moduli and thermal conductivities that exceed dense polymeric materials by an order of magnitude and surpass hybrid materials by nearly that amount as well. The fracture toughness of these materials is also comparable to porous polymeric materials such as SiLK^{TM}. It remains to be seen which material property will govern whether a given low-κ dielectric is commercially viable in future generations of microprocessors.

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Chapter 10
High-*k* dielectrics grown by atomic layer deposition: capacitor and gate applications

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Abstract

The dramatic improvements in microelectronics performance over that past few decades have been accompanied by a severe reduction in the size of memory and logic devices. This scaling has required drastic decreases of the SiO_2 dielectric film thickness to achieve ever-higher capacitance densities. Fundamental limits of SiO_2 as a dielectric material, imposed by electron tunneling, will be reached as this SiO_2 film thickness approaches ~1 nm. By 2005, an as yet undetermined alternate high-*k* interlayer dielectric material will be needed to replace SiO_2 as a capacitor and gate dielectric material. Numerous alternate high-*k* materials are being actively investigated, ranging from Al_2O_3 ($k \sim 9$) to perovskites ($k \sim 10^2$–10^4). High-*k* materials hold the promise of achieving very high capacitance densities with relatively thick films. These thicker films should preclude the excessive tunneling currents observed for very thin SiO_2 films. However, finding a high-*k* material is a major challenge because the high-*k* material must have a high resistivity, act as a good barrier layer, be thermally stable, and form an ideal interface with silicon. SiO_2 films can be conveniently formed via oxidation of the silicon substrate. In contrast, alternate high-*k* materials must be formed by deposition. Atomic layer deposition (ALD) has emerged as a very promising technique for depositing alternate high-*k* thin films for the microelectronics industry. ALD can deposit films with atomic layer thickness control and conformally coat high aspect ratio structures. Most high-*k* dielectric materials have been successfully deposited by ALD. ALD is also very well suited for depositing various types of composites that combine the desirable properties of different materials.

10.1 Introduction

The semiconductor microelectronics industry requires interlayer dielectric films for a variety of applications. Dielectric layers are needed as gates in MOSFETs, as capacitors to store charge in memory devices, and as insulation in back-end interconnects. SiO_2 has been the dielectric

material of choice for all of these applications. SiO_2 is a dielectric material with very low leakage currents, acts as a good diffusion barrier for dopants and ionic contaminants, and forms a well-defined interface with silicon.

The continued drive towards faster processors has required the progressive shrinking of microelectronics devices [1]. The decrease in device feature size allows for increased speed, lower power consumption, and lower cost because of the increased density of devices per wafer. This size reduction presents challenges for the various SiO_2 applications. The insulation of interconnects requires lower dielectric constant materials. Applications such as capacitors and gate dielectrics require higher dielectric constant materials.

Decreasing the thickness of the SiO_2 dielectric film achieves the goal of increasing the capacitance to offset the decrease in the surface area of the capacitor. However, SiO_2 films will soon need to be so thin that tunneling through the film will become significant and will increase power consumption to unacceptable levels. High-k materials are needed to replace SiO_2 in these applications to achieve high capacitances while keeping the leakage currents low.

A wide range of materials has been proposed as alternate high-k dielectrics. The dielectric constants of these high-k materials range from $k < 10$ to $k > 10\,000$ [1–4]. Some of these materials, such as Al_2O_3, Ta_2O_5, and $SrTiO_3$ are already being used commercially for capacitor memory devices [1]. For the more demanding gate dielectric application in field effect transistors (FETs), the search for a suitable high-k dielectric material continues to be a challenge. To replace SiO_2 as the gate dielectric, the high-k material must also have a high resistivity, act as a good barrier layer, and be compatible with other materials and processes used in the microelectronics industry.

A wide range of techniques have been employed for depositing high-k material films [1, 3]. However, only a few of these deposition techniques are compatible with microelectronics processing. These techniques include chemical vapor deposition (CVD) and physical vapor deposition (PVD). This review will focus on a promising CVD-derived technique called atomic layer deposition (ALD) [5–7]. ALD is the only vacuum compatible deposition technique that allows for atomic layer thickness control and has the ability to coat conformally high aspect ratio trenches and three-dimensional (3D) structures. Furthermore, ALD is well-suited for making mixed materials and nanolaminates. Such composite materials have shown promise because the desirable characteristics of different materials can be tuned to achieve optimum properties.

For a detailed review of high-k materials as gate dielectrics, the reader is referred to a recent excellent review article [1]. Various books have also discussed in more detail the synthesis of high-k dielectrics [3] and the properties and applications of high-k dielectrics [8]. This chapter focuses on the high-k dielectrics that can be grown by ALD and will emphasize high-k materials that are important for capacitor and gate applications.

10.2 Limitations of SiO_2 as a dielectric

SiO_2 has served as the dielectric material for silicon-based microelectronic applications for the past three decades. SiO_2 has excellent dielectric properties, including a very high resistivity

of ~$10^{18}\,\Omega$cm and a large bandgap of ~9 eV. Furthermore, the ability to grow high quality, amorphous SiO_2 dielectric films by the oxidation of the silicon substrate is very convenient for process integration. With so much research and infrastructure invested in SiO_2 technology, finding a material to replace SiO_2 has proven to be a great challenge.

The ability to make reliable, ultra-thin SiO_2 layers has advanced greatly in recent years. In 2001, SiO_2 thicknesses on the order of ~2 nm were used in devices. Various studies have explored the minimum SiO_2 film thickness that still retains the bulk properties of SiO_2 [1]. Based on calculations and experimental results, the absolute lower limit for a SiO_2 film thickness is 7 Å. Below this thickness, the material no longer has the SiO_2 bulk bandgap of 9 eV. A further limitation for practical device applications of SiO_2 is the large tunneling current that can leak through such thin films.

A more practical limit of 10–12 Å has been established based on the maximum allowable tunneling current [1]. Transistors with SiO_2 film thicknesses of 10–12 Å can be used in FETs despite the high leakage current densities of 1–10 A/cm^2. Whether or not these 10–12 Å films will be economically feasible will depend on questions about ultrathin oxide reliability and contamination issues [1]. However, even if these optimistic predictions regarding ultrathin SiO_2 layers are realized, alternate high-*k* dielectric materials will be required by 2005 according to the International Technology Roadmap for Semiconductors [9].

Another way to extend the use of SiO_2-based dielectrics has been through the incorporation of nitrogen into SiO_2. Oxynitrides (SiO_xN_y) can achieve dielectric constants of $k \sim 6$, compared to $k = 3.9$ for SiO_2 [2]. Although oxynitrides offer only a small increase in the dielectric constant, they are much more compatible with existing processing technologies than other high-*k* dielectric materials. Oxynitrides have been used as dielectrics in memory devices and are currently being implemented in logic devices [1, 2]. By 2005, however, the equivalent oxide thickness requirements for high-performance devices, as well as for low stand-by power logic devices, can no longer be met by SiO_2, oxynitrides, or any other currently known technology solution. At this date, the need for alternate high-*k* dielectrics becomes critical.

10.3 Desired high-*k* material properties

10.3.1 Requirements for capacitor and gate applications

Memory capacitor and gate applications both need alternate high-*k* dielectrics to achieve higher capacitance densities. However, the requirements for memory capacitor and gate applications are different [1]. Capacitors for memory need very low leakage currents on the order of 10^{-8} A/cm^2. This requirement allows the charge stored in the capacitor to remain large enough to be read for a relatively long time period, typically ~250 ms [2]. In contrast, the nature of the high-*k*/electrode interface is not that critical, provided that the interface does not reduce the capacitance significantly. Metal or highly doped nitrided poly-Si may be used as the electrodes.

Gate dielectrics in FETs can have a much higher leakage current, but the quality of the high-*k*/Si bottom electrode interfacial region is critical [1]. Current densities as high as 1–10 A/cm^2 are acceptable for some processors. Certain low power applications, such as portable devices, demand leakage currents of $< 10^{-3}$ A/cm^2. These leakage current levels are still much less stringent than the requirements for memory capacitors. More important to the performance of an FET is the electric field that penetrates into the silicon channel. Interfacial layers and interface roughness adversely affect the strength and uniformity of this electric field and degrade FET performance [1].

10.3.2 Electrical properties

In addition to having a large dielectric constant, alternate high-*k* dielectrics should have a low leakage current, low loss factor, high breakdown voltage, and a large barrier height when in contact with Si. Unfortunately, high-*k* materials often do not exhibit these properties [1]. Optimizing the properties of alternative high-*k* dielectrics requires an examination of the various factors that influence the dielectric constant and leakage current.

The dielectric constant is determined by the polarizability of the dielectric material. The polarizability is dependant on a number of factors including the density of electrons in the material, the crystal structure, and dopants [1]. For example, transition metal oxides typically have higher dielectric constants than the oxides of lighter elements like Si and Al. There is often a wide range of published dielectric constants listed for a given material. This variability can be attributed, in part, to whether a material is amorphous or crystalline, the type of crystal structure, and the average crystalline grain size.

The dielectric constant of γ-Al_2O_3 is slightly higher than the dielectric constant of amorphous Al_2O_3. This larger dielectric constant is partially explained by the higher density of γ-Al_2O_3. For TiO_2, dielectric constant values ranging from 50 to 110 have been reported [1, 3, 4], with the rutile TiO_2 phase having higher *k* values than the anatase TiO_2 phase. In $BaTiO_3$, grain size has been shown to affect significantly the dielectric constant [8]. The dielectric constant peaks at $k > 5000$ for $BaTiO_3$ with an average grain diameter of ~1 μm. Much smaller or larger grain sizes have $k < 2000$.

The deposition methods and the deposition conditions tend to determine the crystallinity and purity of a deposited dielectric film. High temperature annealing can result in the crystallization and densification of a dielectric material. This densification often increases the dielectric constant. Impurities are generally expected to lead to a decrease in the dielectric constant. However, the intentional doping of high-*k* perovskites has resulted in some very high dielectric constant values [3].

The dielectric relaxation losses of a dielectric material can have detrimental effects on the performance of memory and logic devices. This well-known, but poorly understood, phenomenon has the effect of adding *RC* shunts with varying time constants in parallel to the dielectric

capacitor [10]. While these losses are small for most AC power applications, they may be unacceptably large for memory and logic devices where read and write times are on the nanosecond time scale. The dielectric losses have been studied for some alternative high-*k* dielectrics [10]. HfO_2 was found to have a much higher dielectric loss than Al_2O_3, Ta_2O_5, $BaSrTiO_3$ (BST), and Y_2O_3. Furthermore, the dielectric losses of all of these materials were at least an order of magnitude higher than the dielectric loss for SiO_2.

High leakage currents are a major problem for memory capacitor applications. Amorphous SiO_2 has one of the highest resistivities of any material at ~$10^{18}\,\Omega\,cm$. Some alternate high-*k* materials, such as Al_2O_3, come close to the resistivity of SiO_2. Other high-*k* materials tend have much lower resistivities. The measured resistivity of a dielectric material is not an intrinsic property of the material. Rather, the resistivity can be controlled by the purity, stoichiometry and crystallinity of the material.

Impurities can create defect sites or act as mobile ions. Small deviations from ideal stoichiometry can effectively dope a material, such as TiO_2, and result in a dielectric becoming highly conductive [11]. Grain boundaries in polycrystalline materials also tend to increase conductivity [1, 2]. Crystallization of amorphous films through annealing can lead to increased leakage currents. Unfortunately, most alternate high-*k* material candidates, except for Al_2O_3, crystallize during typical processing conditions.

A large barrier height at the electrode/high-*k* dielectric interface is important because this barrier height minimizes the leakage current. The barrier height at a Si/SiO_2 interface is ~3.5 eV. However, the barrier heights and the bandgaps of high-*k* materials in contact with silicon tend to decrease with increasing dielectric constant [1, 12]. Some of the promising high-*k* materials, such as Ta_2O_5 and $BaTiO_3$, have calculated barrier heights < 0.5 eV. These low barrier heights may lead to unacceptably large leakage currents.

10.3.3 Interfacial layers

The nature of the interface between a high-*k* dielectric and an electrode plays an important role in determining whether a high-*k* material can be suitable for a certain application [1, 2]. Interfacial layers are sometimes intentionally inserted to passivate the surface, prevent diffusion, or promote adhesion. However, most interfacial layers that form spontaneously during deposition of the high-*k* material are detrimental to device performance.

Interfacial layers can severely decrease the capacitance of a high-*k* film. In FETs, these interfacial layers can limit the field penetration into the silicon channel. Interfacial oxide layers can be formed if the substrate reacts: (a) with the oxide precursors used to make the high-*k* film; (b) with the oxygen in the high-*k* film itself; and/or (c) with oxygen species that diffuse through the high-*k* film. Although some high-*k* materials are predicted to be stable in contact with silicon, nonequilibrium conditions are generally present during the deposition of these materials. On a silicon substrate, the interfacial layer formed tends to be SiO_2 or a silicate/high-*k* mixture.

Regardless of what kind of interfacial layer is formed, the overall capacitance that can be achieved with an interfacial layer/high-k stack will be lower than the capacitance of the high-k film alone. The capacitance of two capacitors in series is determined by $C_{\text{total}}^{-1} = {C_1}^{-1} + {C_2}^{-1}$. The capacitance is $C = k\varepsilon_0 A/d$, where k is the dielectric constant, ε_0 is the permittivity of free space ($\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm), A the area, and d the dielectric thickness. Let us assume that a 1 nm thick SiO_2 layer with $k = 3.9$ and $A = 0.0001\ \text{cm}^2$ is formed under a 5 nm thick high-k material with $k = 50$ and $A = 0.0001\ \text{cm}^2$. The capacitance of the SiO_2 layer is C = 0.35 nF. The capacitance of the high-k layer is C = 0.89 nF. The resulting total capacitance is only 0.25 nF.

Another way to see this effect is to consider the equivalent oxide thickness (EOT). The EOT is the thickness of SiO_2 with $k = 3.9$ that would equal the capacitance of the high-k material. The high-k material with $k = 50$ and a thickness of 5 nm would have an EOT of only 0.39 nm. The total EOT of the stack, including the SiO_2 interfacial layer, is much higher and can be given by:

$$\text{EOT} = \frac{k(\text{SiO}_2)}{k(\text{high } k)} \times d(\text{high } k) + d(\text{SiO}_2)$$

The EOT of the stack, including the SiO_2 interfacial layer, is EOT = 1.39 nm. The capacitance of this film is not nearly as high as the original expectations. However, this stack should still have a lower leakage current than a 1.39 nm thick SiO_2 layer.

10.3.4 Processing issues

The processing of devices after depositing the high-k material typically involves annealing to high temperatures of ~1000°C. High temperature annealing can lead to a number of problems [1, 2]. Many high-k materials crystallize at these high temperatures. Crystallization tends to result in higher leakage currents. In addition, mixed materials may phase segregate at higher temperatures. The high temperatures can also accelerate the diffusion of cations into and through high-k materials. This diffusion can degrade the dielectric and the material below the dielectric. Oxygen diffusion, especially at high temperatures, is also a known problem for high-k materials. Oxygen diffusion can result in increased interfacial SiO_2 growth.

10.4 Thin film deposition techniques for high-k materials

Thin films of high-k materials have been deposited by a number of methods. Techniques include CVD, reactive sputtering, physical vapor deposition (PVD), molecular beam epitaxy (MBE), sol–gel methods, and hydrothermal and electrochemical syntheses [3]. Only a few of these methods are compatible with the stringent requirements for microelectronics fabrication processes. CVD is perhaps the most well-known technique for the deposition of high-k thin films. During CVD, gas phase precursors are introduced into a vacuum chamber, where they react and deposit a film on the substrate.

Most high-*k* films in the microelectronics industry are presently deposited by CVD and CVD-derived techniques [13]. High-*k* Ta_2O_5 films have replaced oxynitride films for current use in DRAM fabrication [2]. $BaSrTiO_3$ (BST) has also been investigated for use in memory devices, although a MIM structure, instead of the conventional MIS structure, may be required to avoid interfacial oxides. Ferroelectric random access memory (FeRAM) devices have been developed using $Pb(Zr,Ti)O_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT) dielectrics and are expected to replace DRAM devices [14]. For high-*k* gate applications, HfO_2 films deposited by CVD are promising. Many other films have been investigated for high-*k* gate dielectrics [1, 13].

Other methods that have been successfully employed for depositing high-*k* dielectric materials include MBE and PVD [1, 13]. Recently, HfSiON films deposited by PVD exhibited very good dielectric properties [15]. MBE was used to deposit $SrTiO_3$ films with an EOT < 10 Å [1]. However, PVD and MBE do have some significant problems. PVD suffers from problems with sputtering damage and is a line-of-sight technique. MBE has an inherently slow throughput [1].

For future deposition of ultra-thin high-*k* materials, the need to deposit conformal films with precise thickness control becomes much more critical. ALD is a CVD-derived thin film deposition technique that appears to be the most promising technique for the deposition of ultrathin films of high-*k* materials for future microelectronics applications [1, 13]. ALD is based on the application of sequential, self-limiting surface reactions [5]. ALD may be considered a type of CVD where the gas phase precursors are introduced alternately instead of simultaneously.

A cartoon illustrating the sequential, self-limiting surface reactions that define ALD is shown in Fig. 10.1. Two sequential surface reactions, A and B, produce the ALD thin film growth. Because there are only a finite number of chemical species on the surface, both reactions are self-limiting. The chemical species are exchanged during each surface reaction. In the A reaction, the gas phase precursor reacts with the chemical species left by the B reaction. In the B reaction, the gas phase precursor reacts with the chemical species left by the A reaction. ALD is achieved by repeating the surface reactions in an ABAB … sequence.

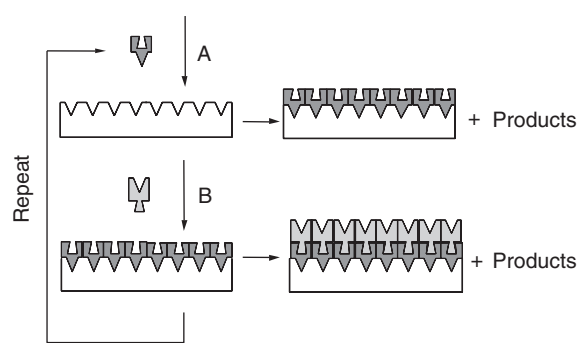

Fig. 10.1 Two sequential, self-limiting surface reactions that define ALD.

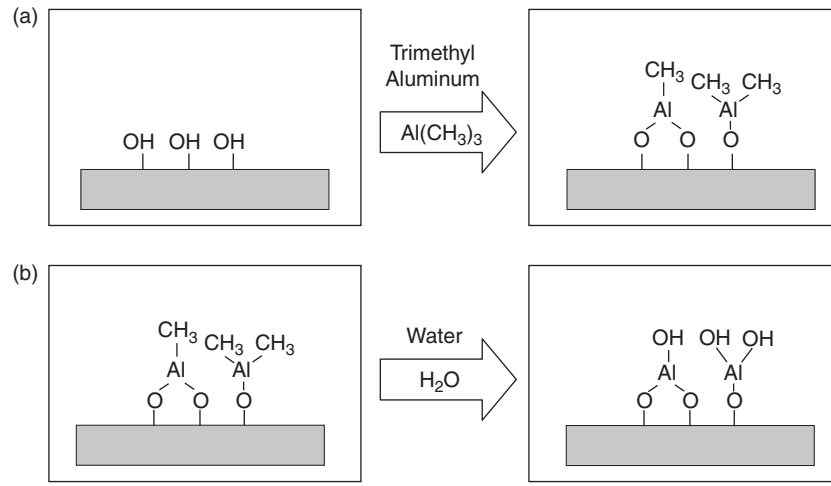

Fig. 10.2 Illustration of the two, sequential, self-limiting surface reactions that define Al_2O_3 ALD.

Al_2O_3 ALD can be used to describe ALD thin film growth. Al_2O_3 ALD is based on the CVD reaction: $2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4$. To achieve Al_2O_3 ALD, this binary CVD reaction can be divided into two separate reactions [16, 17]:

$$AlOH^* + Al(CH_3)_3 \rightarrow AlOAl(CH_3)_2^* + CH_4 \quad (A)$$

$$AlCH_3^* + H_2O \rightarrow AlOH^* + CH_4 \quad (B)$$

where the asterisks designate the surface species. These two separate surface reactions are defined in Fig. 10.2.

During Al_2O_3 ALD film growth, $Al(CH_3)_3$, the gas phase precursor in the A reaction, reacts with hydroxyl groups on the substrate until this surface reaction reaches completion. Subsequently, $Al(CH_3)_3$ is pumped or carried away. The same process is then repeated with H_2O, the gas phase precursor in the B reaction. This procedure completes one AB cycle that deposits approximately one monolayer of Al_2O_3.

These AB cycles are repeated to achieve the desired Al_2O_3 film thickness. The Al_2O_3 ALD growth rate is extremely linear with number of AB cycles. Figure 10.3 shows the linear growth during Al_2O_3 ALD measured using both ellipsometry and stylus profilometer measurements. The Al_2O_3 ALD growth rate is ~1.2 Å per AB cycle at a growth temperature of 177°C [17]. The Al_2O_3 ALD films are also extremely flat and conformal to the underlying substrate. Previous atomic force microscope measurements have confirmed that the surface roughness is only nominally larger than the original underlying substrate [17]. The surface roughness remains nearly constant versus number of AB cycles [17, 18].

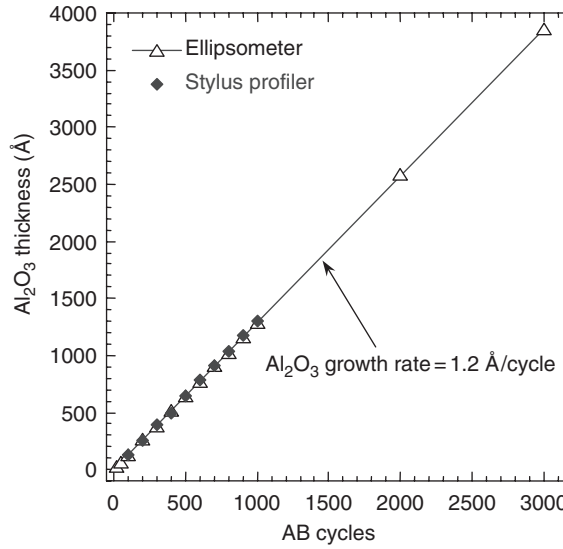

Fig. 10.3 Al_2O_3 ALD film thickness versus AB cycles showing linear growth during Al_2O_3 ALD. The Al_2O_3 ALD film thickness was measured using ellipsometry and stylus profilometry.

ALD is the only technique that combines the ability to grow thin films with atomic layer thickness control with the ability to coat conformally complex 3D structures. Conformality is achieved because the surface reactions are self-limiting [5]. For example, reactions may occur initially and reach completion at the opening of a trench. After this surface area reacts, the gas phase precursors can progressively reach surface area further down in the trench. As a function of reaction time, the reactants can eventually reach the surface area at the bottom of the trench. The chemical species at the bottom of the trench will react until the reaction reaches completion. Conformality is achieved because the maximum deposition is defined only by the surface density of chemical species.

Since the two reactants are present individually in the reaction chamber, ALD also avoids the gas phase particle generation problems associated with CVD. The deposition of these gas phase particles often leads to very granular depositions during CVD. The roughness of the ALD films is also extremely low, particularly for amorphous ALD films such as Al_2O_3 [18]. Because the surface reactions reach completion during each A and B reaction, there is negligible statistical randomness to the ALD growth process. ALD films are generally extremely continuous and pinhole-free. This characteristic is important for the application of ALD films as dielectric insulators. Moreover, deposition temperatures for ALD are generally lower than the temperatures required for CVD.

ALD has been used to deposit numerous high-*k* materials that could be used to replace SiO_2 in memory and gate dielectric applications. Al_2O_3 films grown by ALD are already being used as capacitors in DRAMs by Samsung [19, 20]. For this application, the low processing

temperature and the ability of ALD to coat uniformly intricate 3D structures was important. Several commercial ALD reactors are available, including those by ASM Microchemistry [21] and by Genus [22]. Many more companies are currently investing in ALD technology and more vendors will be providing products in the near future.

10.5 High-*k* dielectric materials

10.5.1 Binary oxides grown by ALD

Most of the known binary metal oxide high-*k* materials have been grown by ALD. These binary metal oxide materials include, approximately in order of increasing dielectric constant, Al_2O_3, Y_2O_3, CeO_2, HfO_2, ZrO_2, Ta_2O_5, TiO_2, La_2O_3, and Nb_2O_5. The dielectric constants of these thin films grown by ALD range from $k < 10$ to $k > 100$. These dielectric constants are comparable with the dielectric constants measured for the same materials grown by other methods.

10.5.1.1 Al_2O_3

Al_2O_3 is the most widely studied high-*k* material grown by ALD. Al_2O_3 films grown by ALD are already used in DRAMs [19, 20]. Al_2O_3 films can be deposited rapidly by ALD. AB cycle times on the order of a second can be achieved in commercial reactors [22]. Furthermore, a variety of precursors can be used to grow Al_2O_3 by ALD [6].

Al_2O_3 exhibits excellent insulating properties. These favorable properties result from the large Al_2O_3 bandgap of 9 eV and the large barrier height of 2.8 eV when in contact with silicon [12]. Recent electrical investigations have measured the current–voltage (*IV*) and capacitance–voltage (*CV*) characteristics for Al_2O_3 ALD films on Si(100) [23]. The *IV* plots are excellent and display a very low leakage density on the order of ~1 nA/cm^2. Various *IV* curves for Al_2O_3 ALD films of different thickness on Si(100) are shown in Fig. 10.4. These *IV* curves display behavior that is characteristic of Fowler–Nordheim tunneling.

Al_2O_3 is thermodynamically stable on silicon. However, SiO_2 or aluminum silicate layers are often formed at the Al_2O_3/SiO_2 interface. These interfacial SiO_2 layers appear to be inevitable, in part, because growth often does not occur under equilibrium conditions [1]. The interfacial SiO_2 layer will seriously compromise the dielectric constant that can be obtained from gate stacks. The dielectric constants for Al_2O_3 ALD films of various thickness on Si(100) are shown in Fig. 10.5. The reduction of the dielectric constant for thinner Al_2O_3 ALD film thicknesses is attributed to an interfacial SiO_2 layer with a thickness of ~10–12 Å [23]. The calculations in Fig. 10.5 show the predicted behavior for a SiO_2 interfacial layer of 11 Å including quantum mechanical corrections.

Al_2O_3 ALD films hold promise for memory and gate dielectric applications. For memory applications, the interfacial SiO_2 problem can be avoided by using non-silicon electrodes.

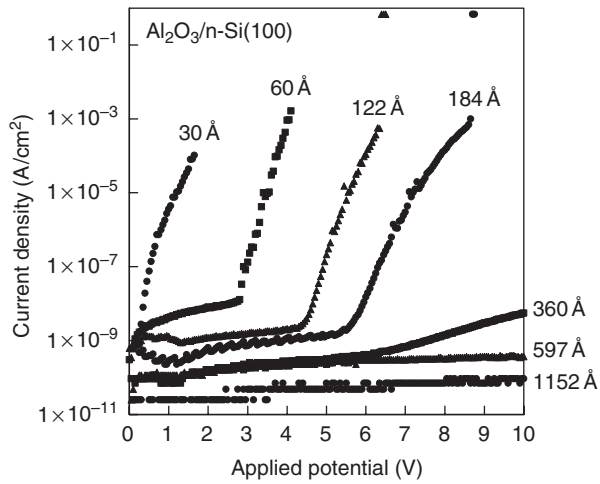

Fig. 10.4 Current–voltage (*IV*) plots for Al_2O_3 ALD films of different thicknesses grown on n-Si(100) at 177°C.

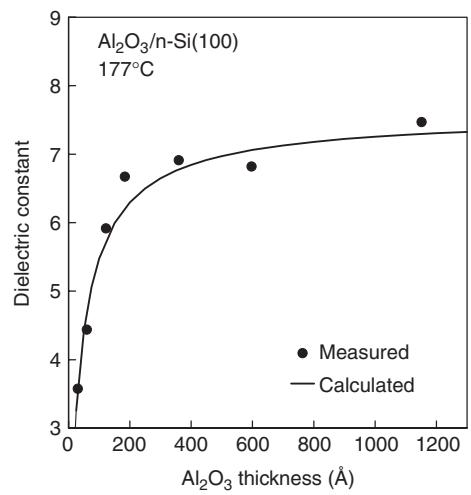

Fig. 10.5 Comparison of the measured and calculated dielectric constants for Al_2O_3 ALD films of different thicknesses grown on n-Si(100) at 177°C.

However, the interfacial SiO_2 is a serious problem for gate dielectric applications because the gate dielectric must be deposited directly on the silicon channel. Even if the interfacial SiO_2 problem can be minimized or avoided, the relatively low dielectric constant of $k \sim 8$–10 for Al_2O_3 is likely to limit its use to only a couple of generations before needing a dielectric with a higher k.

The earliest dielectric constant reported for Al_2O_3 ALD films was $k = 7.1$ [24]. Others who reported dielectric constants for relatively thick Al_2O_3 ALD films measured $k = 8.4$ [25],

$k = 5.3$ [26], $k = 8.5$ [27], $k = 7$ [28], $k = 8.1$ [29], and $k = 9.8$ [30]. A recent study examined ultra-thin Al_2O_3 ALD films with thicknesses down to 1 nm [31, 32]. Dielectric constants of $k \sim 10$–11 were reported for the Al_2O_3 film. However, an interfacial SiO_2 layer with a thickness of 0.75 nm was present that reduced the overall dielectric constant of the gate stack.

Al_2O_3 ALD is possible not only on silicon but on a variety of substrates including various transition metals, alloys, oxides, and even noble metals [23]. Good electrical properties were measured for Al_2O_3 ALD on most of these substrates. The measured dielectric constant was consistently determined to be $k \sim 8$.

10.5.1.2 Y_2O_3

Dielectric constants ranging from $k = 12$ to $k = 20$ have been reported for Y_2O_3 [1]. However, as often observed for a variety of high-k dielectrics, silicate layers have been observed at the interface with silicon. These silicate layers produced much lower overall dielectric constant values. Y_2O_3 growth has been reported by ALD [32]. Dielectric constants of $k \sim 15$ and low leakage currents were observed for Y_2O_3 ALD films grown using $Y(thd)_3$ and ozone. These films were polycrystalline and had a SiO_x interfacial layer with a thickness of ~1.1 nm. Y_2O_3 ALD growth has also been reported using various beta-diketonate yttrium precursors with ozone at temperatures of 250–375°C [33]. Unfortunately, no electrical measurements were reported in this study.

10.5.1.3 CeO_2

The dielectric constant of CeO_2 has been reported as $k = 20$ [4] and $k = 26$ [34]. CeO_2 ALD growth has been performed using $Ce(thd)_4$ and ozone [35]. A later study compared $Ce(thd)_3$ phen and $Ce(thd)_4$ precursors for CeO_2 ALD films grown at lower temperatures [34]. The CeO_2 ALD films were polycrystalline. The preferred $Ce(thd)_4$ precursor displayed CeO_2 ALD growth from 175–275°C. However, no electrical measurements were reported for these CeO_2 ALD films.

10.5.1.4 HfO_2

HfO_2 ALD growth has been reported using $HfCl_4$ and H_2O precursors [32]. These HfO_2 ALD films displayed a dielectric constant of $k \sim 20$. HRTEM images showed uniform, mostly amorphous HfO_2 films grown on a SiO_2-covered Si substrate. Low leakage currents were measured during the electrical testing. Nucleation problems during HfO_2 ALD were observed on H-passivated silicon surfaces (so-called 'HF-last'). These HfO_2 films also exhibited much higher leakage currents. In addition, a thin interfacial layer seems to be present in the HRTEM images.

Self-aligned n-channel MOSFETs have been fabricated using 3 nm thick HfO_2 gate dielectric films grown by ALD [36]. These transistors exhibited promising results after an anneal at 1000°C. Thin sub-oxides were observed at the interfaces with the poly-Si gate and the Si-substrate. The total stack with a thickness of 4.6 nm had an EOT of 1.7 nm.

10.5.1.5 ZrO_2

ZrO_2 ALD film growth has been studied by several researchers. Polycrystalline ZrO_2 films were grown at 200–300°C using $Zr[OC(CH_3)_3]_4$ and H_2O and yielded a dielectric constant $k \sim 32$ [37]. Crystalline ZrO_2 films have also been deposited using $ZrCl_4$ and H_2O [38]. A thick amorphous interfacial layer of < 5 Å, with a k value higher than the SiO_2 dielectric constant, was detected after deposition on an originally H-passivated silicon substrate. Accounting for this interfacial layer, a dielectric constant of $k \sim 25$–35 was estimated for the ZrO_2.

Uneven nucleation on the H-passivated Si substrate was suggested as a reason for the high leakage currents and uneven film morphology of the ZrO_2 films [38]. Nucleation problems have also been reported for ZrO_2 ALD films grown on H-passivated silicon. These nucleation problems are avoided by depositing on a thin SiO_2 layer on silicon [32]. A dielectric constant of $k = 23$ was reported for these ZrO_2 films using $ZrCl_4$ and H_2O precursors.

n-Channel MOSFET devices have been fabricated using ZrO_2 ALD films with a thickness of 5 nm [36]. These MOSFET devices are similar to the transistors described above using HfO_2. Unfortunately, excessive gate leakage currents were observed for these devices. No capacitance measurements were performed because of the high leakage currents.

10.5.1.6 Ta_2O_5

Ta_2O_5 ALD has been performed using $TaCl_5$ and H_2O at 310°C [29] and $Ta(OC_2H_5)_5$ and H_2O at 300°C [39]. These Ta_2O_5 films produced dielectric constants of $k = 28$ and $k \sim 24$, respectively, for the as-deposited amorphous films. However, a large increase to $k = 52$ was observed after annealing above 600°C produced a polycrystalline phase. Annealing at low temperatures reduced leakage currents, probably due to a reduction in impurities. The leakage currents increased greatly upon crystallization at higher temperatures [39].

Additional studies reported a dielectric constant for Ta_2O_5 ALD films of $k = 25$ using $Ta(OC_2H_5)_5$ and H_2O [40]. A dielectric constant of $k = 23$ was also observed for a water-free ALD process using only $Ta(OC_2H_5)_5$ and $TaCl_5$ precursors [41]. Unfortunately, the Ta_2O_5 ALD surface chemistry does have some complications. There is a slow etching of Ta_2O_5 by $TaCl_5$. $Ta(OC_2H_5)_5$ can also thermally decompose at > 275°C. Ta_2O_5 films grown at 325°C exhibited lower Cl contamination and higher dielectric constants than films grown at 275°C [41].

10.5.1.7 La_2O_3

La_2O_3 ALD films have been deposited using $La(thd)_3$ and O_3 [42]. Cubic La_2O_3 was formed at growth temperatures above 300°C and the hexagonal phase formed upon annealing at 800°C. Carbonate contamination decreased with growth temperature but was still significant (~3%) even at growth temperatures > 400°C. The La_2O_3 films were unstable in air and no dielectric constant measurements were reported in this investigation. From other investigations, the dielectric constant of La_2O_3 was reported as $k = 30$ [1].

10.5.1.8 TiO_2

TiO_2 ALD film growth has been described in numerous papers [6]. However, no dielectric constant values have been reported in these studies. Previous researchers have indicated that their TiO_2 ALD films were too leaky to measure the dielectric constant [43]. Titanium precursors included $TiCl_4$, TiI_4, $Ti(OCH(CH_3)_2)_4$, and $Ti(OC_2H_5)_4$ [6]. H_2O and sometimes H_2O_2 were used as the oxygen precursor. Dielectric constant values for TiO_2 include $k = 50$ [4], $k = 80$ [1] and $k = 100$ [3] depending on the crystalline phase of the TiO_2.

10.5.1.9 Nb_2O_5

Nb_2O_5 ALD films have been grown using $Nb(OC_2H_5)_5$ and H_2O at temperatures from 150–350°C [44]. No electrical measurements were reported in this investigation. However, the same researchers indicated that Nb_2O_5 had a dielectric constant of $k = 50$–200 with high leakage currents in a separate study [45]. In another investigation, a dielectric constant of $k = 163$ was measured for Nb_2O_5 ALD films grown at 325°C [46]. In similarity to TiO_2, the low resistivity of Nb_2O_5 films is attributed, in part, to slight deviations from the ideal stoichiometry [11, 46]. Monocrystalline Nb_2O_5 was reported to have a dielectric constant of $k = 35$–50 [11].

10.5.2 Ternary perovskites grown by ALD

Perovskites tend to have very large dielectric constants due to their ferroelectric properties at temperatures below their Curie point [1]. These ceramics have a face-centered-cubic crystal structure and no net polarization of charge above their Curie point. Below this temperature, the ions shift to create a permanent dipole in the material and a very high dielectric constant.

There is some indication that the dielectric constant of perovskites decreases for thin films with thicknesses $< 1\,\mu m$ [2]. This lack of scalability may mean that perovskites do not have an advantage over other high-*k* materials for memory and logic applications. Problems may also arise due to the low Curie temperature of some of these perovskite materials. The lower Curie temperature will make those perovskites unsuitable for devices with high operating temperatures.

$BaTiO_3$ (BTO) ALD films have been deposited using barium(pentamethylcyclopentadienyl), titanium tetraisopropoxide and water precursors at 275°C [47]. These $BaTiO_3$ ALD films yielded a dielectric constant of $k = 165$ after annealing at 500°C. $BaTiO_3$ ALD has also been achieved using barium dipivaloyl-methane chelate ($Ba(DPM)_2 \cdot 2$tetraene), titanium tetraisopropoxide and H_2O [48]. These films produced a dielectric constant of $k = 90$.

$SrTiO_3$ (STO) ALD films have been deposited using strontium bis(triisopropylcyclopentadienyl), titanium tetraisopropoxide and water precursors at 250–325°C [47, 49]. These STO ALD films yielded a dielectric constant of $k = 180$. Additional studies measured a dielectric constant of $k = 170$ using strontium dipivaloyl-methane chelate ($Sr(DPM)_2 \cdot 2$tetraene), titanium tetraisopropoxide and H_2O [48].

Additional studies have tried to grow other perovskite materials. Attempts were made to deposit $Bi_4Ti_3O_{12}$ using triphenyl bismuth, titanium isopropoxide, and water precursors [50]. This effort yielded $Bi_2Ti_2O_7$ with a dielectric constant of $k \sim 60$ after annealing at 500°C. However, $Bi_2Ti_2O_7$ is not a perovskite. $LaMnO_3$ was also deposited using $La(thd)_3$, $Mn(thd)_3$ and ozone precursors at temperatures above 250°C [51]. Unfortunately, no dielectric constants were reported in this study.

10.5.3 Properties of composite dielectric materials

Because finding one high-*k* material that exhibits all the desired properties is difficult, there have been many efforts to combine different materials to obtain the desired properties. Depending on the manner in which the materials are combined, the composite materials may be referred to as mixed materials, solid solutions, doped materials, nanolaminates, or superlattices. Mixed materials and solid solutions refer to fairly homogeneous mixtures of different materials. Superlattices and nanolaminates are layered materials. Doping refers to the intentional introduction of small amounts of impurities into a material.

In many cases, the resultant composite materials tend to have properties that are somewhere between those that were combined to make the composite material. This expectation is often referred to as the 'rule of mixtures'. However, this 'rule of mixtures' behavior is not always observed in practice. Combining materials can sometimes result in unusual and unexpected properties such as extremely high dielectric constants or negative differential resistance. For example, the perovskites $SrTiO_3$ and $BaTiO_3$ have high dielectric constants ($k > 100$). Much higher dielectric constants of $k \sim 10^3$–10^4 have been achieved when these perovskites are mixed to form $Ba_xSr_{1-x}TiO_3$ (BST) [2]. BST has been used in bulk capacitors and is being investigated for DRAM capacitor applications. Even higher dielectric constants of $k > 10^4$ have been achieved by doping high-*k* perovskites materials [3].

Composite dielectric materials are often fabricated to prevent the crystallization of high-*k* dielectrics under processing conditions. Metal oxides are alloyed with SiO_2 and Al_2O_3 to prevent their crystallization. The oxides of La, Hf, Zr, and Y have been alloyed with SiO_2 [2]. The dielectric constants of 50/50 alloys of these materials were predicted and, in some cases, measured to be approximately an average of the two materials.

The crystallization temperature increased approximately proportionally with Si concentration in the La_2O_3/SiO_2 alloy. The crystallization temperature increased from ~400°C for pure La_2O_3 to over 1000°C for an alloy with 70% SiO_2 content [2]. No crystallization was reported for La_2O_3/SiO_2 alloys above 70% SiO_2 content. Promising results have also been achieved with Si-doped zirconium aluminates [52]. These materials exhibit reasonably high dielectric constants of $k > 15$ without crystallization during typical processing conditions. Zr and Si dopants have also been used in Al_2O_3 to quench traps and reduce leakage currents [53].

ALD is particularly well suited for depositing mixed materials (solid solutions) and layered materials (nanolaminates, superlattices). The exact sequence of a large number of different reactant pulses used to deposit the film can be easily and precisely controlled during ALD. Various properties of composite materials can be tailored to meet the requirements for specific applications. Mixed materials can be deposited by alternately dosing the various precursors for the different materials. Nanolaminates are formed by depositing more than one monolayer of each material before switching to the other set of precursors. ALD allows for the precise control of the thickness of the individual layers. TEM images have shown that ALD can conformally and uniformly coat 3D structures with multilayer nanolaminates [22].

10.5.4 Composite materials grown by ALD

Many nanolaminates and solid solutions consisting of combinations of Al, Hf, Nb, Ta, and Zr oxides have been grown using ALD. Dielectric constants ranging from $k = 28$ to $k = 98$ were measured for mixed Nb_xTa_yO solutions and Nb_2O_5/Ta_2O_5 nanolaminates [54]. In addition, the leakage currents were lower than the leakage currents measured for the individual materials. The addition of ZrO_2 further reduced the leakage currents and yielded $k = 28$–33. Another study of the Nb_xTa_yO system was performed and reported dielectric constants as high as $k = 38$ with increasing Nb concentration [55]. Later studies investigated the temperature dependence of the electrical properties of $(Nb_{1-x}Ta_x)_2O_5$ films and measured $k = 24$–38 [46].

Ta_2O_5/HfO_2 nanolaminates have also been grown by ALD [56]. The dielectric constant of the nanolaminates varied between the dielectric constant of pure HfO_2 ($k = 16$) and pure Ta_2O_5 ($k = 25$). However, the leakage currents of the nanolaminates were many orders of magnitude lower than the pure materials. The low leakage is attributed to the nanolaminate structure hindering HfO_2 crystallization. Similar trends were observed for Ta_2O_5/Al_2O_3 and Ta_2O_5/ZrO_2 nanolaminates [57]. However, for the Ta_2O_5/ZrO_2 nanolaminates, the dielectric constant of $k \sim 28$ was higher than the dielectric constant of pure Ta_2O_5 ($k \sim 25$) or pure ZrO_2 ($k \sim 19$).

The dielectric properties of Nb_2O_5/Ta_2O_5 and Nb_2O_5/Al_2O_3 nanolaminates and solid solutions were also investigated more thoroughly in recent investigations [11]. The addition of Al and Ta to Nb_2O_5 dramatically decreased leakage currents by hindering crystallization. In the case of nanolaminates, crystallization was hindered by decreasing the Nb_2O_5 layer thickness. The measured dielectric constants were generally related to the percent composition of the material.

Ta_2O_5 and Al_2O_3 nanolaminates have displayed dielectric constants from $k = 8.1$ to $k = 28$ as the Ta_2O_5 layers became thicker and Al_2O_3 layers became thinner [29]. A related study showed similar results with dielectric constants rising from $k = 8.4$ to $k = 24$ with increasing percentage of Ta_2O_5 [25]. The leakage current of Ta_2O_5 also decreased drastically with the addition of Al_2O_3. Al_2O_3/ZrO_2 dielectric stacks have also been deposited by ALD [58]. A NH_3-treated silicon surface was used to deal with the nucleation problems of growing Al_2O_3 on H-passivated silicon. EOT thicknesses of < 1 nm were achieved using this approach while keeping leakage currents at ~1 mA/cm^2.

HfO_2–SiO_2 and La_2O_3–SiO_2 dielectric alloys have been grown to combine the crystallization resistance of SiO_2 with the high dielectric constants of HfO_2 and La_2O_3 [59]. No *k* values were reported in this work, but similar mixed films had dielectric constants between the dielectric constants of the individual films [2]. For the partially crystallized Zr_xTi_yO ALD films grown at 300°C, the dielectric constant was $k = 45$–65 when grown on ITO [43]. However, the effective dielectric constant was only $k = 35$ when grown on silicon. This lower dielectric constant probably resulted from an interfacial oxide layer.

The perovskite materials have also been explored in alloys and nanolaminates. Much of this work has focused on $BaSrTiO_3$ (BST). Several investigations have used ALD to fabricate $SrTiO_3/BaTiO_3$ solid solutions and nanolaminates [48, 60]. The maximum dielectric constant of $k = 450$ was measured for a 20/2 monolayer $SrTiO_3/BaTiO_3$ superlattice. This dielectric constant compares with $k = 170$ for $SrTiO_3$ and $k = 90$ for $BaTiO_3$. The unusually high dielectric constants are attributed to the lattice strain at the $SrTiO_3/BaTiO_3$ interfaces. This lattice strain results in a change in polarization.

Dielectric relaxors are a class of dielectric materials with very high dielectric constants. Dielectric constants up to $k = 10\,000$ have been measured for La-doped PZT [4]. Even higher *k* values as high as $k = 65\,000$ have been measured for $BaTi_{1-x}Sn_xO_3$ [3]. No reports of the ALD growth of dielectric relaxors were found at the time of this review. However, this area remains an exciting possibility for ALD and awaits future research.

10.5.5 Future use of ALD in device fabrication

Most known high-*k* materials have been successfully deposited by ALD. These high-*k* materials deposited by ALD exhibit dielectric constants comparable with films grown by other techniques. The ease by which ALD can be used to grow mixed films and nanolaminates promises to facilitate the discovery of new composite high-*k* materials. These composite high-*k* materials can be designed for the best combination of high dielectric constant and low leakage current.

Despite all the promising research on alternate high-*k* materials, there are problems for microelectronics applications of high-*k* ALD films. The main problem is that the dielectric constant of high-*k* films tends to decrease significantly when the thickness is decreased to a few nanometers. For example, the dielectric constants for Al_2O_3 ALD films of various thickness on Si(100) are shown in Fig. 10.5. The primary reason for this decrease is that many high-*k* dielectrics, such as Al_2O_3, tend to form interfacial SiO_2 when in contact with silicon. The interfacial oxide reduces the gains that can be achieved with high-*k* materials. The elimination of this interfacial SiO_2 is a critical goal that should be the focus of future research.

Materials with very large dielectric constants, like perovskites, also do not appear to be scalable. The crystal structures that lead to the high-*k* values are no longer present in thin films. This lack of scalability will restrict the application of perovskites to devices with thicker dielectric films.

Researchers are also investigating alternate device designs in conjunction with high-*k* research [2]. Many of these devices are vertical designs rather than the conventional planar designs. Vertical designs will allow for increased device density. These vertical designs include high surface area trench capacitors [20] and vertical transistor geometries [61]. ALD allows for the uniform, conformal coating of complex 3D structures. Consequently, ALD is uniquely suited for fabricating these vertical device structures.

Al_2O_3 ALD films have been used to coat uniformly high surface area, cylinder-type poly-Si to make 1 Gbit DRAM [20]. By using a TiN top electrode to make a MIS structure, a 1 Gbit DRAM has been achieved with a cell capacitance of 30 fF and a leakage current of only 0.5 fA/cell at 1.2 V. Vertical replacement-gate (VRG) n-MOSFET devices have also been produced using Al_2O_3 and HfO_2 films grown by ALD [61]. The devices fabricated using HfO_2 films had an EOT of only 15 Å with very low leakage currents densities of 10^{-7} A/cm^2. This geometry produced 50 nm transistors that was a record as of 2001. Lastly, a new approach for high-density flash memory involves using Si quantum dots grown on a thin tunneling dielectric. A recent study has shown that Al_2O_3 tunneling dielectrics < 1 nm thick deposited by ALD are superior to the previously used Si_3N_4 and SiO_2 dielectrics [62].

10.6 Conclusions

Many promising high-*k* materials are currently being investigated as dielectric materials to replace SiO_2. However, the stringent requirements for microelectronics applications have proven extremely challenging. While some promising results have been obtained, the search for the ideal high-*k* material is continuing and leading towards various kinds of composite high-*k* materials and even new device structures. Atomic layer deposition (ALD) is an exciting and emerging deposition technology that promises to play a key role in enabling the fabrication of these new types of materials and structures. ALD facilitates the conformal, atomic layer controlled growth of high-*k* materials on 3D surfaces at temperatures that are generally lower than those required for CVD. ALD is also especially well suited for making various types of composite mixed materials and nanolaminates. The nanoengineering of materials using ALD has created composite materials that combine the desirable properties of different materials. These nanocomposites can also sometimes exhibit unexpectedly high dielectric constants. The ability of ALD to coat complex structures with thin high-*k* films is also essential for the development of some new alternate device structures.

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Interlayer Dielectrics for Semiconductor Technologies
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Chapter 11
Dielectric materials in optical waveguide applications

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Abstract

Optical waveguide applications of dielectric materials are reviewed. General considerations, including a review of various waveguide applications and desirable specifications of optical waveguide devices, are discussed first. The general characteristics of inorganic and organic dielectric materials are also reviewed. Finally, the literature on specific organic and inorganic materials is reviewed with inclusion of information on both fundamental limitations and demonstrated applications.

11.1 Introduction

In order to extend the development of faster, smaller, and more powerful computers beyond the next few generations, it will be necessary to develop new architectures. The current technology employs silicon CMOS devices connected with aluminum and/or copper wires. The fundamental limitations of electrical interconnects have their origins in the resistance, capacitance, and inductance of long, thin metal wires. Incremental improvements can be made through improvements in materials (e.g. low dielectric constant insulators to decrease capacitance). For more significant long-term gains, researchers are now exploring 3D chip architectures, RF transmission lines, and optical interconnects.

In electronic wire circuits, the length of the interconnect is the most important scale factor. A longer line demands a larger cross-sectional area in order to maintain the same rise time. For a given length, the cross-sectional area must increase in order to increase the data transfer rate. The actual scaling relationship depends on whether the wire is long or short compared to the wavelength of the highest frequency component of the signal [1]. For long lines, wire or strip line bit rate capacity falls as the square of the length of the wire for fixed

cross-sectional area [2, 3]. As wire cross-section increases, it becomes difficult to mechanically attach the wires to a dense set of devices. Multichip modules with multilayer metallization with short vias to appropriately thick wiring layers address this issue now – with thicker layers carrying information for longer distances.

The bit rate capacity or bandwidth of a passive optical waveguide is independent of length for any length considered for chip-level interconnects. Similarly, dispersion will likely prove to be negligible compared to bandwidth limitations imposed by the modulators and sources. The cross-section of the waveguide will be determined by the limits acceptable, losses in parallel guides, and in features such as bends. Coupling between parallel sections of waveguide is determined by the index difference between core and cladding, the spacing between guides, and the wavelength of the carrier.

Optical interconnects require sources, modulators, a transmission medium, and receivers. Interconnects on the MCM, chip-to-chip, or chip-to-board level may involve integrated waveguides, active optical devices including active optical waveguides, external cavities. Photonic integrated circuits may involve architectures in which light propagates parallel to the surface in planar waveguide structures or perpendicular to the surface in stacked structures. Of course, light may also propagate in free space as well as in guided wave systems. We focus in this review on guided wave systems.

Optical interconnects may find useful implementation on a variety of levels of interconnection. In Table 11.1, we have summarized some relevant length scales for different implementation schemes. In Fig. 11.1, we have sketched some of these interconnect schemes with the intent of giving a broad idea of a scheme. The details of the structure of the waveguides or couplers will be discussed later. What is important to us in this discussion are the footprint and the length, width, and depth of the line between devices.

Table 11.1 Approximate length scales for various implementations of passive waveguides for interconnects

Implementation	Via length (μm)	Distance (cm)	Width (μm)	Height (μm)
On-chip	1–5	2	1	1
Stacked wafer – through-connect (3D)	10–100	0.01 (through) 2 (across)	2	2
Stacked wafer – edge-connect (3D)	1–5	0.1–5	5	5
Chip to chip (MCM)	1–5	0.1–5	2–5	2–5
Chip to fiber (chip to board)	1–5	0.1–2	1–5	1–5

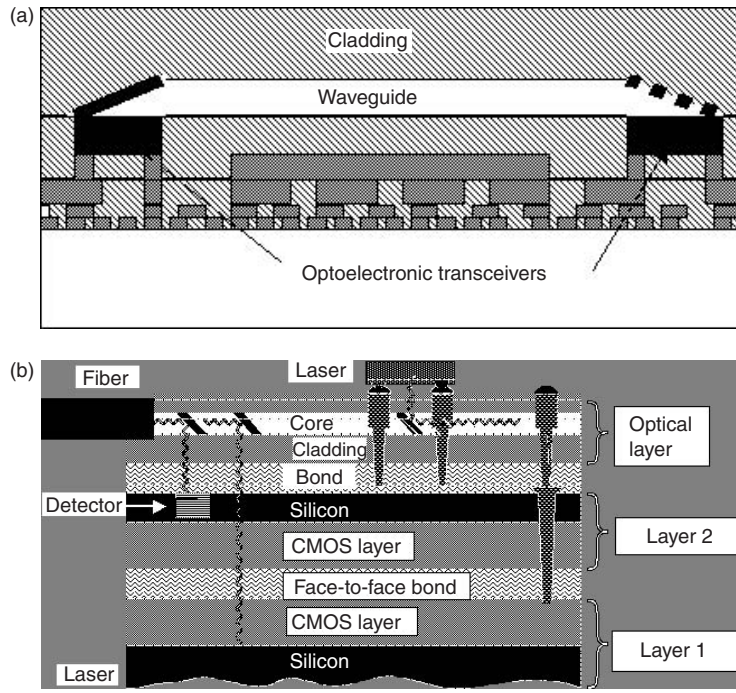

Figure 11.1 Schematics of various realizations of optical interconnects: (a) On-chip interconnects. As an example, the waveguide core would have a thickness of 2 μm, and each of the cladding layers would have thickness of a few micrometres as well. The optoelectronic transceiver dimensions would be of order a few micrometres on a side as well; (b) An example of three-dimensional, through-wafer interconnects based on the face-to-face architecture proposed by Gutmann *et al*. [4].

At the lowest level, optics may be used to interconnect two functional units on the same chip as shown in Fig. 11.1(a). In one scheme, a chip with CMOS FET gate length of 100 nm is electrically coupled to an optoelectronic transceiver by a soldered flip chip pad of dimension, ~4000 nm [3]. A surface-emitting vertical cavity laser (VCSEL) thus bonded might have lateral dimension of 1000–2000 nm and the footprint for the waveguide at the device surface would be ~2000 nm × 2000 nm. At this point the optical wave is traveling vertically and it is necessary to turn it into the plane of the chip surface in order to propagate across the chip; therefore, the beam must be turned within a vertical space of 2–5 μm. This can be accomplished with a sharply angled mirror surface in a high index waveguide such as that modeled using FullWave™ in Fig. 11.2a. A sharp radius bend can also be made with a lower index waveguide but with a reflecting (metal or multilayer) mirror at the bend as shown in Fig. 11.2b. Such interconnects might be used either for clock distribution across the whole chip or to replace only the longest lines on a chip, which are currently a few centimeters in length. We note that there may be a thousand such lines on a single chip. Such lines make up only a small fraction of interconnects, but contribute significantly to clock speed limitations [5]. We note that each modulatable source

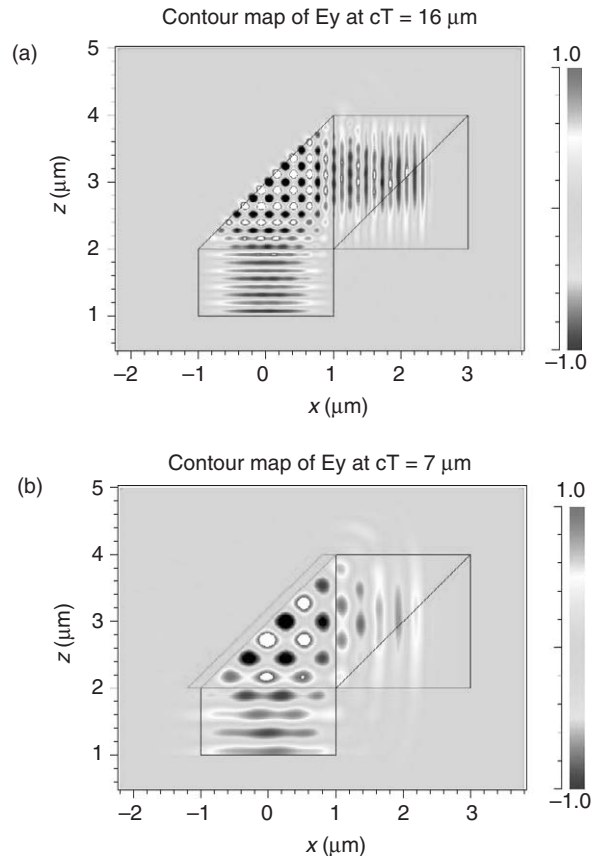

Fig. 11.2 Simulation of electric field intensity in a 90° bend mirror on a 2-μm waveguide: (a) a high-index waveguide that uses a total internal reflection mirror; (b) a low-index waveguide that uses a metal mirror.

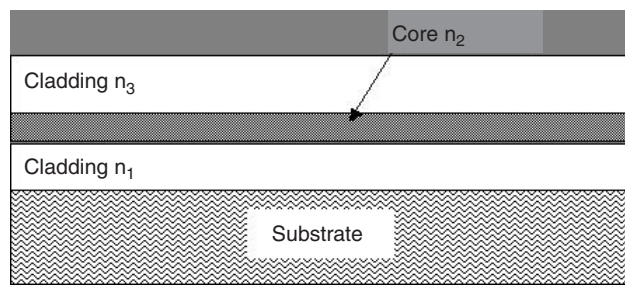

Fig. 11.3 Schematic of a prototypical three-layer index-difference waveguide.

(e.g. VCSEL), modulator (e.g. FET SEED), or receiver will have several transistors associated with it either to drive current or to amplify signal [3].

Optical interconnects could also be implemented in new three-dimensional chip architectures in which portions of a chip are bonded atop one another [4, 6]. A schematic is shown in Fig. 11.1(b). Such a design leads to a significant decrease in the length of the longest metal interconnects, but optical interconnects may still be able to play a useful role for off-chip communication or clocking. An optical guided wave might then be expected to pass from layer to layer. In one scheme, the active CMOS layers are bonded face-to-face and optical interconnects would be expected to replace the remaining longer lateral lines and to be able to pass from chip to chip. In other schemes, wafers are bonded back-to-back or back-to-front and optical vias would need to pass through the substrate as well as along the plane of the wafer. In all of these approaches, new constraints will be placed on materials and processing compatibility beyond normal CMOS processing.

In another three-dimensional scheme, stacked chips are interconnected at their edges to an interconnect backplane. Guided wave optical interconnects could clearly play an important role in this implementation. It would be necessary to steer optical signal from an optoelectronic transducer on the chip to the edge of the chip, couple it from the chip to the backplane, through the backplane, and then back to a transducer on another chip.

Optical interconnects can also be implemented at the package level. The optical signal is coupled from the chip into a substrate that contains passive waveguide components and then back into another chip a few centimeters away. Both the chip and the substrate contain waveguide components. On the chip, it might necessary to bring light to the surface using an optical via. It might also be useful to collect optical signals from different locations on the chip surface into an optical connect pad that is coupled to the substrate. Signals could then be wavelength-demultiplexed in the substrate and sent to other chips on the substrate.

There are already many approaches for coupling from the chip to the board and beyond. Some recent programs in 0.5–100 m optical interconnects are reviewed in Ref. [7]. The aspect of these programs that most directly impacts progress in on-chip dielectrics is coupling the optical signal up from a small high-index micro-optical component to a large multimode optical fiber. If it were possible to accomplish waveguiding, tapering up in size, and bonding with similar materials, many processing issues would be simplified with concomitant reduction in cost.

One final consideration is the wavelength at which the waveguide will be implemented. Long-distance communication is implemented at the low-loss windows in silica fiber, ~1310 and ~1550 nm. High-efficiency lasers have been developed for both of these wavelengths. Polymer optical fibers for distances of up to several hundred meters are designed to operate at ~650 nm. Low-cost, efficient, and robust lasers are available at ~830 nm for optical integration. Performance of hydrogenated polymers generally degrades as wavelength is increased above 800 nm, but may be adequate for short-distance use in the near infrared. One advantage to 1550 nm over 830 nm is that 1550-nm light has a much smaller absorption coefficient in silicon. One then need not worry about excitation of unwanted carriers by stray light.

11.2 Desirable characteristics of passive waveguides

11.2.1 General considerations for on-chip and chip-to-chip waveguides

11.2.1.1 Types of waveguides

The most important waveguide class for optical interconnects is the channel waveguide, in which the optical mode is confined in two dimensions (usually the vertical, or z, direction and either x or y). The channel waveguide permits us to guide signal from point to point thereby interconnecting two elements in a manner analogous to metal wires in an electrical circuit. An optical fiber is an example of a channel waveguide.

Channel waveguides can be fabricated either by enclosing a high-index material within lower-index cladding (as for fiber optic waveguides), by constructing a cladding that acts as an interference or surface mirror, or by changing the effective index in a region of a planar waveguide by use of a stripline.

The classical *index-difference* waveguide is made by cladding a high-index material by lower-index materials as shown schematically in Fig. 11.3. In the geometric picture, waves traveling at small glancing angle ($\theta < \theta_c = \cos^{-1}(n_2/n_1)$) with respect to the waveguide interface experience total internal reflection and specific waves that meet phase-matching conditions of the waveguide can propagate with low radiative loss. This is the basis for fiber optics for long-distance communications. An outline of the important design conditions for index-difference waveguides is given in Section 11.2.3.

An *optical stripline* is formed by depositing a strip of lower-index dielectric material on top of a planar waveguide. The presence of the loading strip changes the effective index of the planar waveguide. It is expected that strip line waveguides will have less loss than rectangular heterojunction waveguides because scattering and absorption at sidewalls is eliminated. Ninety-degree strip line bends with radii as small as 2.5 mm have been demonstrated with negligible losses [8], but such a large turning radius will be unsatisfactory for on-chip and MCM interconnects. Because the index difference in a strip line is small, fabrication of small-radius bends is not practical.

Confinement of the optical wave can also be achieved by replacing the low-index cladding with a variety of other materials and structures that do not involve total internal reflection. Metal coatings lead to strong confinement, but absorption and scattering losses can be significant, so such waveguides cannot be used for distance larger than a fraction of a millimeter. A periodic reflecting medium might also be used to replace the cladding. For angles and wavelengths that fall within the stop band of the periodic structure, the wave decays exponentially with distance into the periodic medium, with most of the reflected wave returning to the core [9]. Recent implementations of these ideas for fiber optics include Bragg multilayers [10] and two-dimensional photonic bandgap claddings [11, 12].

A simpler structure that has been shown to have acceptably low loss for on-chip interconnects is the antiresonant reflecting optical waveguide ('ARROW') structure in which only a

few layers of high and low refractive index material are deposited with thicknesses chosen to create an antiresonant Fabry–Perot condition [13].

Most of the materials systems that we will discuss in the latter part of this review can be used as components in all of the waveguiding structures discussed in this section. For example, polymers can be used as index-difference waveguide cores, as claddings for higher index inorganic materials, or as components of an interference multilayer.

11.2.1.2 Important beam steering structures

Most of the structures we will discuss here are based on the index-difference waveguide. We introduce some basics here. For a monochromatic wave propagating in the z-direction in a slab waveguide (infinite in the y and z directions as shown in Fig. 11.2) the field will have the form: $E(x, y, z, t) = E(x, y)e^{-i(\beta z - \omega t)}$, which must be a solution to $(\partial^2 E/\partial x^2) + (k^2 n_i^2 - \beta^2)E = 0$ for each region of the structure. We shall assume here that $n_1 < n_3 < n_2$. The solutions are either harmonic or exponential functions of x in each region, depending on whether $(k^2 n_i^2 - \beta^2)$ is positive or negative. To support a waveguide mode we must have $kn_3 > \beta > kn_2$ and satisfy the appropriate boundary conditions, resulting in discrete values of β. For a symmetric waveguide ($n_1 = n_3$), the propagation constant for each mode m is easily found by solving the transcendental equation

$$\tan\left(\pi\frac{d}{\lambda}\sin\theta_m - m\frac{\pi}{2}\right) = \left(\frac{\sin^2\theta_c}{\sin^2\theta_m} - 1\right)$$

where $\cos\theta_c = n_1/n_2$. We find $\beta_m = n_2 k\cos\theta_m$, where $\cos\theta_m$ lies between 1 and n_1/n_2. The field decays exponentially with distance in the cladding from the core/cladding interface, $E \propto e^{-\gamma x}$. The mode-dependent exponential decay constant $\gamma_m = k(n_2^2\cos^2\theta_m - n_1^2)^{1/2}$ increases with index difference and decreases with mode order, hence the lowest order mode of a system with large index difference leads to the most well-confined fields. The solution of the field equations for important structures, such as bends, tapers, and splitters, is more complex, but the overall idea that large index difference and low mode order lead to lower radiative losses is maintained. Coaxial fiber-optic waveguides have relatively small index difference for two primary reasons. First, only one mode is allowed in order to eliminate intermodal dispersion. Second, as we will discuss later, the amount of scattering at the interface decreases with decreasing index difference.

11.2.1.2.1 Input/output couplers – off-chip and packaging

The implementation of optical interconnects will progress downward in level from board to board communications, to chip-to-board, chip-to-chip, and then possibly on-chip. It is, therefore, important that optical signal be coupled off-chip to either a fiber or an optical substrate package. For guided wave systems, we will need to couple from on-chip waveguides

to fiber optics with core dimensions of ~5–50 μm and cladding dimensions of tens to hundreds of micrometers. There are several possible coupling schemes involving guided wave optics, among them are: (i) evanescent wave couplers; (ii) butt couplers; (iii) holographic focusing surface gratings (with the fiber entrance perpendicular to the waveguide surface); or (iv) lens coupling.

In evanescent wave couplers, two waveguides run parallel to one another sufficiently close that their fields overlap. If the two waveguides are identical it is possible to achieve nearly lossless coupling. One can estimate the length necessary for complete coupling using coupled-mode theory [14]. The coupling coefficient is defined as

$$C = \frac{1}{2}(n_{\text{core}}^2 - n_{\text{cladding}}^2)\,\frac{k_0^2}{\beta_1}\int u_A u_B \,\mathrm{d}x\,\mathrm{d}y$$

where n is the index of the core or cladding as noted, β is the mode propagation constant, u_A is the field due to the first waveguide at position (x,y), and the integral is over one of the waveguides. The transfer distance is then $z_T = \pi/2C$. The minimum coupling distance for typical waveguide parameters is hundreds of wavelengths.

End-butt coupling involves aligning the core of the waveguide with the end of the waveguide to optimize overlap of the propagating waves. To optimize coupling, it will be necessary to adiabatically taper and shape the waveguide to match the waveguide mode to the allowed mode of the fiber [15, 16].

Input–output coupling to a waveguide can also be achieved with surface or volume gratings, both for surface-normal and in-plane coupling [17]. Gratings are particularly useful for demultiplexing different wavelength signals. Unblazed surface gratings have relatively low efficiencies of 10–30% with much of the intensity going into non-useful diffraction orders. In order to achieve efficient surface normal coupling, tilted gratings have been proposed [18–20]. Surface-relief gratings with tilted profiles can yield high diffraction efficiencies [21]. Holographic volume gratings typically have a small index difference and, therefore, must be relatively long (mm) to achieve high efficiency [22]. In a holographic focusing grating, the spacing between lines in the grating is varied so that light of a selected wavelength is focused to a point above the waveguide. Efficient focusing volume gratings of length ~1 mm have been designed and fabricated [23].

11.2.1.2.2 Input/output couplers

Input/output coupling applies at two levels in the device design. First, light may couple from a transceiver to a waveguide. Second, light must be coupled off of the chip for chip-to-chip or more distant interconnects. On-chip waveguide dimensions will typically be small – with a core of order a few micrometers or smaller. To minimize coupling loss to an optical fiber where the core diameter is of order ~5 μm, the on-chip waveguide must be scaled. Several groups have shown how this can be accomplished with an adiabatic taper [15, 16].

Since active device dimensions are likely to be of the order of a few micrometers, we also want vertical bends to be accomplished in a lateral space of approximately the same dimensions. This can only be accomplished with mirror-like structures and/or high refractive index reflection bends. An example of the field pattern for a bend taking a 2-μm horizontal waveguide into a 2-μm vertical waveguide with a metal 45° mirror is shown in Fig. 11.3. Theoretical insertion loss can be as low as 1 dB.

11.2.1.2.3 Wavelength filters

To take advantage of the bandwidth of optical interconnects, it will be useful to implement components for wavelength filtering and multiplexing. The main performance characteristics are the free spectral range, the finesse, the transmission at resonance, and the extinction ratio. For communications applications, where size is not the main concern, surface or volume gratings in waveguides [20] are the primary demultiplexing approach. For optical interconnects, inherently smaller designs have been proposed including Fabry–Perot multilayers and ring or racetrack resonators [24–27]. To achieve high finesse with small size, both of these structures must take advantage of large index differences (either for reflectivity or for confinement.).

11.2.1.2.4 Horizontal bends

In order to route the optical signal from input to output, it may be necessary to steer the waveguide in the surface plane to avoid existing structures or to direct the wavefront to a coupler. The simplest bend is a radius bend as shown in Fig. 11.4(a). Bend losses can be decreased by matching the field pattern in the input and output waveguides to the field pattern in the bend. A structure such as that shown in Fig. 11.4(b) improves the mode matching at the bend transition points. An example of a structure that employs large index differences to achieve high throughput with small size is shown in Fig. 11.4(c).

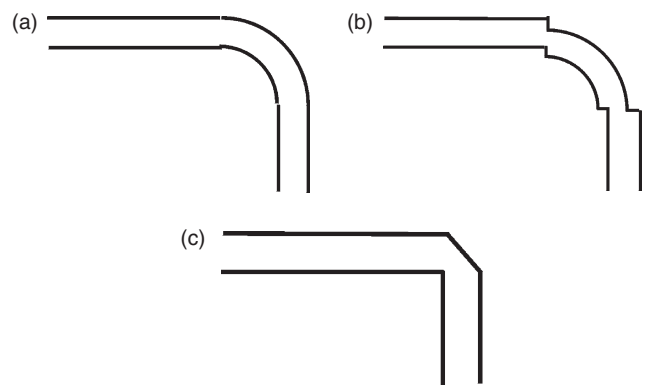

Fig. 11.4 (a) In-plane radius bend 90° turn; (b) Offset radius bend 90° turn; (c) Total internal reflection 90° bend using high-index materials.

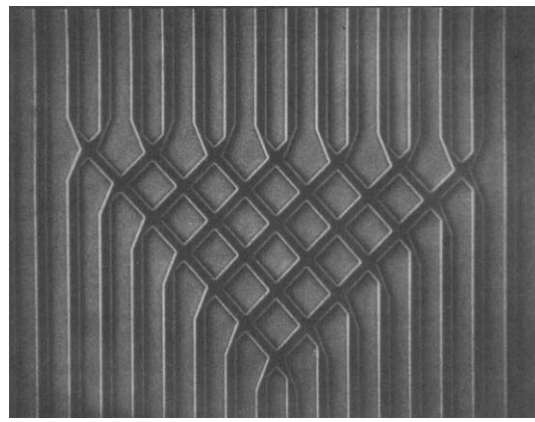

Fig. 11.5 Example of polyimide waveguide array for shuffle data processing [30].

11.2.1.2.5 Fanout

In one proposed implementation of optics on-chip, a regular clock pulse is distributed to many points on a chip simultaneously. This might be accomplished by an 'H-tree' architecture in which the signal is split in several stages along many nominally equivalent paths to receivers [27, 28]. If the power supplied to the center of the tree is P, then the power delivered to each receiver is $\eta P[(1-a)/2]^N$ for 2^N receivers where η is the coupling efficiency from the waveguide to the receiver, and a is the fractional power loss at each splitter. At best, the signal decreases by a factor of 2^N for 2^N receivers. Once again either amplification or source power must be increased to compensate for signal splitting and loss. It is important, therefore, that the loss (a) be negligible compared to 3 dB at each splitter.

Fan-out can also be accomplished by splitting the signal into more than two lines at each junction. An example of a 1×16 splitter is shown in Fig. 11.5. Once again, the magnitude of the signal is decreased by a factor of $(1-a)/N$, where a is the loss in the splitter and N is the number of taps.

11.2.2 Desirable specifications for passive waveguide components

11.2.2.1 Losses in straight waveguides, bends, taps, and fanout

The level of loss that is acceptable in a waveguide system depends on many factors. If the transmitting media have loss, then it is necessary to increase the source power, the power switched by a modulator, and/or the detector amplification. All of these increases result in increased heat generation on the chip and, since heat dissipation is a major issue for integrated circuits [3, 31], it is important to minimize transmission loss. The different implementations listed in Section 11.2.1 have different signal path lengths and differing ratio of path length to number of bends. For straight waveguide sections, the longest lines in any implementation are of order

5 cm, so a loss of < 0.2 dB/cm will likely be acceptable. For on-chip applications, straight-guide losses of < 0.5 dB/cm will likely be acceptable.

In order to route a signal from one point to another or to multiple points using optical waveguides, several features must be considered. First, it will be necessary to incorporate bends in waveguides in order to route guides around components and in order to steer the optical signal into and out of receivers, modulators, and sources. Bends will have to be fabricated both in the plane of the waveguide and perpendicular to the plane. To couple from a vertical emitter to a vertical cavity receiver, one needs at least two sharp 90° bends. In order to traverse a chip, one might expect four crossings and four bends, hence loss per crossing or bend should be kept below 0.5 dB.

For H-tree splitting with more than two stages, a loss of > 0.5 dB/split is likely to be unacceptable. For a single fanout step, a loss of 1 dB may be acceptable.

11.2.2.2 Waveguide cross-sectional dimensions, pitch, and placement tolerance

We wish to make waveguides as small as possible while maintaining acceptably low losses and cross-talk. Waveguide core dimensions of 2-μm diameter appear to be consistent with current wavelengths and etching technology. The distance between cores is determined by the difference in index of refraction between core and cladding. Larger difference allows smaller core–core distances. With core dimensions of 5 μm, it is necessary to place the waveguide $\pm < 1$ μm relative to detectors and modulators.

11.2.2.3 Thermal, environmental, and optical stability

Processing temperature to fabricate a waveguide or a waveguide component should be below ~300°C in order to avoid damage to existing CMOS and/or bump-bonded structures on the chip. Similarly, on-chip waveguides should be stable to > 350°C for 30 min so that they are not degraded by solder-bump attachment or other processing. On-chip waveguide materials should be capable of cycling from room temperature to 150°C many times, so thermal expansion difference with Si should be small. Waveguides should be capable of operating, without degrading, at ~100°C for thousands of hours. A standard environmental test in the CMOS community is to expose the chip to 85% relative humidity at 85°C for hundreds of hours. Optical losses should be less than 0.5 dB/cm for the lifetime of the entire system. Shrinkage must be mechanically compatible with the substrate.

11.2.2.4 Processing compatibility

The choice of materials and processing approach depends on the system in which optical interconnects are implemented. If optical interconnects are to be implemented for on-chip or 3D applications, then it is likely that the waveguides will be fabricated after CMOS and optoelectronic components are in place. Hence, the processing temperature of the waveguides should not

exceed 300°C for 30 min. The materials chemistry should be such that it does not attack or diffuse into existing CMOS, while still making a satisfactory bond to the surface. It is also possible that solder–bump bonding will occur after the waveguides are in place; therefore, waveguides should not degrade with thermal processing to 350°C for 30 min. Some proposed 3D processes may involve 400°C for 30 min. It is also advantageous if waveguide materials can be etched and shaped using standard CMOS techniques, such as reactive ion etching in an HCF_3/O_2 plasma. Non-standard processing, such as laser ablation or focused ion beam milling, adds to the complexity of the processing environment and the likelihood of implementation decreases.

11.2.3 General materials selection and design issues: sources of loss

When we choose a material set and processing path for waveguides, we need to consider many issues. First, we must ensure that the intrinsic absorption coefficient of the material fulfills loss criteria set in Section 11.2.2.1. Mechanisms for absorption loss are discussed in Section 11.2.3.1. Second, we must ensure that intrinsic scattering, such as scattering from thermodynamic density fluctuations, satisfies the same loss criteria. Third, we must ensure that we do not introduce excess surface or interface scattering during processing. This step involves consistent consideration of both processing techniques and the design of the structure. Finally, radiative loss due to mode mismatch or poor design must be minimized. We discuss basic loss mechanisms and design criteria in this section.

11.2.3.1 Absorption spectra – general characteristics for polymers and semiconductors

Several mechanisms can lead to loss in optical dielectric materials. In Fig. 11.6, we show a schematic of various transitions and their energy scales for a typical ionically or covalently

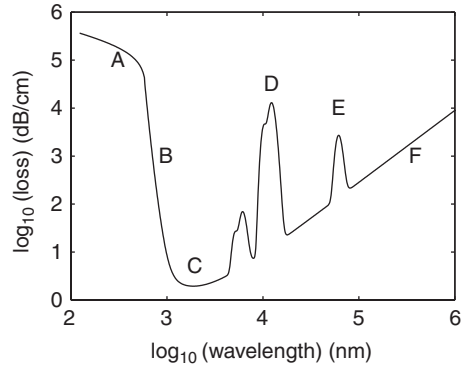

Fig. 11.6 Schematic summary of absorption processes in semiconducting solid materials. Letters label general classifications of transition: (A) electronic band-to-band transition; (B) exponential band tail; (C) electronic defect absorption; (D) vibrational transitions; (E) impurity absorption; (F) free carrier absorption.

bonded solid. Electronic transitions can take place between occupied electronic states and unoccupied states of the proper symmetry, annihilating propagating photons in the process. In semiconductors, the most important electronic transitions are band-to-band and impurity-to-band. Free carrier absorption occurs over a wide energy range, increasing algebraically as the photon energy decreases. Electronic transitions in polymers are usually discussed in terms of molecular states, but the concept of transition between bands is still useful. Vibrational absorption is usually in the infrared and is due to atom motions induced by the optical field. Scattering is a ubiquitous effect, occurring from atoms, from thermodynamic density fluctuations, from interface roughness, and from the edges of fabricated structures.

11.2.3.1.1 Electronic transition absorption

11.2.3.1.1.1 Crystalline and amorphous semiconductors

Electronic transitions between the highest occupied band of electronic states and the lowest unoccupied band give rise to the optical absorption edge or energy gap, E_G. This region of the spectrum is labeled 'A' in Fig. 11.6. The absorption coefficient, α, above the edge of a direct band gap crystalline material frequently has the form $\alpha = D(hc)^{1/2}(1/\lambda - 1/\lambda_G)^{1/2}$ where $D \sim 3 \times 10^4$ $(\mathrm{eV}^{1/2}\,\mathrm{cm})^{-1}$ and $\lambda_G = hc/E_G$ is the bandgap wavelength. Above the band gap of an indirect absorption edge material, vibrational (phonon) modes must be excited to conserve momentum and the absorption coefficient has the form $\alpha = A(hc)^2\lfloor N(1/\lambda - 1/\lambda_G + 1/\lambda_p)^2 + (N+1)(1/\lambda - 1/\lambda_G - 1/\lambda_p)^2\rfloor$ where λ_p is the wavelength corresponding to phonon absorption and $N = (\exp(hc/\lambda_p k_B T) - 1)^{-1}$ is a temperature-dependent phonon occupation factor. The absorption coefficient within several tens of millivolts of the gap is enhanced by excitonic interactions. In direct gap materials, this exciton absorption can be resolved into discrete absorption peaks at low temperature. At room temperature, exciton effects usually serve to enhance and broaden the absorption edge. Amorphous materials such as plasma-deposited silicon, silicon oxide, and silicon nitride are also potentially important for waveguides. A band gap can also be defined for these materials, where the absorption for wavelengths below the gap can be approximated by, $\alpha = B\lambda(hc)(1/\lambda - 1/\lambda_G)^2$ with $B \sim 10^5$–10^6 $(\mathrm{cm\ eV})^{-1}$ [32]. For amorphous materials, the band gap wavelength depends on both composition and details of the local structure [33].

For wavelengths longer than the absorption edge, the absorption in many materials can be characterized by an exponential region, $\alpha \sim \exp(hc/\lambda E_e)$. This is frequently referred to as band-tail absorption and is labeled 'B' in Fig. 11.6. In crystals, the exponential slope E_e is temperature dependent and is $\sim kT$ at room temperature and above. In amorphous materials, the exponential slope is preparation-dependent and has a value between 0.04 and 0.1 eV.

To avoid interband and associated band-tail absorption, the operating wavelength should be significantly longer than the band-edge wavelength. In Table 11.2 we have grouped some well-known and potential waveguide materials based on whether the electronic bandgap wavelength is shorter than each of the three major operating wavelengths (650, 830, 1310, and 1550 nm). Materials listed for a given wavelength are also likely to be useful for longer wavelengths.

Table 11.2 Well known and potential waveguide materials grouped by the electronic gap wavelength relative to predominant laser operating wavelengths

Gap wavelength	Materials
< 650	most polymers, SiO_2, Al_2O_3 AlAs, GaN, Si_3N_4, a-SiN_x:H, TiO_2, ZnO, Ta_2O_3, ZnS
< 830	a-SiC_x:H, a-Si:H Ca_2Si
< 1310	Si, GaAs, InP, a-Si:H, InAlGaAs
< 1550	a-Ge:H

In amorphous materials, network defects (e.g. dangling bonds) dominate absorption spectra in the long-wavelength region. The density of defects and hence the absorption loss is strongly dependent on preparation and history. For example, loss in high-purity sputtered amorphous silicon can be as high as 10^4 dB/cm at 1550 nm whereas loss in a-Si prepared with ~5–10% hydrogen can be as low as 1 dB/cm. A similar absorption is observed for grain-boundary related defects in crystals. This defect absorption varies slowly with energy and is labeled 'C' in Fig. 11.6.

At longer wavelengths, where the exponential tail absorption has become small, impurity and defect absorption becomes dominant. The peak energy, strength, and shape of the absorption spectrum in this region depend on preparation history and purity of the material. In crystals, impurity levels are well defined. Excitation from an acceptor (valence band) to the conduction band (donor) gives rise to absorption slightly below the interband absorption edge. Excitation from a neutral donor to conduction band or from valence band to neutral acceptor gives rise to absorption at energies well below the absorption edge (labeled 'E' in Fig. 11.6). Typical ionization energies for impurities in semiconductors are 5–50 meV.

Free carrier absorption occurs when an electron in the conduction band or a hole in the valence band is excited to a higher energy within its band. The free carrier absorption coefficient is proportional to carrier density and has an approximate power law dependence on wavelength ($\sim\lambda^2$) as shown in the region labeled 'F' in Fig. 11.6.

11.2.3.1.1.2 Polymers

The absorption spectrum of a polymer is generally similar to that of semiconductors; usually including an absorption edge (A), exponential tail (B), defect absorption (C), and vibrational modes (D). Optical and ultraviolet absorption in polymers is best described in the language of molecular orbitals, and the absorption bands are much narrower than in inorganic semiconductors. There are three important types of orbitals for describing polymer spectra. A σ-orbital has a cylindrically symmetric bond about the internuclear axis and a π-orbital usually has a plane through the axis along which the electron density is zero. An *n* orbital contains non-bonding electrons. If placing an electron in an orbital lowers the energy of the molecule then it is a bonding orbital. If it raises the energy, then it is antibonding and it is denoted with an asterisk (π^*).

Table 11.3 Electronic transition wavelengths for selected polymer bond types

Bond	Peak wavelengths (nm)
C–H	125
C–C	135
Si–O	150
C═C	180
COOH	205
NO	300, 665
Aromatic ring	205, 255

The primary transitions that give rise to optical and ultraviolet absorption in polymers are σ to σ^*, n to σ^*, π to π^*, and n to π^*. σ to σ^* transitions are usually the highest energy transitions. Electronic transitions are broadened by simultaneous closely spaced vibrational and rotational transitions that overlap to form a band. We have included a short list of specific bonds and typical peak wavelengths in Table 11.3. For additional chromophores and a description of how one can predict wavelengths shifts due to local environment, see Ref. [34].

11.2.3.1.2 Vibrational absorption

Absorption due to vibrational excitations is labeled 'D' in Fig. 11.6. The typical range of energies for fundamental vibrational modes is quite large, 5–500 meV. For semiconductors, the fundamental modes are low in energy, and vibrational absorption does not contribute significantly to loss. The frequency of the vibrational mode is determined by the spring constant k and the reduced mass of the atoms involved m, $\omega \propto \sqrt{km}$. The spring constant depends on the shape of the atomic potential well $k \propto \partial^2 U/\partial r^2$. Larger bonding energy generally results in proportionately larger spring constant. The magnitude of the fundamental peak increases with the ionicity of the bonds. We have listed optical absorption wavelengths for the fundamentals of selected vibrational modes in Table 11.4. Most of these wavelengths are much longer than the important data and communications wavelengths of 830 and 1550 nm, so the overtones that fall near these wavelengths are much more important. The measured absorption coefficient for PMMA is shown in Fig. 11.7. Figure 11.8 shows the calculated absorption strengths for various stretching modes of C–H, C–F, and C–Cl bonds. We note that the strength of the overtone peak falls exponentially, about one order of magnitude for an increase of overtone order by one. Because it has such a high fundamental frequency, the principal mode contributing to loss in the near-infrared is the C–H stretch. The first harmonic falls near 1600 nm, leading to excess absorption at 1550 nm. Substituting D for H decreases the calculated vibrational peak absorption losses in the near-infrared by about one order of magnitude. Substituting F leads to a further decrease by three orders of magnitude. The second harmonic of the O–H bond falls around 1400 nm, causing excess absorption at both 1310 and 1550 nm.

Table 11.4 Vibrational transition wavelengths for selected polymer and solid materials

Bond	Peak wavelength range (nm)
O–H (in SiO_2)	1 380, 2200
C═C	1 500–1600
H–H	1 850–2500
N–H	3 000
C–H	3 200–3400
C–H_n	3 300–3600
C–D	5 000
Si–H (in Si)	4 500–5000
C–F	8 000
C–Cl	13 000
Si–C	14 000–15 500

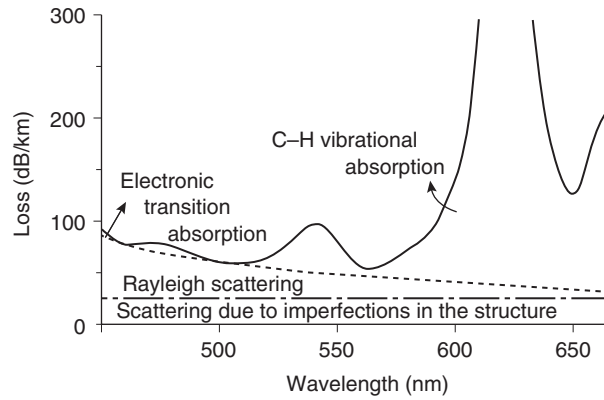

Fig. 11.7 Optical absorption coefficient plotted as a function of wavelength for PMMA [35].

11.2.3.2 Scattering

11.2.3.2.1 General considerations

Scattering from spatial fluctuations in index on a scale shorter than the wavelength of the light is an important source of loss in all waveguides. The spatial variation in index can arise from roughness of the interface profile, or from fluctuations of the density or composition. A fluctuation in density can be intrinsic; for example, it can arise from thermodynamic or statistical fluctuations. A fluctuation in composition is usually extrinsic; for example, it is due to a grain boundary in a crystal or an impurity. Variations in phase (e.g. crystalline versus amorphous) or

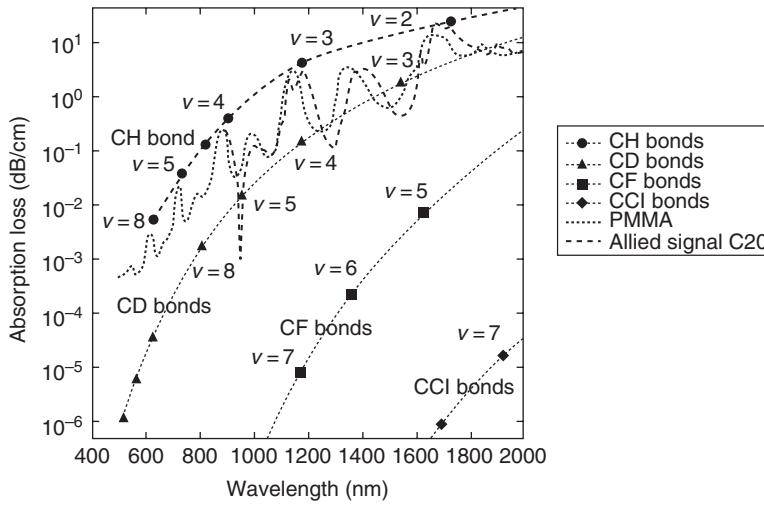

Fig. 11.8 Calculated absorption losses for various vibrational overtones [36].

orientation (if the has molecular anisotropy) can also lead to variations in index. Some aspects of scattering are independent of the detailed origin of the fluctuations. If the size of the scattering center is small compared to the wavelength of light, then the scattering can be described by the Rayleigh approximation. The scattered power for a single non-absorbing spherical scatterer displays the most important relationships [37], $P_{sca} \propto E^2\alpha^2/\lambda^4$, where E is the local field. The polarizability α is proportional to the volume of the scatterer and the difference in the index of refraction between the scatterer and host, so $P_{sca} \propto E^2V^2\delta n^2/\lambda^4$. So scattering loss from small inclusions varies as λ^{-4}, increases as the square of index difference, and the square of scatterer volume. These relationships must be modified when the dimensions of the scattering volume approach optical wavelengths or if the scatterer is absorbing, but the strong scaling with wavelength and scatterer size should be kept in mind when choosing waveguide materials or processes.

11.2.3.2.2 Intrinsic bulk scattering

Local fluctuations in the index of waveguide materials can have several intrinsic origins. Total scattering in homopolymers and glasses is dominated by frozen-in density fluctuations and adiabatic waves for all glasses, and orientational variations of polymer groups (birefringence) and ordering of macromolecules [37–39]. The relation between density and index relates scattering to density fluctuations, $\delta\varepsilon = (\partial\varepsilon/\partial\rho)\delta\rho$. Even in an isotropic network glass such as SiO_2, local isobaric density fluctuations can be frozen in as the material is cooled through the glass transition temperature. Isobaric density fluctuation due to temperature fluctuations has the form, $\delta\rho \propto k_B T^2\sigma^2/C_p$ where σ is the coefficient of volume expansion and C_p is the specific heat.

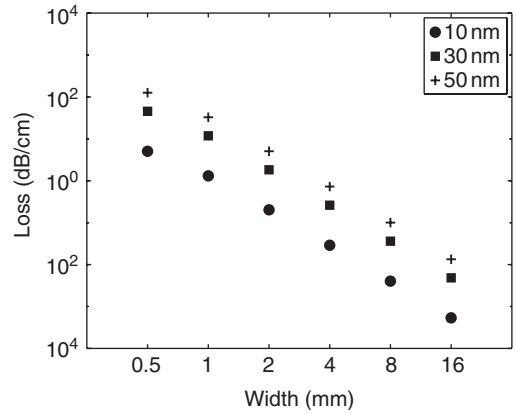

Fig. 11.9 Computed transmission loss in a polymer core waveguide plotted against waveguide width for various rms roughnesses. The core index is taken to be 1.52, the substrate index 1.46, and the cladding is air.

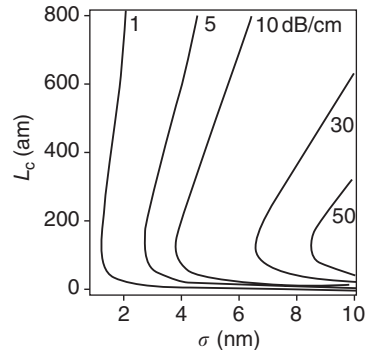

Fig. 11.10 Calculated contour map of loss with correlation length L_c and roughness σ as parameters. The index of the core is 3.5, the cross-section of the waveguide is 500×200 nm, and the wavelength is 1540 nm (from [45]).

Adiabatic density fluctuations have the form $\delta\rho \propto \rho k_B T_{eff} \kappa$ where κ is the adiabatic compressibility. Fluctuations can be frozen-in if the glass is cooled through the glass transition temperature and will certainly be non-thermodynamic if the material is vapor deposited below T_g. Intrinsic scattering loss in glassy homopolymers can be quite low, of order 21×10^{-5} dB/cm in polystyrene and 12×10^{-5} dB/cm in PMMA in the visible at room temperature [35].

Polycrystalline and nanocrystalline materials have been suggested as candidates for thin films waveguides. Scattering in these systems will occur if the index varies (i) at the grain boundaries, (ii) with crystal orientation, or (iii) with strain (which may change from crystallite to crystallite) In addition, the polycrystallinity may lead to etching variations that result in rough surfaces. The scattering scales as the square of the index difference. The correlation length of

the index variation is also important; when the correlation length (crystallite size) is comparable to the wavelength of the light in the medium the scattering is a maximum. Polycrystallinity will also contribute to side and top surface roughness, which also affects loss as we discuss below. We note here that grain boundary regions and surfaces may also contribute to excess absorption due to electronic defects.

11.2.3.2.3 Interface scattering

Scattering from interface roughness can be one of the primary loss mechanisms for micrometer-scale waveguides. The problem of interest is that of scattering of glancing incidence rays from a slightly rough interface. By slightly rough, we mean $\sigma \ll \lambda/(4\pi \cos\theta)$, where σ is the rms interface width and θ is the angle from the mean surface normal. We summarize here some of the important scaling factors for scattering – detailed treatments of many specific cases can be found in Refs [41–46]. Analytical approximations predict that interface scattering loss α_{ts} in a ridge waveguide scales simply with interface roughness σ, wavelength, index difference Δn, and interface field strength E. For a step-index ridge waveguide, $\alpha_{is} \propto \lambda^{-4}\sigma^2\Delta n^2 E^2$. The interface field strength depends on other waveguide parameters such as index difference, waveguide size, and mode number, complicating the simple scaling dependence on these parameters [40]. For sidewall scattering the field dependence introduces dependence on size: $\alpha_{is} \propto w^{-4}n^{-1}$ [45]. In Fig. 11.9, we show an example of computed and experimental interface scattering loss plotted against waveguide width. In Fig. 11.10, we show an example of the computed loss for various correlation lengths and surface roughnesses. The strongest scattering is found when the interface autocorrelation length is comparable to the wavelength of the light.

11.2.3.3 Loss due to direction changes and junctions

Bends can be accomplished in two general ways. First, the wave can be guided through a gradually changing path. The simplest model structure for this is a 90° radius curve. Second, the wave can be reflected at a sharp turn as shown in Fig. 11.4.

11.2.3.3.1 Radius bends

There are three categories of loss introduced by radius bends. First is radiation loss due to the curvature of the waveguide as described by Marcuse [46]. Second, the curvature of the guide shifts the field maximum towards the outside of the curve and increases the field at the interface, thus increasing scattering from roughness at the interface. Third, the mode mismatch between the straight and curved guide segments leads to scattering out of the fundamental mode into higher-order modes that may have higher loss.

The radiation loss for a bend of radius R can be described by an expression of the form [48] $R\alpha_R \propto e^{-CR}$ where $C = 2(\beta^2 - n_{clad}^2 k_0^2)^{3/2}/3\beta^2$ depends on core and cladding refractive indices (See Fig. 11.11). Loss, thus, decreases dramatically when either the refractive index difference is

increased or the radius is increased. In Fig. 11.12, we show a simulation of the radiation loss for various radii plotted as a function of the index difference. We thus see that it is not possible to make a low-loss radius turn with radius less than ~10 μm using practical index values. This large radius may be satisfactory for in-plane turns, but will not suffice for vertical bends.

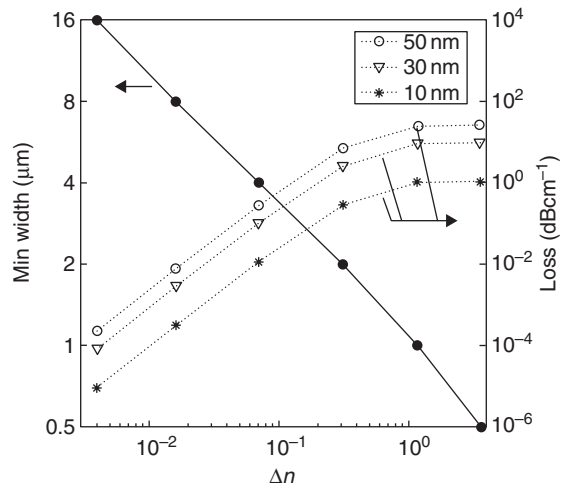

Fig. 11.11 Dependence of scattering loss on the index difference between core and cladding for a cladding index of 1.46; wavelength = 1550 nm; rms roughness of 10, 20, and 50 nm; and waveguide dimensions of 1000 nm × 1000 nm (right axis). If we set a maximum allowable loss of 1 dB/cm, then the minimum allowable waveguide dimension can be estimated (left axis).

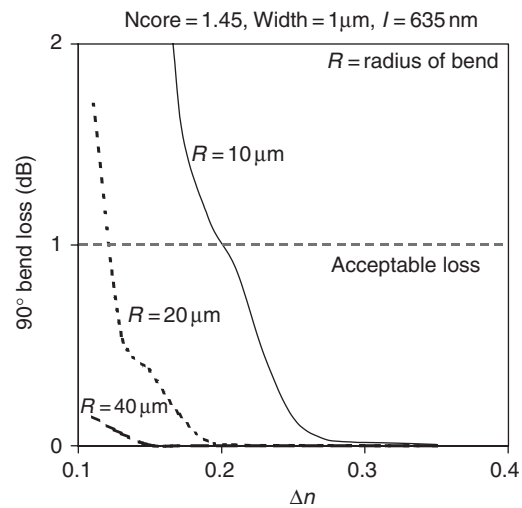

Fig. 11.12 Radiation loss plotted as a function of core–cladding index difference for 635 nm light passing through a 90° radius bend for various radii. The cladding index is 1.46 and the waveguide dimensions are 1000 nm × 1000 nm (from Ponoth [49]).

Intermodal scattering loss can be ameliorated by adjusting details of the shape of the waveguide entering and exiting the bend. For example, for a 2000-nm wideguide with core index of 1.6, cladding index of 1.46, and radius of 20 μm, offsetting the straight waveguide sections laterally by 200 nm decreases the loss to < 1 dB, compared to the loss in an unshifted waveguide bend of > 10 dB.

11.2.3.3.2 Mirror bends

Spatial constraints in CMOS-compatible on-chip waveguides will require beam steering through large angles in a longitudinal or vertical space as small as a few micrometers. This cannot be accomplished with radius bends as described above. For small effective bend radii, the use of reflection from a corner mirror or reflection in a very high index contrast system is necessary. A right angle 'nanowaveguide' bend has been fabricated by the Kimerling group at MIT. The waveguide core is recrystallized Si and the cladding is SiO_2, resulting in an index difference of more than 2. A 'bulge' on the inside corner of the waveguide bend acts as a resonator and increases transmission efficiency of the bend. Sharp radius bends in Si have also been reported by Sakai *et al*. [49, 50] with a loss of < 1 dB for a channel width of 0.5 μm and effective bend radius of 0.5 μm. In Fig. 11.3, we show the electric field magnitudes plotted as a function of position for a 90° mirror bend in a polymer waveguide. In this case, the core/cladding index contrast is small, so it is necessary to include a metal mirror at the bend. For a 2-μm wide waveguide and a 90° bend, the bend loss is computed to be 2 dB. Loss can be decreased by adjusting the details of the shape of the inner corner of the waveguide.

11.2.3.4 Scaling and design considerations

From the point of view of CMOS compatibility we wish to decrease waveguide component size to sub-micrometer pitch and micrometer radius turns. Consideration of the wavelength of the signal, scattering, and the refractive index of available materials pushes the design in the opposite direction – to large structures. Replacing the longest on-chip metal lines and most chip-to-chip interconnects necessitates near straight-line waveguides of 1–20 cm in length. All of these desired properties lead to a multiscale design and fabrication problem.

11.3 A brief review of specific systems

Most of the materials that have been proposed for passive waveguides have relatively low as-deposited intrinsic losses at either 830 or 1550 nm – we must also consider extrinsic losses due to fabrication imperfections and losses at the insertion points of bends, couplers, and vias. In Tables 11.5 and 11.6, we show reported refractive indexes and losses for various passive and active waveguide materials; most loss numbers are for slab waveguides. If the report is for a ridge waveguide, dimensions are listed in the notes. Since the typical interconnect length will be

Table 11.5 Optical properties of selected inorganic waveguide thin film materials

Material	Index	Straight guide transmission loss (dB/cm)	Processing or deposition temperature (°C)	Maximum exposure temperature (°C)
		EPITAXIAL AND SINGLE CRYSTAL MATERIALS		
AlGaAs/AlGaAs	2.5	0.1 (830 nm)	> 500 (OMCVD)	> 500
GaAs/AlGaAs [51]	3.4	0.2 (1520 nm)	> 500 (OMCVD)	> 500
GaN [52]	2.33 (1300 nm)	–		
Lithium niobate [53]	2.2	0.2	~1000 (growth)	> 500
(Pb, La)TiO_3 [54]	1.87–2.4	> 10 at 633 nm	350	350
Potassium niobate [55]	2.1–2.35	0.2 (860 nm)	~1000 (growth)	225 (phase transition)
		POLYCRYSTALLINE AND AMORPHOUS MATERIALS		
SiO_2	1.46	< 0.1 (600–1600)	300 process (PECVD)	> 500
SnO_2/porous silica [56]	1.5–1.6		1200	> 500
Al_2O_3 [57]	1.7	< 2	200	
Amorphous silicon [58]	3.4	0.3 (1300 nm)	200	300
Si_3N_4 [59]	2.02	0.3 (633 nm)	770	> 500
a-SiN_x:H	1.9–2.05	1 (830 nm)	200–300	350
Polycrystalline Si on Insulator (SOI) [46]	3.5	< 0.1 (1550 nm)	600	> 500
TiO_2	2.5–2.7			> 500
ZnO [60]	1.98	< 0.01 (630 nm)	500	500
ZrF_4 [61]		~10 (670 nm)	100	?
Ta_2O_5	2.2	1 (633 nm) [62]		
Nb_2O_5	2.27	1 (633 nm) [62]		
ZrO_2	1.97–2.05			
ZnO	1.98 (830 nm)	5 (633 nm) [63]; 0.01 [60]	400; 500	

of the order of a centimeter, a loss per unit length of <1 dB/cm is acceptable. We have divided Table 11.5 into amorphous and polycrystalline materials that have been deposited onto a variety of substrates, and epitaxial and single crystal films that are typically grown only on specific substrates.

Table 11.6 Optical properties of selected polymer waveguide component materials

Polymer material	Index	Straight guide transmission loss (dB/cm at wavelength)	Maximum exposure temperature (°C)	Comments
Polycarbonate [64, 65]	1.59	0.2 (830 nm)		
Polycarbonate [66]	1.546	< 0.2 (830 nm), 0.8 (1300 nm)	200	
PMMA [67]	1.49	< 0.1 (630 nm), 0.2 (850) [65]	80	
Polystyrene [65]	1.59		90	
Polyurethane [68]	1.56	0.8 (850 nm)	100	
Photopolymerizable acrylate [69]	1.46–1.52	< 0.2 (630–900 nm)		Sensitive to oxygen
Benzocyclobutene	1.5–1.55	1[a], < 0.1[b]	350	Process w/CF_4
Preimidized polyimide [71]	1.62	0.3 (830 nm)		
Polyimide mixtures [72]	1.65	1.5 [72]; 0.4 [73]	250	
Polyetherimide [74]	1.61–1.65	0.23 (830 nm)		Stable
Polysiloxane [75]	1.53–1.535	< 0.2 (1330 nm)	200	Stable
Deuterated polysiloxane [76]		0.43 (1550)		Stable
Phosphazene [77]	1.37–1.65 (633 nm)			
Poly(cyclohexylsilyne) [78]		< 0.04 (830)	'Poor' [79]	Poor stability
Poly(norbornene) [80]	1.54	< 0.1 (820 nm)	280	Stable
Polyphenylsesquisiloxane	1.52	0.17 (1300)	200	
Siloxane epoxy [49]	1.52	< 0.5 (633, 830)	350	
		FLUORINATED MATERIALS		
Fluorinated acrylate polymers [76]	1.32–1.56	< 0.01 (830 nm) 0.07 (1550)	400, $T_g = -50$ °C	Stable. Sensitive to O during processing

Table 11.6 Continued

Polymer material	Index	Straight guide transmission loss (dB/cm at wavelength)	Maximum exposure temperature (°C)	Comments
Fluorinated polyimide [81]	1.55	<0.5 (630 nm)		
Photosensitive fluorinated polyimides [82]	1.52–1.62	0.3 (1300 nm)	300	
Photosensitive fluorinated polyimides [83]	1.55–1.60	0.4 (800 nm); <0.4 [71]	400	
Fluorinated polyimide copolymers [74]	1.52–1.62	<0.5 (830 nm)		
Chloro-fluorinated polyimides (6FDA/DCB) [84]	1.52–1.57 (1550 nm)	<0.4 (1550 nm)	350	
Perfluorocyclobutene (XU 35121) [76]		0.25 (1550)	400	

[a] From Ref. [68].
[b] Non-photodefinable bulk BCB (DOW Chemical Co., Technical Bulletin).

11.3.1 Inorganic materials

11.3.1.1 Silicon dioxide

Silicon dioxide is a ubiquitous material in CMOS and is, therefore, likely to be an important component in any waveguide system. The index of refraction of thermal oxide in the near-IR is 1.46. Thermal oxides have the lowest loss but they cannot be grown on top of existing CMOS devices. The index of plasma-deposited silicon oxide can be varied from ~1.45 to 1.49. The presence of H and the effects of stoichiometry play a role, affecting both the absorption and index. The relatively low index of oxide suggests that it will find use primarily as a cladding layer. The best-quality oxides are grown at higher temperatures [85]. Plasma deposited silicon oxides of excellent optical quality can be deposited below 200°C [86]. Chemical etching of oxides usually requires either HF (for wet etching) or some other source of fluorine (e.g. HCF_3) for plasma etching. One must take care with plasma deposited oxides to choose conditions that do not produce large strains.

Since the degree of mode confinement depends on the difference between the core and cladding indexes, we can improve confinement either by increasing the core index or decreasing the cladding index. Xerogels, which are also being investigated as low-*k* materials in current metal–dielectric interconnect schemes, are an obvious choice for a low refractive index material. Xerogels are a porous class of dielectrics that are usually prepared by a wet chemistry *sol–gel* process. They consist of cross-linked nanometer sized silica clusters. If the diameter of the silica clusters is much less that the wavelength of light, then scattering is low. The refractive index is an average of the index of the silica spheres and the space between them and results in a nearly linear relationship of index to porosity. Stable films with index from 1.1 to 1.34 can be cast by spin-on techniques. Details of xerogel preparation and electrical applications are discussed elsewhere in this volume.

Ponoth *et al*. have demonstrated both silicon oxide and polymer waveguides with xerogel cladding [49, 87]. Around 1 μm of oxide was deposited with a silane and nitrous oxide plasma chemistry using a 13.56-MHz Plasma-Therm® deposition system. The substrate temperature during deposition of the oxide was varied from 150 to 300°C. It was deposited on xerogel films that had porosities ranging from 30–65%. Oxide waveguides exhibited lower loss and better adhesion for lower deposition temperature and for lower porosity xerogel cladding. Polymer slab waveguides on $n = 1.34$ xerogel exhibited loss below 0.5 dB/cm [49].

11.3.1.2 Amorphous silicon nitride and silicon oxynitrides

Amorphous silicon nitride can be deposited by thermal CVD from suitable precursors or by plasma-assisted chemical vapor deposition from silane and ammonia or nitrogen.

High-quality Si_3N_4 optical waveguides have been grown by thermal CVD of dichlorosilane and ammonia at $T \sim 750$–800°C. The index of refraction is 2.02 and slab waveguide loss has been reported of less than 0.3 dB/cm in the TE mode at 633 nm [59].

The band gap wavelength for plasma deposited material is ~400 nm and can be varied by changing the ratio of Si to N [88]. (The variation in stoichiometry is accommodated by excess hydrogen.) Hydrogen content also affects the band gap [89]. Optical-quality material can be deposited from room temperature to 300°C. The index of refraction also varies with hydrogen content, in the range from 1.9 to 2.05. For wavelengths more than a few hundred nanometers above the edge, the absorption is dominated by deep defects whose magnitude depends on details of deposition and thermal history. High-quality material has defect absorption in the 800–1550 nm range of ~5 dB/cm [90], so a-SiN_x:H is an unlikely candidate for the core of long on-chip lines. It may find application in shorter (millimeter-scale) devices such as splitters and bends. Using plasma-assisted CVD, silicon nitride can be easily deposited sequentially with silicon oxide or amorphous silicon to produce high-quality multilayer mirrors for wavelength selection [91]. Because of its differential etch rate (to silicon or silicon oxide) in wet or RIE etching, silicon nitride has also been used as an etch mask for CMOS processes.

Silicon oxynitrides have been deposited by plasma-assisted CVS from silane, oxygen, and ammonia or nitrogen [90, 91]. The band gap wavelength can be continuously varied from ~400 nm down to < 300 nm by replacing nitrogen with oxygen [85, 94–96]. The refractive index at 633 nm can be continuously varied from ~1.9 for nitride to ~1.45 for oxide [85, 94–96]. Thus, this system can be used for both core and cladding. When the nitrogen content exceeds 20%, the residual defect absorption is greater than 10 dB/cm unless care is taken to optimize growth conditions for each reactor.

11.3.1.3 Amorphous silicon

Hydrogenated amorphous silicon has been known as a device-quality material for transistor, detector, and photovoltaic applications for over 25 years [97, 98]. Since amorphous silicon has a large refractive index, it is a candidate core material for large index difference components such as mirrors and sharp bends; the major issue is absorption loss. Hydrogenated amorphous silicon waveguides are deposited by plasma-enhanced CVD from silane or by reactive sputtering in Ar and hydrogen at temperatures at ~200–300°C. Deposition at lower temperature frequently yields columnar microstructure [99] that could produce excess scattering from etched sidewalls. The wavelength corresponding to the band gap energy can be varied from < 750 to > 600 nm by varying temperature and plasma conditions. The intrinsic absorption coefficient decreases exponentially with increasing wavelength above the gap wavelength and still has a significant magnitude (> 10 dB/cm) at 830 nm. Thus, a-Si:H is most useful as a waveguide for long-wavelength applications at 1.3 and 1.55 μm. Above about 900 nm the absorption becomes dominated by deep defects, with typical absorption coefficients for intrinsic material of 0.5–50 dB/cm. The density of deep defect levels that give rise to absorption at 1310 and 1550 is affected by many growth and history parameters, including doping level and absorption of photons [100]. Interfaces can also contribute to excess absorption above 900 nm [101]. Examples of amorphous silicon ridge

waveguides on Si, SiO_2, or SiC_x:H, fabricated by photoresist and reactive ion etching techniques, can be found in Ref. [58].

11.3.1.4 Crystalline and polycrystalline silicon

Because of its high index and obvious compatibility with silicon integrated circuits, silicon itself is an important candidate for waveguides. The bandgap of silicon allows for applications at wavelengths longer than 1300 nm. In order to achieve strong confinement, the silicon waveguide should be bounded by a low-index material – silicon dioxide being a clear choice. This means that the silicon waveguide material will be grown on an amorphous substrate. The general requirements for low-loss waveguides on SiO_2/Si are: low doping in the guiding layer to decrease free carrier absorption, adequate SiO_2 thickness for isolation, and good crystalline quality with smooth interfaces to decrease scattering. Since grain boundaries contribute to excess scattering and absorption, they must be either passivated or eliminated. Silicon-on-insulator (SOI) materials can be prepared by a variety of approaches including SIMOX (Separation by IMplantation of OXygen), BESOI (Bond and Etch back SOI), Ultrabond (bonded wafers separated by hydrogen implants), and polycrystalline silicon (growth and annealing of thin film Si on oxide).

Kimerling and collaborators [24, 46, 102] have fabricated thin SOI waveguides with very low loss at 1540 nm. In order to lower scattering and absorption loss, both polycrystalline-Si and amorphous-Si films were annealed at 600°C for several hours. (Amorphous silicon films crystallize at this temperature.) Control of surface and sidewall roughness was very important, low-loss films had roughness of less than a few nanometers [103]. High-quality SOI substrates are also available commercially.

Rather than depositing the thin silicon waveguide layer, the SIMOX process creates a buried oxide layer within a Si wafer. The wafer is then annealed to remove implantation defects and recrystallize the Si overlayer. A SiO_2 cladding is added by PACVD. Losses as low as 2 dB/cm have been reported for 1300 nm [104]. They are largely due to the fact that the buried oxide layer is thin and the confined wave leaks out into the Si substrate.

Since both deposited polysilicon and SIMOX waveguides must be annealed at temperatures in excess of 500°C, such waveguides may be unsuitable for back-end-of-the-line CMOS designs.

11.3.1.5 Metal oxides and oxide ceramics

Low-loss thin-film waveguides have been demonstrated for several metal oxides. Many of them are transparent from the ultraviolet through to the far-infrared. SiO_2 has been discussed separately above as a low-index material. Medium-index materials include alumina (Al_2O_3), zirconia (ZrO_2), tantalum pentoxide (Ta_2O_5), zinc oxide (ZnO), and magnesium oxide (MgO). Titanium dioxide has a relatively high index of 2.4.

Zinc oxide has a bandgap in the ultraviolet and single crystal material has extremely low absorption throughout the visible and near-infrared. Its piezoelectric and oriented films have

been explored for electro-optic and acoustic wave devices [103]. The principle source of loss in thin films is scattering. The index of refraction at 830 nm is ~1.98. There is little dispersion beyond this wavelength. Zinc oxide has been deposited heteroepitaxially on crystalline substrates including Al_2O_3 [63] and GaN [52, 106]. Waveguide-quality ZnO films have also been deposited by RF diode sputtering onto glass substrates [63] and by DC triode sputtering onto thermal silicon oxide [60]. Early work on evaporated films showed excess absorption in a long tail from the fundamental gap [105]. Typical substrate temperatures during sputter deposition are 200–300°C. Waveguide losses in as-deposited films on amorphous substrates can be less than 0.5 dB/cm. Dutta *et al*. [60] found that laser annealing with a CO_2 beam that is absorbed only in the SiO_2 substrate and which heats the sample to an estimated temperature of 500°C for less than 1 s could decrease loss in the visible below the measurement limit of 0.01 dB/cm [60]. They proposed that this was due to decreased scattering at the substrate–film interface.

Bulk tantalum pentoxide has a refractive index of 2.2 in the red and very low absorption throughout the visible. Thin films have been developed primarily as high dielectric constant capacitor materials [107]. Films have been deposited or grown by a variety of techniques including oxidation of tantalum at 500°C [105], CVD, OMCVD, reactive sputtering, evaporation, ion-assisted deposition, sol–gel, and laser-assisted CVD. These growth techniques and dielectric properties are reviewed in Ref. [107]. The index of refraction of sputtered or CVD films can be slightly lower [107, 108]. Waveguide losses of less than 1 dB/cm at 633 nm have been reported for films on thermal oxide, prepared by reactively sputtering Ta in an oxygen and argon atmosphere [109].

Titanium dioxide has a bandgap wavelength of ~400 nm and can be prepared with very low absorption through the visible and infrared. The index of refraction is quite high among the metal oxides, approximately 2.5–2.7 in the near-infrared, depending on phase. Polycrystalline, nanocrystalline, and amorphous thin films have been deposited by a wide variety of techniques, including PECVD [110], reactive sputtering [110–115], evaporation [116, 117], and sol–gel [118–120]. Titania is commonly used as a high-index layer in reflecting stacks, but materials developed for this application are not optimized for the low loss necessary for waveguide cores and loss numbers are not frequently reported.

Lithium niobate is the workhorse material for electro-optic modulation. The refractive index is ~2.2 in the wavelength range of interest, so thin films clad by oxide or polymer are candidates for strong confinement systems. Waveguides are usually patterned into lithium niobate by diffusion such that there is only a small index difference between core and cladding. Single crystals are grown at high temperature. Since this approach will be difficult to integrate into the CMOS back-end we focus on other, thin film, approaches here.

Several methods have been used to prepare thin film lithium niobate. High-quality epitaxial films with very low loss have been grown by sputtering [121], CVD [122], and liquid phase epitaxy [123]. Single crystal lithium niobate waveguides are grown at ~1000°C and are therefore incompatible with back-end CMOS processing. Polycrystalline thin films have been

sputter deposited onto a variety of substrates, including SiO_2 [124] and Si_3N_4 [125]. The substrate temperatures for better-quality films are in the 500–600°C range [125]. In some cases, the film quality has been improved by a post-deposition anneal at 600–650°C [126]. Losses as low as 2 dB/cm have been reported in polycrystalline films for 633-nm wavelength [126].

Other high-index insulating oxide ceramics that can be deposited in thin film form include the titanates ($BaTiO_3$, $SrTiO_3$, $PbTiO_3$), the zirconates, and combinations of the two [127]. Bulk and thin film materials have been employed in high dielectric constant, electro-optic, and piezo-electric devices [128].

11.3.1.6 III–V Semiconductors

There is a large body of work on III–V materials as waveguides because GaAs alloys are the basis for many successful semiconductor laser systems and, therefore, offer the possibility of monolithic integration with other III–V devices. Hybrid integration, in which prefabricated III–V devices are mounted on a host CMOS wafer [129, 130], for example, by bump-bonding, is outside the range of this review. The majority of the monolithic work has been on preparation of high electronic quality devices with low defect density for laser and detector applications [131, 132]. Waveguides do not need to meet these exacting standards.

GaAs has a band gap wavelength of ~870 nm and a high index of refraction (3.4) typical of semiconductors. It is, therefore, a candidate for microphotonic waveguiding at 1310 and 1550 nm. Alloying with AlAs lowers the bandgap wavelength and decreases the index, whereas alloying with InAs increases the wavelength and increases the index. In order to avoid excess loss due to free carrier absorption, the carrier density should be less than ~10^{17} cm^{-3} [133].

Optoelectronic-device-quality III–V materials have been prepared by a variety of techniques, including molecular beam epitaxy (MBE), liquid phase epitaxy, chemical beam epitaxy, and organometallic chemical vapor deposition (OMCVD). Device-quality materials can have very small optical absorption losses, less than 0.1 dB/cm [51]. The typical deposition temperature range for AlGaAs and GaAs devices prepared by OMCVD is 550–700°C. Higher temperatures give higher-quality material, but have deleterious effects on other parts of the device (e.g. interfaces). Another approach to waveguide preparation that permits deposition at temperatures that are consistent with CMOS processing is ‘Low Temperature’ (LT) GaAs [134]. LT III–V materials are grown by MBE at temperatures in the 200°C range. The deposited films are subsequently annealed for a brief period at higher temperature. They contain a small amount (~1%) of excess As that forms small precipitates [135] after annealing. LTG GaAs has low carrier density, implying low free carrier absorption.

In channel waveguides, the major loss mechanism is sidewall scattering due to residual roughness; therefore, efforts have been made to optimize processing to minimize roughness [43, 133, 136–139].

11.3.2 Organic and inorganic polymers

The highlights of polymers for integrated optics are: (i) low-cost fabrication due to simple fabrication techniques and low-temperature processing; (ii) low-loss coupling to glass fibers; (iii) easy scaling from lithographically defined thin film to formed waveguide coupler, applicability to CMOS due to low-temperature processing during fabrication. In addition, it is possible to vary the properties of polymers, for example, by adding ligands or altering the molecular weight.

Issues for polymers include thermal and chemical stability, glass transition or crystallization effects, optical losses and stability, processability, adhesion, material compatibility.

In the following, we review some properties and implementations of selected polymers. We have attempted to include examples of several important classes, including polyacrylates and polyimides as well as fluorinated materials, but it is not possible for a review of specific polymer materials to be comprehensive.

11.3.2.1 Acrylates

Polyacrylates are built from acrylate monomers that are esters which contain vinyl groups. Polymethylmethacrylate (PMMA) is a well-known photoresist material that is patterned by UV photoexposure and either chemical or ion beam etching. Material losses in PMMA are low in the visible (< 0.1 dB/cm at 633 nm), but can be significant at 1550 nm due to overtones of the C–H vibrational stretch. It is relatively easy to produce high-resolution patterns with smooth sidewalls in PMMA. As a reference, $3 \times 7\,\mu$m PMMA channel waveguides have been recently reported that have 0.08 dB/cm loss at 633 nm [138]. PMMA as used for photoresist applications has a relatively low glass transition temperature and cannot be processed above 80°C. Unfortunately, PMMA is not stable thermally – it goes through a glass transition temperature at only 80–100°C and, therefore, exhibits excess scattering after it has been through back-end CMOS-type thermal cycling.

Allied Signal has developed a class of optical polymers based on combinations of acrylate monomers/oligomers and various additives [141]. Upon photoexposure these monomers form highly crosslinked networks which exhibit low intrinsic absorption and scattering in the range from 400 to 1400 nm. By blending and copolymerizing selected monomers, the refractive index could be tailored from 1.3 to 1.6, allowing them to be used as both core and cladding. Intrinsic optical loss is 0.02 dB/cm at 840 nm, 0.2 dB/cm at 1300 nm, and 2 dB/cm at 1550 nm. These polymers have been estimated to be optically stable for years at 125°C. Fluorinated versions of these polymers have also been developed by Allied Signal for lower loss at 1550 nm [36, 76, 142, 143].

Polyguide is a proprietary acrylate polymer developed by Dupont for board and backplane level optical interconnect applications as part of the POLO and POINT programs funded by DARPA. [30, 144]. Waveguides are formed based on internal diffusion of high-mobility and

low-weight monomers. This process is light induced and can take place at temperatures in the range 15–45°C. Subsequent photo/thermal mixing and curing completes the formation of the waveguide. Optical loss of 0.35 dB/cm has been reported for 1300-nm wavelength; losses at 1550 nm are significantly higher. Extrapolated experimental data suggest a degradation of only 0.01 dB/cm in 1 year for continuous operation at 85°C.

11.3.2.2 Fluorinated acrylates

Fluorinated acrylates have been developed by Allied Signal for optical interconnects. Upon photochemical exposure, these monomer systems form highly crosslinked networks with very low loss of < 0.02 dB/cm at 840 nm and loss < 0.15 dB/cm over the range from 400 to 1500 nm. Thin films from 1 to 400 μm have been prepared by spin casting or slot coating, followed by photoexposure at room temperature. Waveguide structures have been fabricated using photoresistive overlayers by both mask photolithography and direct laser writing. Fluorination decreases the loss by an order of magnitude in the wavelength range from 900 to 2000 nm. These polymers are susceptible to oxygen interference in polymerization, more highly crosslinked polymers are less susceptible. Allied Signal's acrylate polymers have good thermal stability, degrading at the rate of $\sim 2 \times 10^{-7}$ dB/cm/h at 100°C , $\sim 1 \times 10^{-5}$ dB/cm/h at 150°C, and $\sim 3 \times 10^{-4}$ dB/cm/h at 200°C (an activation energy of 26.6 kcal/mole) at 840 nm.

11.3.2.3 Polyimides

The use of polyimides as optical waveguides has been the subject of several reviews [83, 145, 146]. Polyimides contain the imide group and have one of two basic forms. The first of these is a linear structure where the atoms of the imide group are part of a linear chain. The second is a heterocyclic structure where the imide group is part of a cyclic unit in the polymer chain. Aromatic cyclic polyimides are typical of most commercial polyimides including ULTEM (GE) and Kapton (Dupont). The index of refraction of optical polyimides is in the range from 1.52 to 1.65 with loss of order 0.5 dB/cm.

A collaborative effort between Honeywell and GE has developed polymer-based optical interconnects for MCM and backplane level integration [74, 147]. The waveguide structure consists of benzocyclobutane (BCB)/polyetherimide/BCB sandwich with the BCB as cladding. The index of the polyetherimide can be varied from 1.61 to 1.65 whereas the BCB has an index of 1.50–1.55 at 800 nm. Channel guide losses as low as 0.2 dB/cm have been reported [148]. Forty-five-degree end-mirrors formed by laser ablation have resulted in loss of 1 dB for each 90° bend of the optical path.

The incorporation of the hexafluoroisopropylidene group into polyimides reduces optical anisotropy that leads to scattering losses [145, 146], but these polymers tend to be less stable thermally and mechanically than polyimides, which include rigid rods and include biphenyl dianhydride. The rigid rod polyimides have higher optical loss due to absorption in charge transfer

complexes and scattering. It has been shown that heavy fluorination with CF_3 groups in all components of the polymer have reduced charge complex absorption. Fluorination also enhances solubility of polyimides, which can cause problems for multilayer fabrication. Overcoating a thermally cured layer with another layer exposes the first layer to solvent and frequently results in stress cracking. Fabrication of waveguides in polyimide has been carried out by electric field poling, photobleaching, selective diffusion [149], reactive ion etching, and direct laser writing. Unfortunately, for waveguide applications, the chromophores that are used to increase the refractive index in poling, photobleaching and diffusion are not stable at package assembly temperatures [150].

Fluorinated polyimides combined with a photosensitizing group have been developed by Buehler *et al.* [83]. Solubility is reduced in these materials after photochemical crosslinking; therefore, multilayers are feasible. Crosslinking is accomplished with 300 mJ/cm^2 of 365 nm excitation for a 10-μm thick film. Absorption loss is about 0.5 dB/cm at 800 nm for 6FDA/BAAF/photosensitizer after curing at 300°C. Channel waveguides have been fabricated by the following process: the photosensitive polyimide is spin-coated onto an appropriate substrate (which may be a previously deposited polyimide layer). The new layer is soft-cured to remove solvent, exposed through a photomask, and then etched using solvent developers into a rib waveguide. The waveguide is baked at more than 300–350°C. One can make buried channel guides by etching the under-cladding layer and backfilling with higher index polymer or ridge waveguides by etching the core layer itself and then planarizing with the over-cladding layer. High-quality channel waveguides with line widths of 4–5 μm have been demonstrated.

NTT [73] has proposed and demonstrated an optical MCM interconnect based on fluorinated polyimides. The waveguide layer is fabricated on an electrical MCM-type copper/polyimide multilayer substrate. Optical polyimide waveguide layers consisting of a 37.5-μm cladding and a 50-μm thick core were cured at 300–350°C after being spin coated on the substrate. Ridge waveguides were formed by reactive ion etching. Loss in linear waveguides was less than 0.4 dB/cm. Chip-to-chip interconnection, coupling between waveguides, and coupling to flip-chip bonded photodiodes is achieved using a total internal reflection (TIR) mirror fabricated at the end of each waveguide. The TIR mirror was fabricated by reactive ion etching while tilting the substrate with respect to the cathode. The excess loss at the mirror was less than 1.5 dB at 1.3 μm.

11.3.2.4 Polysiloxane

Polysiloxane waveguides have been developed and characterized at NTT [75]. The core polymer is prepared from deuterated and non-deuterated phenylsilyl chloride monomers. Fabrication was as follows: cladding and core polymers, which differed only in additional phenyl groups were spin coated in an organic solvent onto the substrate. (Index of core and cladding differed by 0.3%.) Each polymer layer was baked at 150°C. Channel waveguide masks were formed by standard photolithography. The core ridges were formed by reactive ion etching until the

surface of the undercladding layer was exposed. An overcladding layer was then spun on. The waveguide core was about 8 μm wide and 8 μm high. Straight waveguide loss was about 0.17 dB/cm at 1.3 μm. There was no additional loss after heat treatment in air at 200°C for 30 min, 1000 h at 120°C, or 1000 h at 90% relative humidity and 75°C. Mirrors were not fabricated.

Silicon-backbone polymers have also recently been investigated by Brown and coworkers [79]. They spun 1–2-μm thick poly(phenylsilsesquioxane) (PPSQ) films on silicon oxide and found an average loss of only 0.16 dB/cm at 633 nm. The index of refraction, measured in waveguide configuration, was 1.55. The thermal stability appeared to be excellent with < 0.001 change in index for temperatures up to 400°C. Prior work on similar materials for potential application as interlayer dielectric [151] indicates that this material is readily filterable, suitable for spin application, and patternable with a CF_4/O_2 reactive ion etch. This group has also reported on poly(cyclohexylsilyne) thin film optical waveguides [78]. Measurements of bulk absorption indicate loss of < 0.04 dB/cm. Loss in 2-μm-thick waveguides is closer to 0.5–1 dB/cm. The authors suggest that surface scattering is responsible for the discrepancy. The authors later reported that they felt that this class of materials demonstrated poor thermal and mechanical stability [79].

A siloxane-based epoxy polymer has recently been developed by Polyset Inc. Epoxy monomer/solvent liquids can be easily spun into 0.5–5-μm-thick films that can sensitized for UV curing or cured by heat treatment at < 200°C. Because of the siloxane backbone, these epoxies are stable to over 350°C. The index can be varied by control of side groups off the backbone. The refractive index of a typical siloxane epoxy polymer described by Ponoth *et al.* [49] is 1.52, thus silicon oxide can be used as the cladding. Spun-on films have good adhesion to both oxide and xerogel claddings and have losses of less than 0.5 dB/cm at 650 and 830 nm [49].

11.3.2.5 Benzocyclobutane

Benzocyclobutane (BCB)-based polymers have many characteristics that are desirable for optical waveguides. BCBs were originally developed for dielectric applications, but they have suitable characteristics for waveguides as well [152]. They have excellent planarization, low moisture uptake, and thermal stability to 350°C. They also adhere well to other materials and to themselves. This class of polymers exhibits a wide range of refractive indices from 1.54 to 1.62 at 835 nm [152]. Intrinsic optical loss is low (0.04 dB/cm at 1300 nm) and slab waveguide loss of 0.2 dB/cm has been reported [152]. Recently, photodefinable BCBs have been developed [68]. Kane *et al.* [70, 153, 154] reported the fabrication of waveguides. They first spin-coated a 10-μm layer of non-photodefinable BCB, which was thermally cured in vacuum at temperatures up to 250°C. The photodefinable core layer was then spun on and soft-cured at 80°C. The waveguides were patterned using a contact mask and exposure of 6 J/cm^2. The unexposed regions are then washed away. The ridge waveguides were then cured at 250°C. Loss in an 8×8-μm ridge waveguide was ~0.9 dB/cm at 830 nm and 0.81 dB/cm at 1300 nm.

11.3.2.6 Polynorbornene

Polymers based on cyclic olefins (polynorbornene) have recently been proposed for optical waveguide applications. Early work on this system was aimed at a variety of applications including labware and packaging [155] as well as low-k dielectrics for integrated circuits [154]. The intrinsic properties of polynorbornenes, developed and reported by BF Goodrich [156], include low transmission loss (< 0.02 dB/cm at 820 nm), low birefringence [$\Delta n < 10^{-5}$ (in plane), $\Delta n < 10^{-3}$ (out of plane)], good long-term thermal stability at operating temperatures, high glass transition temperature (280°C), and low moisture take-up [157]. Extended heat treatment causes degradation of transmission with loss of ~0.1 dB/cm after 2000 h at 125°C, but this is still very acceptable for on-chip and chip-to-chip waveguide applications. Although waveguides shaped by RIE and laser ablation are possible, BF Goodrich has focused on gratings and waveguides fabricated by molding techniques.

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Chapter 12
Reliability

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Abstract

Reliabilty in a given thing or process means that this thing or process must be capable of performing its function throughout its intended useful life. This chapter discusses the reliability of the interlayer dielectric materials/films used as the insulating layers between electrically conducting metallic interconnections that are formed in modern integrated circuits using a multilevel interconnection scheme. It emphasizes all types of failures and knowing the causes that affect the usefulness and the intended life, focuses on identifying and eliminating these causes, and the modes of valuation and prediction of the useful life of the interlayer dielectric and thus of the device and/or circuit.

12.1 Reliability

Reliability in a given thing or process means that this thing or process must be capable of performing its function throughout its intended useful life. Failure to provide the function is a lack of reliability. Note the use of the words ‘intended’ and ‘useful life’. Whenever we make something, based on our prior knowledge we predict the useful life of this thing. Our experience has, however, shown that invariably this is not true. The real useful life can only be determined in actual use. The times required to examine the actual-use-failure are invariably large. Thus, it is useful to simulate the actual use. To simulate the actual use we then devise conditions to test the thing and draw relations between accelerated use conditions and actual conditions to predict the useful life. That, then, becomes a limit to our intended useful life.

In this chapter, we are interested in the discussion of the reliability of the metallization schemes, particularly the interlayer dielectric (ILD) materials and films, for devices, circuits, and packages and in knowing (1) the causes that affect the usefulness and the intended life, (2) the methods and concepts that will minimize or eliminate the failure modes and enhance the usefulness and the intended life or the reliability, and (3) how to evaluate the usefulness of a given ILD scheme and its intended life. We are concerned with all types of failures, their detection,

understanding the cause, and their elimination. Failures related to the ILD can be grouped in two major categories: (i) those inherently related to the dielectric itself and (ii) those that occur in the neighboring metal layer but are induced by the dielectric itself. Note that besides those reliability issues that can be related to all dielectrics, there are specific issues associated with (i) inorganic, (ii) organic, (iii) porous, and (iv) mixed organic–inorganic dielectric materials. They are related to the ILD materials properties as discussed in Chapter 2 and we will only emphasize them once again in this chapter.

This chapter is organized accordingly. First, we shall discuss the known causes of ILD and ILD-related failures. This is followed by the discussion of the mechanisms of such failures. How to relate and evaluate the reliability in such cases, methods to avoid such failures, and how to improve the reliability will be discussed towards the end. It must be pointed out that, in this chapter, our discussion is limited to the reliability of the ILD and ILD-related effects. Only related metallization failures are covered in this chapter.

12.2 Known ILD failure modes

There are a large number of failure modes related to the interconnect-metallization and the interlayer dielectric films. Much more emphasis has been given, in the past, to metallization-related effects than to those related to the ILD itself. Perhaps the simplicity of processing and the properties of deposited SiO_2 films, which as our experience has shown were practically failure-proof, did not cause much concern about the reliability of SiO_2-ILD. The film was deposited in high quality by CVD, especially PECVD, at a thickness generally in the range of 0.3 to over 1 μm. Deposited films, however, showed some unwanted behavior, related to stoichiometry, stress, pinhole density, etc. only at thicknesses less than 0.2 μm [1]. Any observed reliability concerns were mostly process-related and were the result of poor control or design of the deposition process and other times due to a lack of 100% conformal deposition in very high aspect ratio features. Process-related failures, if any, could be grouped into the following modes:

1. particulate generation;
2. misalignment during lithography;
3. thinning and cracking of the ILD over steps and at inner corners and width reduction at corners (over-etching, non-uniform deposition);
4. poor adhesion resulting from improper cleaning prior to ILD deposition, due to predeposition contamination in the deposition chamber, and/or due to a lack of interfacial bonding at the metal/ILD interfaces;
5. poor adhesion due to high-stress conditions that result from poor control of the deposition or excessive heat treatments;
6. poor control of the stoichiometry and density of the deposition films;
7. incomplete etching of the ILD over the metal causing high resistance between two levels of the metal;

8. interlevel and intralevel shorts due to pin holes or cracks in the ILD or due to protrusions on the underlying metal or on the ILD surface;
9. mobile ion contamination;
10. premature dielectric breakdown associated with the applied electric field, time-dependent variations in the electric field, or rise in temperature that lowers the breakdown field;
11. time-dependent dielectric breakdown, cyclic fatigue; and
12. excessive exposure to charged-environments leading to charge-damage to ILD.

Two major changes have occurred in the applications of ILD films: (i) chemical mechanical planarization (CMP) technologies are used to planarize ILD films leading to an elimination of the failure-mode #3 (listed above), because the ILD is deposited on flat surface and (ii) Al films are being replaced with Cu films. In addition, there is a thrust to replace SiO_2 films with a low dielectric constant (low-κ) films to achieve lower RC time constant and thus lower signal transmission delays. All these changes have introduced additional reliability concerns, namely:

1. scratching of the dielectric surface, leading to a localized dielectric thinning and to cross-scratch-centers that may become electric hot-points of high-field intensities after metal deposition;
2. adsorption, absorption, and permeation of the slurry medium (generally water) and chemicals on and in the ILD exposed to CMP;
3. abrasive inclusions in the ILD;
4. when metal is polished on top of the ILD, metal inclusion in the ILD is of concern;
5. localized stressed on top dielectric layers near the surface that may also retain slurry chemicals/liquids;
6. diffusion of Cu species, thermally or electrically induced, in the ILD leading to enhanced leakages and, therefore, to the requirement of a diffusion barrier that also must be removed by CMP form non-functional surfaces;
7. failure related to adhesion of the Cu to ILD, requiring that the diffusion barrier must also act as an adhesion promoter; and
8. the use of low-κ ILD raises several other reliability concerns, which are specific to low-κ materials, as discussed below.

As noted, most of these failure modes are process (e.g. deposition, CMP, etching, annealing, cleaning, and process environment) related and have been or can be studied and eliminated. However, there are others that are related to the ILD materials characteristics (e.g. adhesion to Cu, stress, diffusion in ILD of metal or of the process species, e.g. water or a gas, and chemical interaction) and the process or use temperature.

12.2.1 Reliability concerns associated with low-κ dielectrics

Low-κ dielectrics are polymers with or without fluorine, polymers with or without voids, polymers mixed with inorganic dielectrics, inorganic dielectrics with F and/or C (e.g. C–SiO_2,

F–SiO_2), porous inorganic dielectrics, and some combination of more than one of these options. All these options raise several reliability concerns:

1. Very low thermal conductivities of these low-κ materials may cause excessive temperature rise in the material and surroundings. Significant increases in the ILD film temperature may lead to early failure due to lowered field strength at higher temperatures.
2. Generally low glass-transition temperatures of many of these materials raise concern of the mechanical stability.
3. Adhesion to polymers, especially to fluorinated polymers, has been poor particularly with Al and even with Cu and some known refractory metals used as diffusion barrier.
4. Degassing of these materials.
5. Molecular weight and/or density variation across the wafer surface to which these low-κ materials are applied and across the thickness of the deposited layer.
6. Compositional stabilities of the fluorinated and carbonaceous dielectrics (generally SiO_2).
7. Stability of poor size distribution and density.
8. Gases, if any, trapped in the pores.
9. Mechanical stability of all low-κ materials especially during CMP and stress–temperature hysteresis.
10. Reproducibility of the film composition and properties in actual manufacturing and use environments. Although this concern applies to all ILD materials, it is iterated here because of our relatively poorer experience with low-κ materials.
11. Recent studies of the dielectric's electrical stability, studied using metal–insulator–semiconductor capacitators, have shown (i) certain polarization effects under bias (in a bias–temperature–stress test) and (ii) metal in-diffusion that varies from polymer to polymer [2–4].
12. Whereas SiO_2-based ILD materials were, in general, insensitive (against chemical attack) to most organic solvents and photoresists, polymers may not have this insensitivity.

12.2.2 Impact of ILD properties on metal's reliability

Aluminum was, practically, an ideal metal for use on SiO_2 used as an ILD. It adhered very well and formed a self-forming interfacial barrier (of Al Si_xO_y) at the Al–SiO_2 interface such that no further interaction occurred between the two materials. Problems with Al were not related to the use of SiO_2 as an ILD. The use of SiO_2 as an ILD created problems with W metallization, because of the lack of adhesion between SiO_2 and W. This led to the use of Ti/TiN on SiO_2 as an adhesion promoter and also as electromigration-lifetime enhancer and as a antireflection coating (ARC) on Al. The recent use of copper caused concerns not only related to the adhesion on the ILD (SiO_2 or a low-κ material) but also related to diffusion in the ILD that eventually, then, may cause electrical leakage [5]. TaN_x films have been used to provide both the adhesion and diffusion barrier properties. A SiN_x film is used intermittently to insure a barrier against Cu migration.

It is, thus, apparent that the ILD material plays an important role in the design of interconnect-structure and optimization of the metal's reliability. Besides the concerns related to the control of the dielectric properties (which may affect the metal's stability/reliability) during deposition, one worries about the effect of processing, especially CMP and dry-etching, on the properties of the dielectric–metal interface and thus of the final interconnect structures. Lower thermal conductivities of the ILD may lead to increased temperatures in metal and thus enhanced reactivity and electromigration. ILDs with low glass-transition temperatures generally lead to a flow and distortion and subsequently to a failure in metal interconnections. Also there are worries about the dielectric–metal interactions that increase the metal's resistance and leakage in the dielectric. PECVD-SiO_2 has been nearly an ideal dielectric. Future low-κ materials must be carefully designed to replace SiO_2.

12.3 Sources of the dielectric failures

All these ILD failure modes and others can be grouped in the following general source categories:

1. deposition;
2. pattern definition and generation and CMP;
3. fundamental materials' stability (structure, density, molecular weight, T_g, etc.) related problems;
4. liquid/gas permeation and/or absorption and adsorption (interaction with surroundings);
5. dielectric/metal adhesion and interfacial stabilities (including interdiffusion); and
6. stress.

12.3.1 Deposition-related problems

Impurities in the film, adhesion, stress, cracks, ion-damage-related effects, stoichiometry and molecular weight variations, step coverage, and thickness non-uniformity are associated with deposition. All of these problems can be solved by tailoring the deposition process. *Impurities* in the films affect not only the electrical, mechanical, and chemical properties, but also, by their diffusion and chemical interaction with the surroundings (metal films), affect the performance of the surrounding materials. Incorporation of the impurities in films can be practically eliminated by the use of high-purity evaporation and sputtering sources, high-purity chemical precursors for CVD, high-purity spin-on chemicals for spin-on deposits, high vacuum or excellent predeposition background pressure, pure gases, clean surfaces, and oil-free vacuum systems with separate deposition and load chambers. The film deposition rate (or spin rate followed by generally required anneals) also plays an important role in determining the concentration of impurities in the film. The fraction of the impurity species trapped in the film is inversely related to the film deposition rate. Much of the present-day deposition equipment has optimized the deposition

rate to minimize the contamination from the vapor phase. By isolating the deposition chamber from the loading and unloading chamber, the deposition environment is maintained in a very high purity state. Appropriate maintenance and occasional cleaning of the deposition chamber are necessary to avoid contamination and particulates resulting from the pile up of the deposits on the inner fixtures of the chamber.

Adhesion of the films, as discussed in Chapter 2, is promoted by (i) inducing strong atom–atom bonding (between the film and substrate) within the interfacial region, (ii) reducing the stresses to the lowest levels, (iii) the absence of easy deformation or fracture modes such as those caused by surface unevenness and particulates, and (iv) the absence of long-term degradation modes such as those that may happen due to exposure to moisture and air. Surface cleanliness and localized deposit–surface interaction will improve localized atom–atom bonding.

Stress in the film is mainly responsible for the mechanical failures such as cracking, peeling, and curling of the films. In Chapter 2, the origin of stress during deposition and subsequent processing (generally the thermal treatments) were discussed. Although the intrinsic stress associated with deposition parameters can be minimized, the thermal stress, stress associated with volume change, and introduction of impurities and defects during subsequent processing, and that associated with a deposition of a covering layer of metal are difficult to eliminate. The most important among these stress contributors is the thermal stress, which can only be eliminated by choosing materials with matched thermal expansion coefficients or by minimizing or eliminating the temperature excursions the films see during and after deposition.

Cracks in the deposits are the result of poor adhesion, the presence of particulates or unevenness, or stresses in the film. A control of these parameters will eliminate cracks in practically all cases. Cracks may, however, result following a heat treatment or CMP of the films; this is usually due to a volume change or a chemical interaction. Polymer films are generally less prone to cracking. Insulator films deposited by CVD and sputtering or spin-on-glasses have often been found to crack when subjected to a thermal cycle. Thermal mismatch between the substrate or the metal and insulator films, hillock growth in metal film, and densification and evolution of gaseous species, such as hydrogenous species in CVD films and solvent in spin-on-glasses, are the cause.

Sputtering, plasma-enhanced, and ion-assisted depositions expose the substrate and the depositing film to ion and/or electron bombardments. Evaporation using the e-gun also leads to electron and X-ray exposure of the substrate and the film. Such ion, electron, and X-ray exposures cause damage to the material and changes in properties. Generally, such damages are not severe and can be annealed out at low temperatures in the range of 300–450°C.

Step coverage is another serious ILD-deposition-related problem for deposition on patterned metal interconnections. For ILD deposited by CVD methods or spin-on techniques, this is not a serious issue. Also now, in most cases, ILD is deposited on a planarized surface (e.g. W or copper CMP followed by ILD deposition), making the step-coverage issue for the ILD deposition a mute one.

12.3.2 Pattern definition and generation

With the use of CMP, ILD surfaces are planarized prior to pattern generation. This has led to a significant improvement in the reliability of the ILDs and the metal interconnections that ILDs isolate.

There are several etching-related problems that cause failures: (i) etch rate and film thickness variations across the wafer surface requiring an overetch and high selectivity; (ii) an isotropic component of the etch leading to undercutting the photoresist mask and thus an enhancement in the via dimension or in the line width; (iii) loading and microloading effects associated with etching more than one wafer at the same time and etching patterns of variable dimensions on the same wafer; (iv) redeposition of materials; and (v) corrosion of the underlying metal and associated with the gases trapped on etched surfaces. Plasma and reactive ion etchings are two of the least-understood processes and are, therefore, poorly controlled processes. A careful determination of the optimum process to etch and a tight control on this process to provide wafer-to-wafer and run-to-run reliability in etching are thus necessary to avoid many of the above-mentioned problems. A post-etching treatment, *in situ* in the etch chamber, must be developed to remove the trapped etch species that may be the cause of corrosion-related failures in the metal.

12.3.3 CMP-related issues

In most modern processing of the integrated circuits, CMP is either used to planarize the deposit dielectric or to define the metal using a damascene-CMP approach [6]. In the latter the deposited metal is polished until the dielectric surface is cleared. Even the use of a reproducible and reliable CMP process, as mentioned in Section 12.1, leads to specific ILD reliability concerns related to metal diffusion, scratching, solvent/slurry adsorption, absorption, and/or permeation, the abrasive inbedding on the surface, and induced stresses/strains. These reliability concerns are heightened in polymer and porous dielectrics, which have lower mechanical strengths. A careful evaluation of such effects and subsequent development of elimination techniques is essential. For flat and single material surfaces one can use a touch-up chemical etch technique to take care of many of these issues. For multi-material surfaces, such as those where CMP is carried out to clear ILD from metal and adjoining surfaces, such chemical treatments may not be feasible. A post-CMP clean followed by a low-temperature inert-ambient anneal may eliminate concerns related to solvent entrapment and surface stresses/strains. The best choice is to optimize CMP processes to avoid all or most of these concerns.

12.3.4 Interaction with the surroundings

Many ILD-related failures occur from the interactions of the ILD with the surroundings, namely the underlying semiconductor and contact materials, underlying or overlying metallic films, and

the environment. Some of these interactions are aided by the applied electric field. Most of them, however, are thermally activated and diffusion controlled. One can define these interactions to be caused by (in terms of the reliability definitions [7]) voltage and electrostatic discharge, temperature, humidity, chemicals, and/or reactive gases that may be present in the ambient or evolved from the surrounding materials during stressing (exercising the ILD). The typical practice of the reliability evaluations followed by the failure analyses and necessary materials and/or process modifications are then needed to locate the problems and correct them.

Typically, dielectrics are evaluated by subjecting them to a so-called bias–temperature stressing (BTS). A metal–dielectric–semiconductor or a metal–dielectric–metal capacitor is used for capacitance–voltage (*C–V*) or current–voltage (*I–V*) measurements, respectively, although the first type can also be used for *I–V* measurements. These structures are subjected to increasing biases and temperatures and exercised under such conditions for various times followed by measurements (i) after cool-down to room temperature or (ii) at temperature measurements in case of the *I–V* tests. For reliability evaluations a large number of such randomly on-surface distributed devices on a wafer (and then large number of wafers) are tested and data statistically analyzed.

One must emphasize that newer dielectric materials (e.g. polymers, C- and/or F-doped SiO_2, porous materials) are very different from the classical SiO_2-ILD. Thus, the interpretation and the understanding of the data on such materials may not have parallel in SiO_2-based devices and, therefore, should be carefully generated.

12.4 Failure detection, failure analyses, and reliability measurements

Classically, thin-dielectric films have been tested to detect failures (i) in as-deposited condition, (ii) after a thermal-annealing treatment as prescribed by a study of materials properties–anneal temperature–time relationships, and finally (iii) under a bias–temperature (with or without intentionally induced humidity or reactive environments) – stressing conditions. Table 12.1 lists the most common and useful characterization/test techniques, many of which are discussed in Chapter 3. Note that microscopic examination of the film surface, bulk of the film, or the metal–ILD film interface is not listed in Table 12.1. Optical microscopic/visual examinations are essential in detecting surface planarity, cracking, or uneven growths after deposition or after anneals. Transmission electron microscopy (TEM) examinations (planar or cross-sectional) are essential to detect these small causes of failures and materials 'changes that affect the ILD performance. Coupled with energy-dispersive X-ray spectroscopy (EDS) and electron diffraction studies, TEM methods provide an excellent means of locating, sizing, and analyzing the particulates, second phases, precipitates, etc. in the ILD films. Although TEM analyses are very powerful in providing the information, it is very time consuming and analyzes a very small area/volume of the film under investigation and, therefore, should be used as a tool to elucidate failure–cause relationships.

Table 12.1 Thin ILD film properties and characterization techniques and test conditions

Property	Methodology	Test conditions
Dielectric constant	Metal–insulator–metal (MIM) plate capacitance measurements	1 MHz at RT in an inert ambient
Charges/traps in the dielectric (metal or mobile ion diffusions in the dielectric)	Metal–Insulator–semiconductor (MIS) plate capacitance	1 MHz, *C–V* measurements with or without bias temperature aging in an intert ambient
	MIS-triangular voltage sweep (TVS) measurements	Inert ambient
Refractive index η_{TM} (out of plane) η_{TE} (in plane) (birefringence $\Delta\eta = \eta_{TE} - \eta_{TM}$)	Equipment example: Metricon 2010 prism coupler using $X = 632.8$ nm	Ambient environment
Thermal stress and glass transition temperature (T_g)	Stress measuring tools both for room temperature and at temperature measurements	Inert or atmospheric environments
In-plane coefficient of thermal expansion and T_g	Thermomechanical analyzer	Under inert environment
Young's modulus and elongation at break	Micro-tensile tester, nano-indentor	Inert or regular environment
Dielectric stability as a function of temperature	Differential calorometry post-anneal analysis	
Water pick up or loss	Nuclear reaction analysis (NRA) for H_2, weight measurement, FTIR measurements	Regular environment
Dielectric breakdown	Current–voltage measurements at room temperature, also as a function of temperature and of time at a temperature	Dry environments
Metal–dielectric interactions	RBS, SIMS, metal resistance measurements	
Porosity	X-ray diffraction, NRA, RBS	
Chemical bonds, radicals, and groups	FTIR, XPS, Auger	Dry environment

12.4.1 Accelerated failure analyses

Many of the causes of the device/circuit failures are related to materials such as an ILD or a metal. Normally, an optimized materials preparation leads to excellent films with, generally, not much concern about causing a failure. However, the same may not be true at higher temperatures and under high electrical bias conditions. Thus, there has been a practice of subjecting dielectric films, with or without being in contact with the metal, to increasingly high temperatures and/or increasingly high electrical biases and then measuring the film's performance and comparing them with the performance of the as-deposited films and with that of an idealized ILD film. By measuring certain properties as a function of temperature and/or bias, one can derive a functional relationship between those properties and temperature (e.g. an Arrhenius relationship) or electrical field (e.g. current–voltage relationships supporting various mechanisms of conduction, as described in Chapter 2). Such tests are called *accelerated tests* that provide a relationship, which, in turn, provide a means to predict failure at operating conditions.

Typical accelerated tests (carried out on a large number of samples) use temperatures in the range of room temperature to about 300°C, although in certain cases higher temperatures can be used. Similarly, in accelerated bias tests, biases above the normal device/circuit operating biases but below the breakdown bias (see Chapter 2) of the ILD are preferred. Bias–temperature stressing during *C–V* measurements and *I–V* tests (see Chapter 2) are most commonly used for qualifying the dielectric materials.

Detailed discussion of the statistical analyses and reliability models is out of scope of this chapter. References [7–15] are excellent in providing a variety of approaches and models. We provide a brief discussion of the time-proven models in the next section. Here, we list a few time-transformation models that are used to enable transformation of the results of the accelerated tests (at those elevated conditions) to a normal device/circuit/material operating conditions. Accordingly, Kuo *et al*. [7] (based on the summary analyses of Tobias and Trindada [8]) have presented several functional relationships between the accelerated, represented by the subscript 2, and normal conditions, represented by the subscript 1, and η as the time transformation factor or the acceleration factor:

1. the time to failure
   $t_1 = \eta t_2$,
2. the cumulative distribution
   $F_1(t) = F_2(t/\eta)$,
3. the probability density function
   $f_1(t) = 1/\eta\, f_2(t/\eta)$,
4. the hazard rate function

$$h_1(t) = \frac{f_1(t)}{1 - F_1(t)} = \frac{1}{\eta} h_2(t/\eta),$$

5. the reliability

$R_1(t) = R_2(t/\eta)$.

For temperature only as the acceleration factor one assumes an Arrenius-type relationship because most metallurgical, chemical, and physical phenomena are known to follow this relationship. Assuming an Arrhenius-type temperature dependence, it can be shown that

$$\eta_T = \frac{t_1}{t_2} = \exp\left[\frac{Q}{R}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \tag{1}$$

where Q is the activation energy obtained from Arrhenius dependence and is given in calories per mole, R is the gas constant, and T is the temperature.

Similarly, the most widely used voltage acceleration factor is assumed to be given as [7]

$$\eta_V = \exp[\beta \Delta V] \tag{2}$$

where ΔV = stress condition internal voltage − normal internal voltage. Note, that β can be estimated by using two different stressed condition internal voltages. Such analysis help us in determining η_T or η_V. Larger the number of samplings more accurate are these factors, leading to more reliable estimates for the normal operating conditions.

One must determine or make assumptions for such acceleration factors to establish the effect of temperature, voltage, current or current density, thermal shock and thermal cycling, humidity, mechanical shock, etc. on the device/circuit reliability and relationships of these to the dielectric reliability. From materials point of view such assumptions, based on our scientific knowledge of studying crystalline/ordered materials, may not hold for amorphous and highly defected interlayer dielectric materials and for polymers or voided materials. Experimental evaluations on larger number of identical samples thus become very essential to predict reliability and to generate models that provide a foundation for understanding

12.5 Reliability concepts and evaluations

12.5.1 Yield

Reliability of a given product is related both to the process yield and the useful life. The yield, Y, in percentage can be defined as the ratio of fully working products, N_E, obtained at the end of the processing to those originally introduced, N_I, at the initiation of the processing:

$$Y = \frac{N_E}{N_I} \times 100 \tag{3}$$

In microelectronics, three types of yields are defined: (i) the percentage of wafers that survive the process; (ii) the percentage of functional circuits (chips) after probing; and (iii) the percentage

of packaged parts that can be sold. If one defines these as Y_W, Y_P, Y_{PP}, then the total yield, Y, is given as

$$Y = Y_W \cdot Y_P \cdot Y_{PP} \tag{4}$$

Note that Y_W and Y_P are related to chip fabrication processes, whereas Y_{PP} is related to packaging methods. The process yield, Y_W, is related to several factors such as wafer breakage, process changes, number of process steps, equipment malfunction, and operator errors. The process yield, Y_P, is related to materials property changes, defects, accidental burn-outs during probing, wafer diameter, and the chip area. The greater the number of processing steps, the lower is the yield. The larger the wafer diameter and the smaller the chip size, the better is the yield. The last two factors are related to the defect distribution, whereas decrease in yield with increasing process steps is related to the finite probability of a lower than 100% yield after each process step. The effect of metallization and ILD-related failures is incorporated in Y_P and also in Y_{PP}. It is difficult to estimate the yield loss associated to metallization and/or ILD unless (i) the devices and circuits are tested after each metallization and/or ILD step, and pre- and post-ILD and metallization yields are compared and (ii) the failure at the probe level (of the completed chips) is diagnosed to be associated with the ILD and/or metallization.

In any attempt to model the yield based on defects, one must assume a defect density distribution behavior. Several models have been proposed in the literature. Some of the simpler models are summarized in Table 12.2, where $f(D)$ is the normalized defect density distribution function, D_0 is the density of defects, A is the chip area, $\delta(d)$ is the delta function, $\Gamma(\alpha)$ is the gamma function, and α and β are the two distribution parameters. Figure 12.1 shows a comparison of the various models (Parks, H.G., private communication). Only the Seeds–Price model [17] predicts yields that are considerably higher than others.

Table 12.2 Models of defect and yield

$f(D)$	Yield	Reference
Delta function $F(D) = \delta(D)$	$Y = e^{-AD_0}$	[16]
Triangular distribution $F(D) = D/D_0$ for $0 \leq D \leq D_0$ $f(D) = (2/D_0) - (D/D_0^2)$ for $D_0 \leq D \leq 2D_0$	$Y = [(1 - e^{-AD_0})/AD_0]^2$	[16]
Expotential distribution $f(D) = (1/D_0 \exp(-D/D_0)$	$Y = 1/(1 + AD_0)$	[17]
Gamma distribution $f(D) = D^{\alpha-1}\exp(D/\beta)/\Gamma(\alpha)\beta^{\alpha}$	$Y = 1/(1+A\beta)^{\alpha}$	[18]

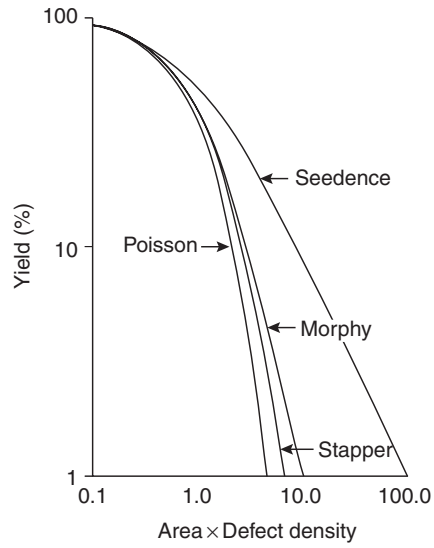

Fig. 12.1 A comparison of the yield obtained using different defect distribution functions (see Table 12.2). From Parks [19].

There are a variety of defects with different mechanisms for their generation and effect on the yield and reliability. Each defect could be treated independently by using its own gamma yield function (see Table 12.2)

$$Y_n = \frac{1}{(1 + A\beta_n)^{\alpha_n}} \tag{5}$$

where Y_n now represents the yield for nth type of defect and α_n and β_n are the distribution parameters of this defect, so that $\alpha_n\beta_n = D_{\text{on}} \cdot \mathrm{D}_{\text{on}}$ is the defect density of this defect. The overall yield, Y, is then given by the product of all the yields for all defects:

$$Y = \prod_{n=1}^{N}, \quad Y_n = \prod_{n=1}^{n} (1 + A\beta_n)^{-\alpha_n} \tag{6}$$

Finally, it should be pointed out that in at least some cases there is a radial dependence of occurrence of a defect on a wafer [19].

Figure 13.2 shows one example of the fabrication yield and defect density as a function of the time. It is clear that as the defect density decreased yield improved [19].

12.5.2 Reliability

In practice, reliability is determined by calculating the number of failures as a function of time in actual use. These data are then used to generate failure (distribution curves) frequency or

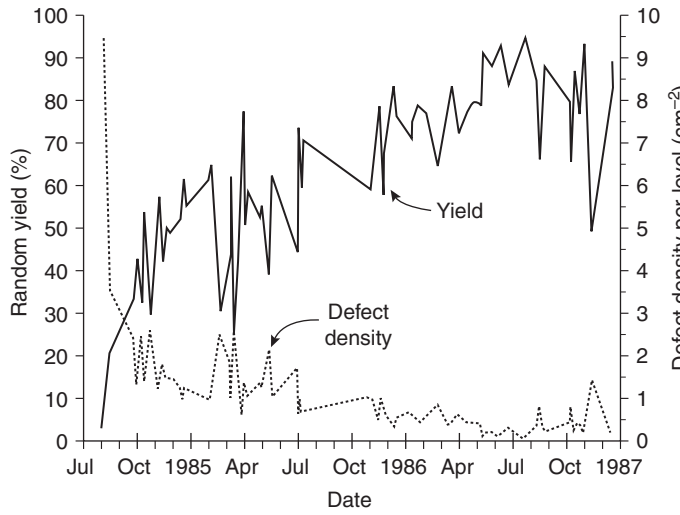

Fig. 12.2 Experimentally determined yield-defect relationships in a fabrication line. From Parks [19].

cumulative. Such distributions are then modeled mathematically assuming a distribution function, for example, an expotential function [20, 21]. Here we introduce some functions used in evaluating reliability.

A cumulative distribution function, $F(t)$, is given the following properties, defining an occurrence of a failure in time, t:

$$\begin{aligned} &F(t) = 0 \qquad t < 0 \\ &F(t) = 1 \qquad t \to \infty \\ &0 \leqslant F(t) \leqslant F(t^1) \quad 0 \leqslant t \leqslant t^1 \end{aligned} \tag{7}$$

A probability distribution function, $f(t)$, where $f(t)\,\mathrm{d}t$ is the fraction of failure occurrences in time, $\mathrm{d}t$, is defined as

$$f(t) = \frac{\mathrm{d}F(t)}{\mathrm{d}t} \tag{8}$$

that is,

$$F(t) = \int_0^t f(y)\,\mathrm{d}y \tag{9}$$

A reliability function, $R(t)$, is simply equal to $[1 - F(t)]$ and defines that the product is still working up to time, t.

Instantaneous failure rate, $\lambda(t)$, at time, t, is defined as

$$\lambda(t) = -\frac{1}{R(t)}\frac{\mathrm{d}R(t)}{\mathrm{d}t} \tag{10}$$

Table 12.3 Commonly used reliability distribution functions[a]

Function	Distribution
Exponential function where $\lambda_0 =$ constant	$R(t) = \exp(-\lambda_0 t)$
Weibull function where γ and β are constants	$R(t) = \exp[-(1/\gamma)^{\beta}]$
Log-normal function where $y = (\ln t - \ln t_{50})/\sigma$, $\sigma = \ln t_{50} - \ln t_{16}$ t_{50} and t_{16} represent time when 50%, and 15.866% of the devices are failed, respectively.	$R(t) = 1-(1/2)(t\,\mathrm{erf}\,y)$

[a]Hines and Montgomery [20] and Bertram [21].

and mean time to failure, MTF, is defined as

$$\mathrm{MTF} = \int_0^{\infty} tf(t)\,\mathrm{d}t \tag{11}$$

Table 12.3 lists commonly used distribution functions. For further details see Hines and Montgomery [20] and Bertram [21].

12.5.3 Reliability evaluations

The distributions discussed in the preceding section help in understanding the observed behavior in the yield and reliability and in predicting future behavior. However, the key to such understanding and predicting lies in obtaining the experimental data. As previously mentioned, many materials failures are associated with the poor control or understanding of the fabrication processes and random events, which cause defects and loss of the product. A constant vigil is required to improve these failure modes, including the use of particle-free processes. There are other failure modes, which in normal uses may not be detectable in a reasonable time but can be accelerated by the use of increased temperature, pressure, or environmental controls such as increased humidity. As mentioned earlier, by precise control of the accelerated experiments one can draw a relationship between failure rate and time at the product use temperature and thus predict the product's reliability. It must be pointed out that any relationship obtained for a given material, device, or product by accelerated testing methods may not be applicable to all materials, devices, or products. For each generation of devices, chips, and packages, new relationships should be calculated. Similarly, for each ILD fabricated by different methods accelerated tests should be done independently.

The practice of defining reliability is to give failure rate in time in terms of the unit FIT, which is defined as one failure in one billion device-hours. Thus, if there is one failure in a million devices tested for 1000 h, the failure rate will be on FIT.

The most common acceleration methods used to evaluate reliability are to determine the failures at high temperatures, high humidity, increased current or voltages, and increased stress if necessary.

12.6 Conclusions

It has been mentioned at several places in this chapter and in other preceding chapters of this book that the reliability of ILDs can be enhanced by eliminating the causes that lead to failure – impurities, defects, porosity, fatigue, stress, corrosive environment, and interdiffusion, for example. Most of these causes are related to deposition process. Some are related to the ILD itself. Use of pure materials on clean surfaces will eliminate many of the problems. An understanding of the various processes, failure modes, and the limitations should be obtained and then used to define and enhance the usefulness of the ILD. Many of the concepts mentioned are based on prior experience and should be used as general guidelines to obtain better experimental data on actual samples and models that extend the usefulness of experimental data.

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Chapter 13
Future trends in silicon technologies

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Abstract

The advancements in silicon semiconductor technology in the last 30 years has primarily been driven by Moore's Law. This was enabled by lithographic device shrinks as well as the introduction of new materials for each new generation of devices. In addition, scaling of the planar CMOS transistor structure has allowed improvement in performance for the last 20 plus years. However, conventional planar CMOS device structure is fast approaching its scaling limits. New materials as well as new device structures will be needed to alleviate the scaling issues. Two of the most important new materials being introduced are high-κ and low-κ dielectrics. Some of the new devices under investigation include SOI, strained Si, vertical CMOS transistors with double gate, 3D ICs, etc. In addition, new memory devices, such as FeRAM, MRAM, and OUM devices, will evolve to replace DRAM and Flash for embedded logic devices in the foreseeable future. This chapter examines the future trends in CMOS device technology, and the extension of CMOS scaling, for both high-performance logic and memory devices. It also examines the implications of these new device structures on future process and material requirements, with emphasis on dielectrics materials.

13.1 Introduction

The preceding chapters discuss the fundamental properties (Chapter 2), characterization techniques (Chapter 3), interface properties (Chapter 4), and reliability (Chapter 12) of dielectric materials for semiconductor applications. These dielectrics include conventional SiO_2-based material for isolation, gate, and insulating layers between conducting metals, high-κ gate and capacitor dielectrics, and various low-κ dielectrics for interconnects. High-κ gate and capacitor materials, including Ta_2O_5 and a new class of transition metal oxides (i.e. HfO_2) deposited by atomic layer deposition (ALD), are discussed in Chapter 10. Low-κ materials include a totally different class of materials, such as low-κ polymers, C-F based and carbon-doped CVD low-κ materials, spin-on Si-based low-κ materials, and porous low-κ dielectrics. Deposition techniques, film

properties, integration issues and applications of these materials are reviewed in Chapters 4–9. The low-κ and high-κ materials discussed above present the two most important classes of dielectric materials for semiconductor applications going forward. In this chapter, we discuss the future trends in semiconductor device technology and the impact of new dielectric and metallic materials to enable the continued evolution of future semiconductor devices.

13.2 Trends in silicon device technologies

The advancements in silicon semiconductor technology in the last 30 years has primarily been driven by Moore's Law, which states that the number of transistors on a chip doubles every 18 months. This is enabled by a shrink in transistor feature size of 0.7x per technology generation, which occurs about every 18 months, and is driven by gains in performance and cost as discussed in Chapter 1. New materials were introduced to accommodate the shrinks and improve performance. Figure 13.1 shows the Moore's Law plot of increasing transistor density with each generation of microprocessor and dynamic random access memory (DRAM) devices and the introduction of new materials at the respective technology nodes. It depicts the accelerated pace of new material introduction into each generation of products, and the transition from DRAM to microprocessor as the technology driver for new materials introduction. This translation began in 1989 with the application of three-layer metallization in high-performance logic devices. The graph underscores the importance of introducing new materials extending Moore's Law.

Figure 13.2 shows the trend in lithographic shrinks for each device technology generation and the accelerated trend in physical gate length shrinks compared to technology node shrinks in the last two to three device generations [1]. This is enabled by the introduction of lower wavelength and higher NA (numerical aperture) lithographic tools and advanced etching technologies. Figure 13.3 shows an exponential decrease in gate oxide thickness with each generation of devices [1]. This is dictated by the CMOS scaling rules where the speed of the device is a function of gate length and the dielectric film thickness. This graph shows that we have approached the tunneling limit of conventional SiO_2, underlining the need for high-κ gate dielectrics. The results illustrated in Figs 13.1–13.3 have allowed the semiconductor industry to extend Moore's Law.

To enable the continuation of Moore's Law, this trend in device shrink and its requisite new materials introduction will likely continue at an even faster pace. Examples of some of the conducting and semiconducting materials being introduced are Cu metals and TaN barriers for interconnect metallization, and PolySiGe to reduce the poly-Si depletion effect and double-metal gates to enhance mobility. The rest of the new materials to be introduced are dielectric materials.

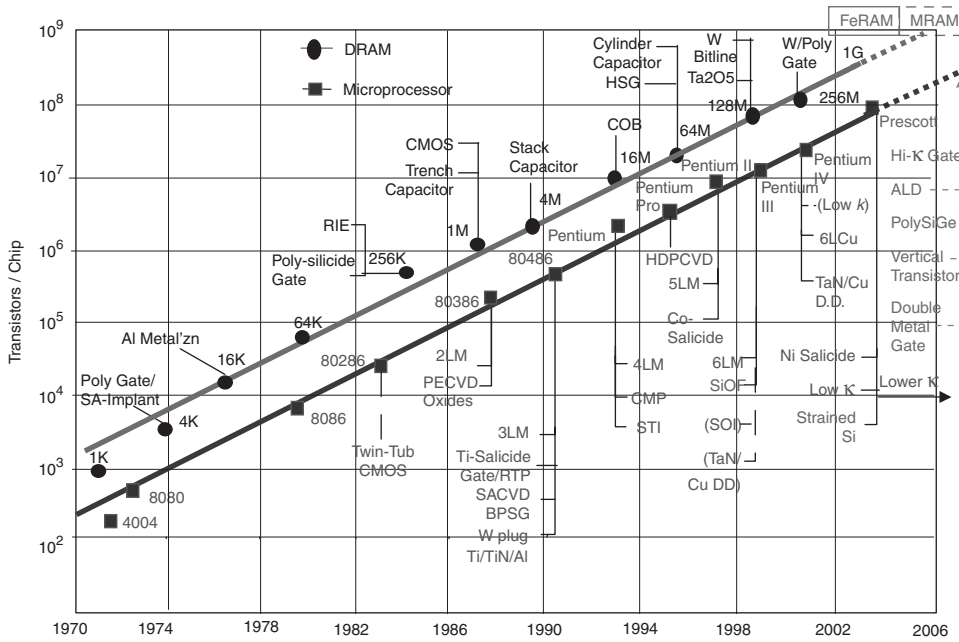

Fig. 13.1 Moore's Law and the Introduction of New Materials and Technology. This graph depicts Moore's Law, which shows an exponential increase in transistor counts/chip over the last 3 decades. The top line depicts the trend in DRAM devices starting from 1Kb to 1Gb, while the bottom line depicts the trend for high performance Logic devices (e.g. Intel's Microprocessor, starting with Intel's 4004 to Prescott). The introduction of new materials and technologies for each device node are depicted in solid lines while the dash line indicates new materials first introduced during that time frame, albeit, for a different microprocessor (e.g. IBM first introduced SOI and Cu in 1998 for their 0.22 μm MPU devices). The technologies connected to the dash line with the arrow pointed upwards are future technologies to be introduced to meet the CMOS scaling requirements. (*Source*: http://www.intel.com/research/silicon/micron.htm, G. Shahidi (2002), 'SOI Technology for the GHz Era' *IBM Journal of Research and Development* **46**, 121.)

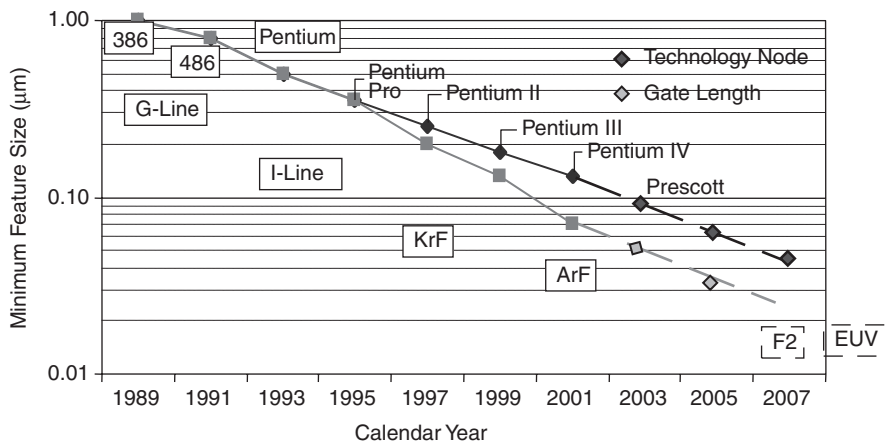

Fig. 13.2 Lithography-enabled feature size and gate length shrink for each technology node with time.

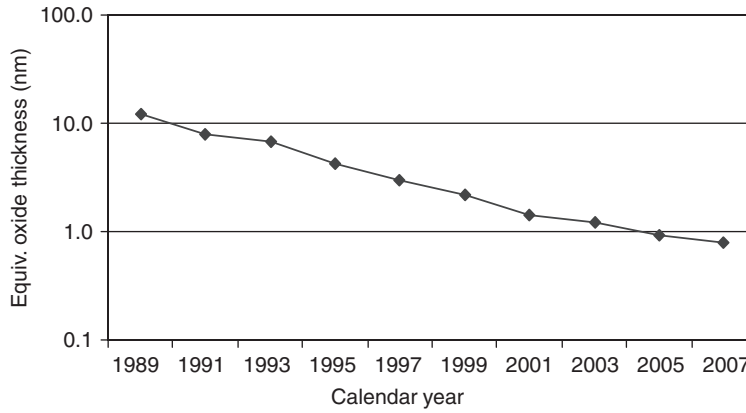

Fig. 13.3 Gate dielectric thickness scaling with time.

To decrease RC delay to enhance speed while reducing power consumption and improving portability, low-κ dielectrics such as CVD carbon containing SiO_x [2, 3], spin-on polymer low-κ (e.g. SiLK) [4], and porous oxides [5] are being introduced to lower interconnect capacitance. These materials are discussed in Chapters 1–9. Future low-κ dielectric materials may include air bridges to achieve the ultimate κ value. To improve transistor performance, high-κ gate dielectrics will be needed to satisfy the scaling of the gate oxide thickness and to reduce leakage. For memory devices, high-κ capacitor dielectric is introduced to accommodate the shrink by reducing the cell size without sacrificing the signal-to-noise ratio. The high-κ materials were briefly mentioned in Chapters 1 and 4 and discussed in detail in Chapter 10.

For metallization, the focus is to lower resistivity yet improve reliability. Doped Cu and single crystal electromigration and stress migration-free metallization processes will be needed. Optical signal may someday be used to enhance the clock speed. However, alternative circuit architecture and wiring approaches such as 3D chip architecture and high-frequency transmission lines may be more beneficial in alleviating the problem with interconnect RC delay and materials requirements [6, 7].

A billion people worldwide are now connected by networked communication devices. Advances in semiconductor technologies that provide more powerful, portable, and more affordable chips will enable the next billion people to join the global community in the information age. In the subsequent sections, we will discuss the trends and evolution of future semiconductor device technologies and their impact on the dielectric materials requirements.

13.2.1 Transistors

For mainstream logic devices, the conventional planar CMOS structure (Fig. 13.4) will be scaled down to the 65 nm technology node with ~35 nm physical gate lengths (Fig. 13.2) with minimal

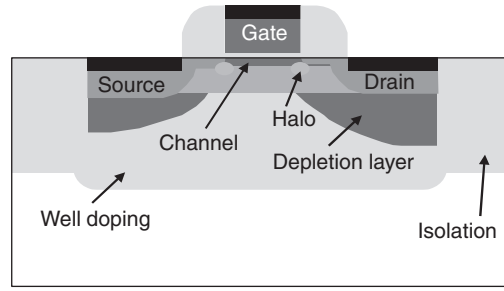

Fig. 13.4 Planar CMOS structure.

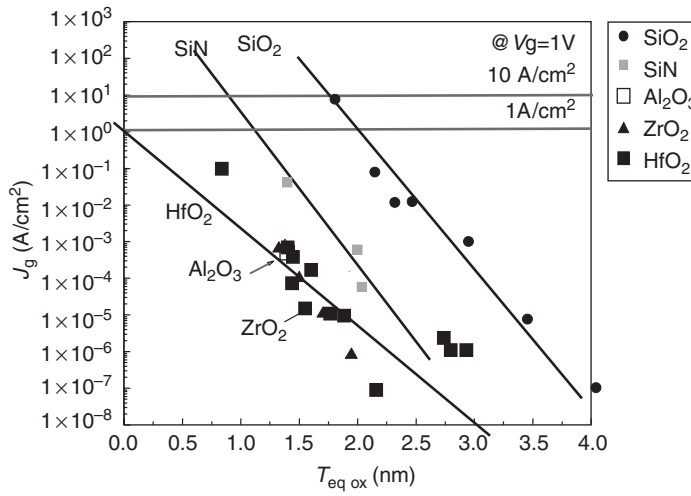

Fig. 13.5 Thickness dependence of leakage current for high-κ materials.

material and process changes. Gate CD control will continue to remain the most critical parameter, especially for high-performance logic devices since it affects the speed of the device.

Beyond the 65-nm technology node, the planar CMOS structure will start hitting the scaling limits in several areas such as gate oxide thickness, poly-gate electrode sheet resistance, control of short channel effects (SCE), which results in device performance degradation due to drive current degradation, and S/D extension resistance. The conventional SiO_2 gate has reached its physical limit at ~15 Å due to very high direct tunneling leakage and reliability limitations. Nitrided oxide (SiON) and nitride-stacked gates (SiO_2/Si_3N_4) helped extend the useful life of gate oxides to about 12–14 Å. Equivalent oxide thickness (T_{ox}) and may extend down to the 65 nm node with a T_{ox} of ~10–12 Å. High-κ gate dielectrics will be needed for high-performance logic devices, and may be introduced first for low power/wireless devices since these devices are less tolerant to gate leakage [1]. Figure 13.5 shows the thickness dependence of leakage current for

the various high-κ materials compared to SiO_2 [8–10]. The SiO_2-based gate oxide will reach the 1 A/cm^2 limit at about 18 Å and 10 A/cm^2 at ~15 Å. The Si_3N_4 gate can extend to about 10–12 Å using the same criteria. Al_2O_3, HfO_2, and ZrO_2, on the other hand, can meet the requirement below the 10 Å region.

With gate oxide thickness at only two to four atomic layers, atomic layer deposition (ALD) technology will become a critical approach for depositing high-quality, ultra-thin layer films with conformal step coverage. The ALD process deposits films less than one monolayer at a time. The films are deposited in a very small volume chamber and the reactants flush out rapidly after each deposition cycle. ALD can also be used to deposit high-κ dielectrics for DRAM capacitors as well as for Cu barriers and seed layers at the 90–65 nm node. The applications of ALD to the fabrication of high-κ gate and capacitor dielectrics were discussed in Chapter 10.

PolySiGe gate electrodes will extend PolySi gate technology, prior to the introduction of metal gates, to suppress the poly-depletion and boron penetration effect for logic devices and as a lower bandgap material to change the work function of the PMOS transistor for DRAM devices. Ni salicide is being introduced at the 65 nm node to overcome the sheet resistance rise from narrow lines as well as to meet ultra-shallow junction requirements. Selective epi/raised S/D techniques are being introduced to elevate the junction and address ultra-shallow junction leakage. In addition, selective epi/SiGe can provide strain Si in the channel to enhance mobility and improve the speed of the device. Dual work function metal gates will be needed thereafter. Figure 13.6 shows the work function of the various candidates for metal gate electrodes. It has been shown that N_2 can be used to dope TiN_x [11] and Mo [12] to provide an adjustable work function for N^+ and P^+ devices. This is a current area of active research. The industry likely is start using to metal gate electrode around the 45–32 nm technology node; but the metal of choice is yet to be determined. It will largely be determined by several factors: the ease of integration and compatibility of this material to the high-κ gate dielectric, the device structure under

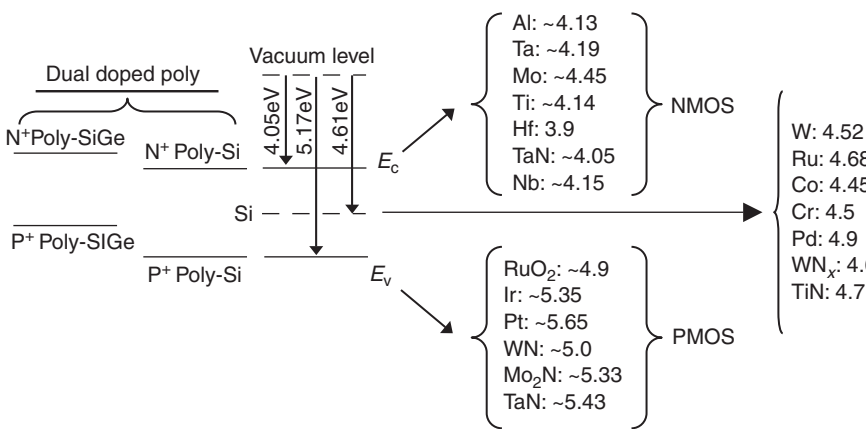

Fig. 13.6 Work functions of candidate gate electrodes.

Table 13.1 Challenges and potential solutions of planar CMOS technologies

Challenges	Potential solutions
Maximum drive current (I_{dsat}) and minimum off-state current (I_{off})	Small poly-gate width with gate trim or poly undercut technology Increase mobility by using strain SiGe Decrease leakage with SOI
Oxide leakage due to gate oxide thickness approaching physical limits	High-κ gate dielectric
Gate sheet resistance increase due to narrow gate width and poly-depletion effect	Ni salicide and PolySiGe gate electrode Nitrogen implant into poly-gate Dual work function metal gate
Short channel effect	Precise control of halo implant (location, angle, and dose control) for threshold voltage (V_t) and punch through
Ultra-shallow junction	NiSix, Quench cool RTA, or laser anneal

which the metal gate is to be implemented, whether single or double metal gates are used, the use of SOI, and performance gain and long-term reliability issues.

The major challenges and potential solutions of planar CMOS technologies are summarized in Table 13.1.

In summary, the most critical challenge in the transistor or front-end technology in the next few years will be the introduction of high-κ gate dielectrics, even though thermal oxide has been used for the last 30 years and has been the pillar of silicon MOS device technology.

13.2.2 Interconnects for logic devices

For today's high-performance logic devices, there are up to eight metal interconnect layers for the 130 nm technology node; this number will increase with future device generations. Interconnect RC delay can rapidly become the limiting factor in circuit speed. Both CVD [2, 3] and spin-on low-κ dielectric materials ($\kappa = 3.0$–2.8) [4] are currently being introduced at the 130-nm node to alleviate the RC delay problem. This same family of materials will extend to the 90–65 nm node with some modifications to lower the κ value to 2.6–2.5 and even down to $\kappa \sim 2.2$. Significant effort has been invested by the industry to integrate these materials (with different etch and clean sequences, etc.) into the production line. Below the 65-nm technology node, dielectric films with $\kappa = 2.2$–1.1 will be needed; these films again will present significant integration challenges to the industry. The integration challenges of these materials are thoroughly covered in Chapters 4–9 for different low-κ films. The introduction of low-κ dielectrics and the continued evolution of these materials to achieve lower and lower κ values will continue to be

one of the most critical challenges in materials technology for years to come, which is why this topic receives the widest coverage in the book.

For the Cu dual damascene process, a thin, conformal barrier will be required to reduce the cross-sectional area consumed by the barrier, to reduce overall metal line resistivity. The ALD process will become an important technique for depositing these films due to its conformality and monolayer thickness control capability. Cu electrochemical plating (ECP) with subsequent chemical mechanical polishing (CMP) are the most widely accepted methods for fabricating Cu wires today. However, due to its process complexity, cost and performance limitations (i.e. step coverage, non-uniformity, void formation, and reliability concerns) in meeting the requirements of the sub-100 nm technology node, Cu metallization technology will continue to evolve. Eventually, a simpler, cheaper, and more uniform deposition technique will emerge that provides Cu films with better electromigration and stress migration resistance to meet these requirements.

13.2.3 Memory devices

Conventional DRAM devices consist of one capacitor and one transistor cell structure (Fig. 13.7). To continue with the scaling of DRAM memory cell, Ta_2O_5 is used as a high-κ capacitor dielectric starting at the 256 Mb DRAM device generation [13, 33]. Although ALD Al_2O_3 was shown to have better thermal and leakage properties [14] than Ta_2O_5, it has a κ value of only ~8–9

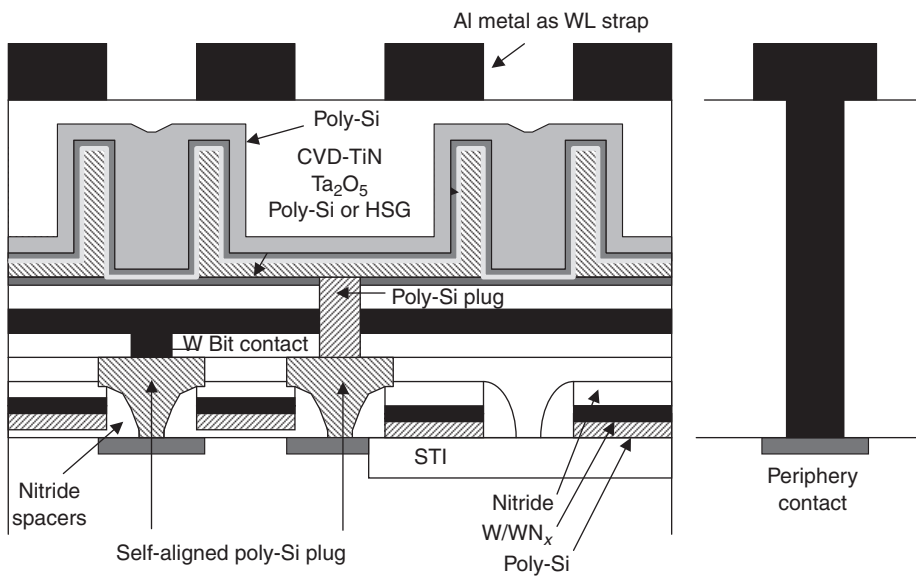

Fig. 13.7 DRAM cell and periphery contact structure.

compared to a κ value of ~22–25 for Ta_2O_5. It may be possible to improve the leakage properties of Ta_2O_5 with ALD. Nevertheless, Al_2O_3 may be a more suitable high-κ dielectric material for trench capacitor cell DRAM devices due to its better thermal and leakage properties. Al_2O_3 can also be used as an encapsulated barrier layer material to prevent H_2 diffusion into the high-κ capacitor dielectric material during ILD anneal and metal alloying process [15]. It is also used as a tunneling oxide layer for MRAM (Magneto-resistive RAM) devices. These two devices are discussed later in the chapter. In addition, Al_2O_3 appears to have good interface properties with Si and may serve as a good interfacial layer between Si and high-κ gate oxide. This and other high-κ dielectric materials are discussed in Chapter 10. Continued scaling of DRAM devices will require capacitor dielectrics of higher and higher κ value, such as BST that has a κ value of ~300. This requirement, similar to the high-κ gate oxide and the low-κ interconnect dielectric requirements for logic devices, will present the most critical materials technology challenges for DRAM devices for years to come.

The Flash memory market is growing rapidly due to wireless communications and portable applications. Figure 13.8 shows a cross-section schematic of a Flash NOR cell structure. It consists of multiple transistors such as a core memory cell, a high-voltage transistor, and a low-voltage transistor for the periphery circuit. This structure has significant process complexity,

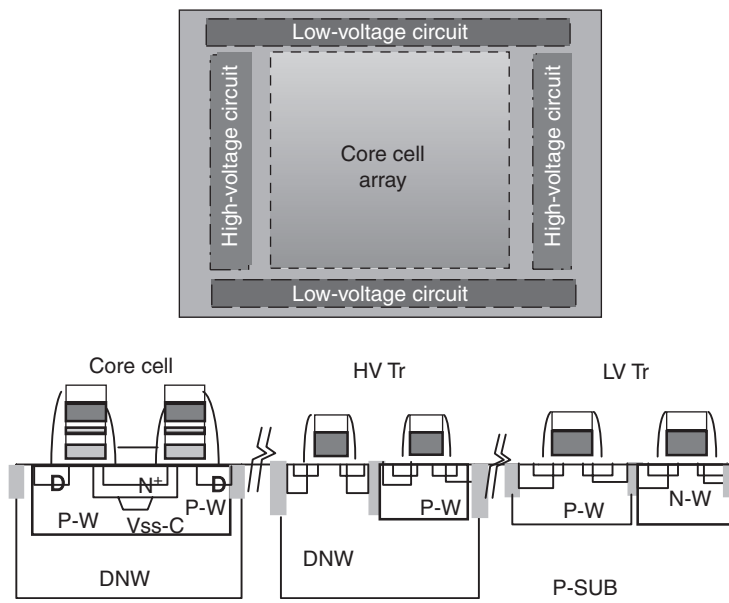

Fig. 13.8 Flash NOR transistor structure. It shows a flash core memory cell transistor structure that consists of the flash memory and the word line gate stack, with deep N-well, a high-voltage transistor, with deep N-well and the word line transistor, and a low-voltage transistor for logic circuits, which consists of conventional N- and P-wells, and polycide gate.

requiring multiple gate oxide thicknesses, a triple well for core cell and high-voltage circuits, dual trench isolation, and dual spacer technology, all within a single device [16].

The most significant technology challenge for Flash memory is that it hits the scaling limit at the tunnel oxide thickness of 8–10 nm due to reliability constraints from high-voltage requirements. Future scaling of the Flash cell has taken the approach of lateral scaling without vertical scaling, thereby increasing the aspect ratio. The multiple-bits per cell structure have been used for 180 nm technology, but requires much better process control (such as V_t, etc.). In addition to the conventional NOR and NAND flash memory structure, a new scalable Flash cell structure will emerged in the near future.

13.2.4 Future memory devices

Other memories such as FeRAM (ferroelectric RAM) and MRAM (magneto-resistive RAM) devices have the advantage of being non-volatile, use low power, have fast read/write time, high endurance, and alpha particle immunity. Hence, they are being investigated as a universal memory to replace DRAM, Flash, and SRAM devices for system on a chip (SOC) applications. Advanced FeRAM devices, like DRAM, consist of a one-capacitor, one-transistor cell structure [17, 18]. Figure 13.9 shows the schematic of a typical FeRAM cell. The most critical component of the FeRAM is the ferroelectric capacitor, which is used for data storage and retention. The structure typically consists of a planar capacitor with two ferroelectric metal electrodes and a high-κ dielectric sandwich. Typical electrode materials are Pt, Ru/RuO_2, or Ir/IrO_2. The most challenging material requirement for FeRAM devices, like DRAM, is the high-κ dielectric sandwich. Typical dielectric materials being used are PZT [Pb (Zr, Ti_xO_3)] or SBT [($SrBi_2$) Ta_2O_9], ALD Al_2O_3 or SiN is used as the H_2 diffusion barrier or capping layer to prevent ionic contamination to the device, which causes leakage problems.

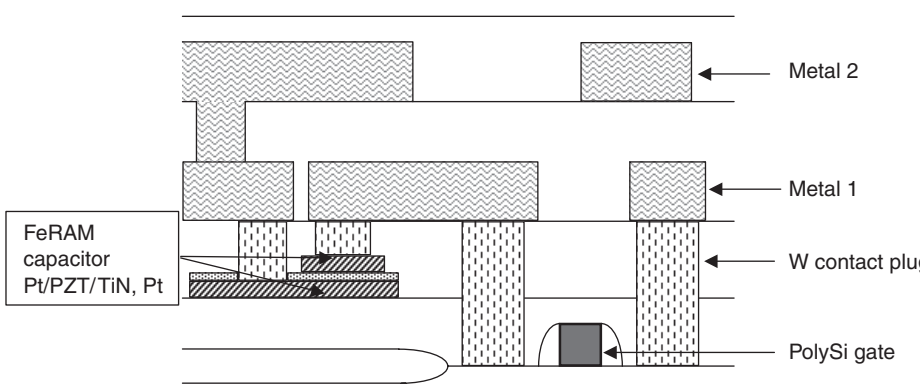

Fig. 13.9 Planar FeRAM structure.

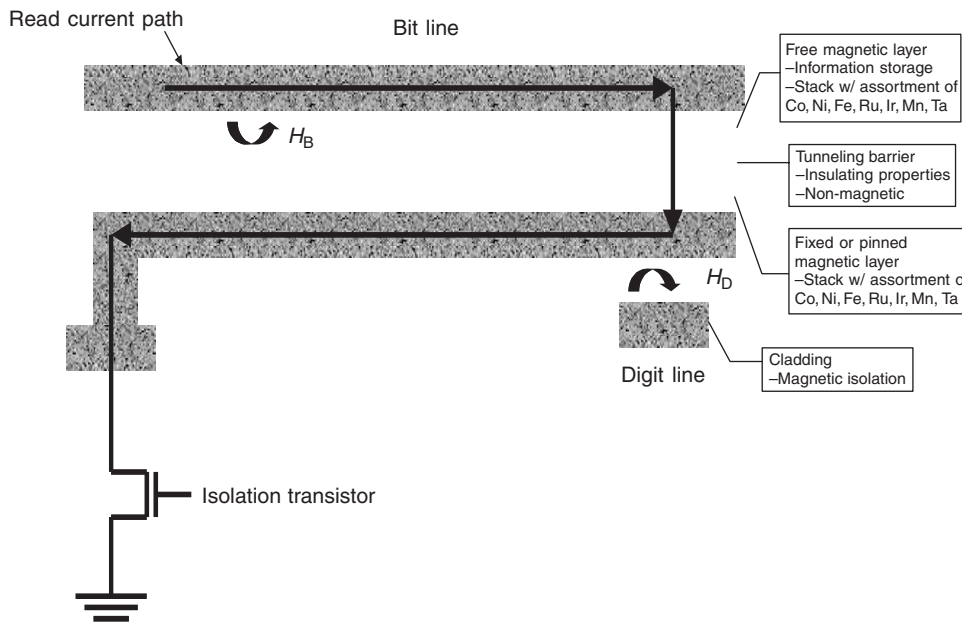

Fig. 13.10 MRAM structure.

MRAM (magneto-resistive RAM) devices (Fig. 13.10) consist of a stack of very thin ferromagnetic layers (on the order of sub-10 nm thickners) comprised of Co, Fe, Ni, Ru, Ir, Mn, Ta, etc., and an antiferromagnetic layer stack with a tunneling oxide sandwich. This multilayer ferromagnet–insulator–antiferromagnet sandwich enables electrons to tunnel through the insulating barrier, usually Al_2O_3, with their spin directions conserved. This tunneling oxide layer is typically a few nanometers thick of Al_2O_3 and requires a thickness uniformity control of ~1% 3σ, which can hopefully be achieved with ALD. These magnetic tunnel junction devices are said to possess field-dependent tunneling conductance or tunneling magnetoresistance. The most critical challenge for the successful implementation of this technology is the ability to deposit the thin ferromagnetic and antiferromagnetic stack layers, and its tunneling oxide sandwich, with the required thickness control and spin properties.

Another promising technology to replace Flash and DRAM is the Ovonic Unified Memory technology (OUM) [19]. This technology is based on a thin film of chalcogenide alloy material ($Ge_xTe_ySb_z$), which changes between the amorphous and polycrystalline states when subjected to heat (Fig. 13.11). The cell is programmed by application of a current pulse at a voltage above the switching threshold. The programming pulse drives the memory cell into a high (amorphous) or low (crystalline) resistance state, depending on current magnitude. Information stored in the cell is read out by measurement of the cell's resistance. For example, an electric

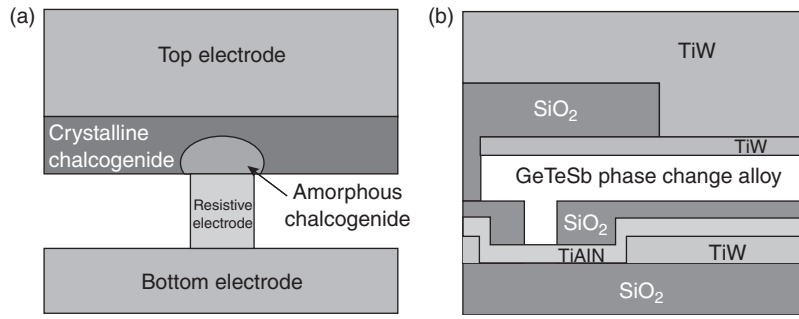

Fig. 13.11 Ovonics unified memory cell technology: (a) OUM cell technology; (b) Cross-section of cell structure. (*Source*: Ref. [19] and www.ovonyx.com).

current through the material shifts it from an amorphous to a crystalline state. This changes the material's capacitance by up to 200%, activating the cells to store data bits. The data are retained even when the power is switched off, and can be restored when the power is switched back on, making it non-volatile. The OUM device can be reprogrammed through RESET to revert back to the high-resistance (amorphous) state. The concept has been demonstrated with a 4-Mb test chip. The Ovonics memory technology has read and write times of 100 ns, which is faster than the current Flash technologies, and is non-volatile. The other perceived advantages are that it is less expensive to produce than Flash and DRAM, due to its smaller cell size, and is also easier to integrate into a standard logic process for an embedded memory device. The most critical material technology challenge for this device is the fabrication of the chalcogenide alloy material. The rest of the materials technology requirements are similar to conventional CMOS technology.

13.2.5 Technology trend summary

To enable the fabrication of these advanced devices, new fabrication technologies, such as ALD, and low-temperature processing, such as spin-on technologies, with environmentally friendly process solutions need to be developed. New diagnostic and metrology tools, that are non-destructive, and can give real time, high resolution and quantitative measurements of electrical conductance of layers, dielectric film thickness, pore sizes as well as GHz capacitance measurements, will be required, along with predictive models and tools with adaptive control capabilities. In addition, new and more advanced packaging technologies (i.e. 3D chip stack, flip chip, etc.) will be needed to accommodate the shrink and enable the overall improvement in system performance as well as the decrease in form factor to increase portability.

13.3 Future CMOS device structures

Around the 45 nm technology node and beyond, more drastic changes in future device structures will be introduced to alleviate the transistor scaling issues associated with conventional planar CMOS structures as discussed above. These new device structures include fully depleted silicon on insulator (FDSOI), double metal gate CMOS, vertical transistor, etc. They will require the introduction of new materials technologies.

13.3.1 Silicon on insulator (SOI) device structure

SOI device structure offers the extension of CMOS scaling by reducing device parasitics, such as junction capacitance. Partially depleted SOI (PDSOI) devices have exhibited better control of short channel effects down to a very small gate length (<60 nm) with an increase in drive current (I_{on}). This results in faster transistor with lower power consumption over comparable bulk CMOS device [20]. Figure 13.12 shows the different SOI transistor structures [21]. The main difference between these SOI structures lies in the thickness difference of the Si layer. The PDSOI device consists of a thin Si layer, on the order of 200–50 nm, on top of a buried oxide layer (BOX). The CMOS device is built on this Si layer. In this device, the depletion depths of the CMOS channel are shallower than the thickness of this Si layer, hence the name partially depleted SOI. For a fully depleted SOI (FDSOI) device, the Si layer is on the order of 10 nm, and is equivalent to the channel and source–drain extension depth. The thin-body nano-SOI is just another version of the FDSOI, with an even thinner SOI layer. PDSOI devices are being manufactured today for high-performance logic products in the 130 nm technology nodes [22]. As shown in Fig. 13.12, PDSOI is simply a bulk CMOS device truncated at the BOX interface.

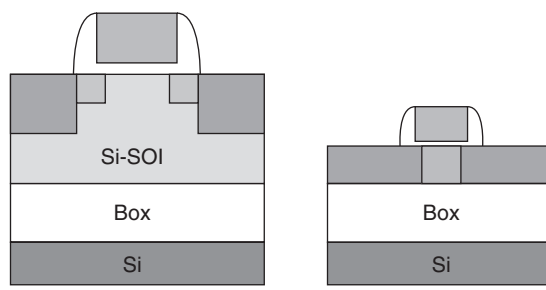

Fig. 13.12 SOI CMOS transistor structures.

Hence, its scaling considerations are nearly identical to a bulk CMOS device. The biggest difference between PDSOI and bulk CMOS is that the channel body of the PDSOI device is electrically floating, which leads to the well-known "floating body effect" caused by stagnation of excess majority carriers in the body. This floating body effect could induce V_T variation, and lead to propagation delay variation, especially as the supply voltage is reduced. This puts a significant burden on device and circuit designer to reduce the floating body effect [23].

In the next few years, FDSOI devices will be introduced at or below the 45 nm technology node. The FDSOI device has been demonstrated to provide significant performance gain over bulk CMOS without the floating body effect [24]. Much steeper sub-threshold slopes, reduced DIBL (drain-induced barrier lowering) have been demonstrated for both NMOS and PMOS transistors down to the 50 nm physical gate length for the FDSOI device. To overcome the salicide formation and high parasitic resistance problems in thin-silicon-body devices, a raised source–drain was used. This improved the drive current (I_{on}) and provided a 30% gain in I_{on} for a given off-current (I_{off}) over previously reported PDSOI and bulk CMOS devices. However, Sherony *et al.* [25] have shown that to totally eliminate the floating body effect, the Si film thickness must be significantly thinner than the depletion depth of the channel. This presents significant manufacturing challenges. Nevertheless, the FDSOI device structure allows the possibilities of implementing new IC device architecture that exploits the third dimension. These include double-gate MOSFETs for increased current drive density and dynamic V_T control, a substantial increase in usable levels of interconnect, and 3D IC implementation [6]. In addition, FDSOI structures are also compatible with Si/SiGe strained Si material for enhanced mobility and lower temperature processing. Figure 13.13 shows the structure of an ultimate SOI transistor [26]. It suggests that to gain the full benefit of the SOI device structure, the transistor would still need to have all the process and materials enhancements that are consistent with the CMOS scaling rules, although SOI may be one generation of device performance improvement if everything else is equal.

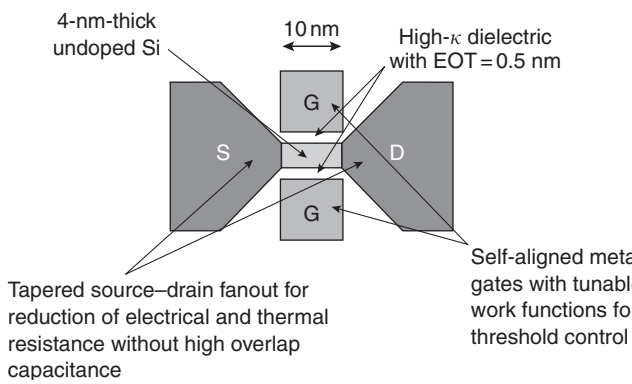

Fig. 13.13 The ultimate SOI transistor. (*Source*: Yuan Taur, UC San Diego, unpublished).

13.3.2 Double gate vertical CMOS transistor

ITRS 2001 predicted that beyond the 45 nm technology node the conventional single-gate planar CMOS transistor technology would run out of steam. The double metal gate CMOS transistor will be needed in conjunction with the ultra-thin-body FDSOI (<10 nm) to lower the parasitic capacitance and sub-threshold slope for short channel devices. The double metal gate technology would require that both gates are self-aligned to the source and drain and to each other, and the source–drain are fanned out to reduce series resistance as well as thermal resistance (Fig. 13.13). Since the threshold voltage would be dictated by the metal gate work function, it would be difficult to have multiple V_t on a chip. However, it has been reported that Mo can be doped with N_2 to provide different values of work function [12]. In addition, it may also be possible to operate both gates separately by biasing the back gate separately from the front gate to alleviate the requirement for having to align both gates to each other. However, this would add considerable process complexity. Since the planar CMOS structure has been perfected and used as the major transistor structure for the last 20 years, deviation from the conventional single gate planar CMOS structure will create significant challenges to the industry. To alleviate some of the processing problems associated with the double metal gate CMOS device, a double metal vertical replacement gate (VRG) transistor structure [27, 28] and a FinFET structure [29] have been reported. These structures are shown in Fig. 13.14(a) and (b), respectively. The VRG

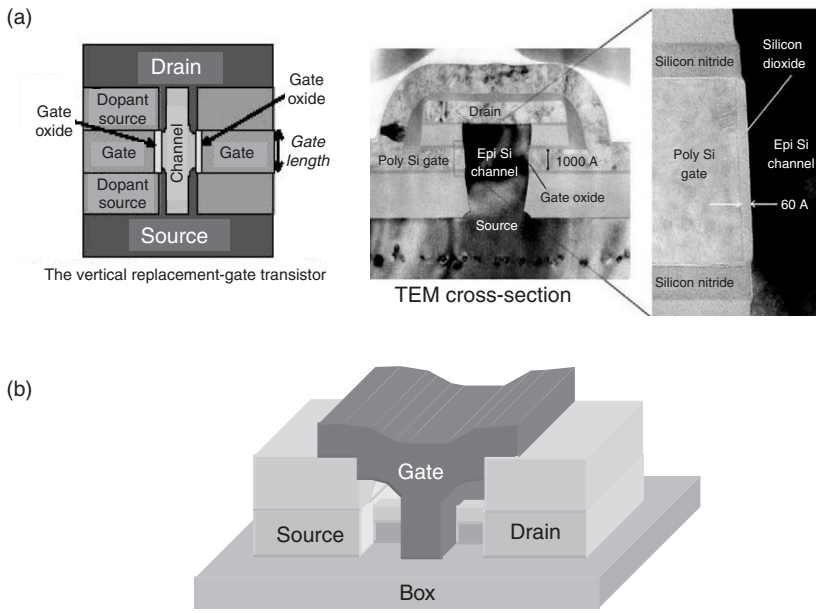

Fig. 13.14 Double gate CMOS vertical transistor: (a) vertical replacement gate (VRG) MOSFET; (b) double gate FinFET [29].

vertical transistor structure offers the unique advantage of the gate length controlled precisely by the deposited film thickness, and not by lithography and etches. Hergenrother *et al.* [30] demonstrated that a process control capability of 1% 1σ can be achieved with this device compared to the typical 3% 1σ values for the conventional lithography and etch process. The vertical transistor structure is also quite compatible with double metal gate technology. The FinFET structure, on the other hand, consists of a vertical Si fin controlled by a self-aligned double gate [31]. These structures offer some unique capabilities for extending the CMOS device down to below the 20 nm node and are being actively researched in universities and company research labs.

13.3.3 Future device trends summary

A conventional single gate planar bulk CMOS device structure will reach its scaling limits with performance degradation at around the 45 nm technology node if no new materials are introduced. PDSOI has been introduced to alleviate the short-channel effect associated with CMOS scaling, and FDSOI with a double gate structure will be needed at below 45 nm to extend CMOS. In addition, all the material enhancements, such as high-κ gates, low-κ interconnects, metal gates, and mobility enhancement materials such as SiGe, strained Si, which will be implemented

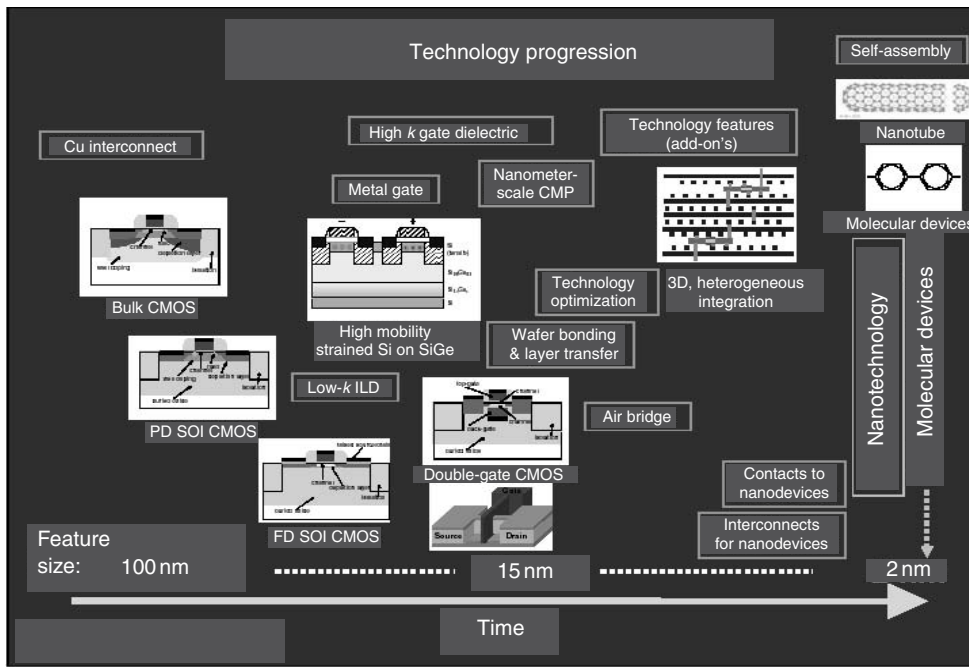

Fig. 13.15 Technology evolution beyond bulk CMOS *(Source*: Philip Wong, IBM, unpublished).

for bulk CMOS devices down to the 45 nm node, would still be required for the FDSOI device to provide the performance gain. Optical interconnects may replace electrical Cu wires for clocks and input/output circuits in the next 5–10 years to address RC delay and power problems if a cost-effective solution can be found. Alternatively, 3D ICs could be built to alleviate these problems. Figure 13.15 [32] shows the evolution and transition of various possible device structures beyond bulk CMOS technology. These new structures and materials will bring us to the next decade where molecular assembly and nano-fabrication technology may become a reality.

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