Chapter 1 Introduction and Background

The evolution of *very large scale integration* (VLSI) technology has developed to the point where millions of transistors can be integrated on a single die or "chip." Where integrated circuits once filled the role of sub-system components, partitioned at analog-digital boundaries, they now integrate complete systems on a chip by combining both analog and digital functions [1]. *Complementary metal-oxide semiconductor* (CMOS) technology has been the mainstay in mixed-signal[1] implementations because it provides density and power savings on the digital side, and a good mix of components for analog design. By reason of its wide-spread use, CMOS technology is the subject of this text.

Due in part to the regularity and granularity of digital circuits, computer aided design (CAD) methodologies have been very successful in automating the design of digital systems given a behavioral description of the function desired. Such is not the case for analog circuit design. Analog design still requires a "hands on" design approach in general. Moreover, many of the design techniques used for discrete analog circuits are not applicable to the design of analog/mixed-signal VLSI circuits. It is necessary to examine closely the design process of analog circuits and to identify those principles that will increase design productivity and the designer's chances for success. Thus, this book provides a hierarchical organization of the subject of analog integrated-circuit design and identification of its general principles.

The objective of this chapter is to introduce the subject of analog integrated-circuit design and to lay the groundwork for the material that follows. It deals with the general subject of analog integrated-circuit design followed by a description of the notation, symbology, and terminology used in this book. The next section covers the general considerations for an analog signal-processing system, and the last section gives an example of analog CMOS circuit design. The reader may wish to review other topics pertinent to this study before continuing to Chapter 2. Such topics include modeling of electronic components, computer simulation techniques, Laplace and *z*-transform theory, and semiconductor device theory.

1.1 Analog Integrated Circuit Design

Integrated-circuit design is separated into two major categories: analog and digital. To characterize these two design methods we must first define analog and digital signals. A *signal* will be considered to be any detectable value of voltage, current, or charge. A signal should convey information about the state or behavior of a physical system. An *analog signal* is a signal that is defined over a continuous range of time and a continuous range of amplitudes. An analog signal is illustrated in Fig. 1.1-1(a). A *digital signal* is a signal that is defined only at discrete values of amplitude, or said another way, a digital signal is quantized to discrete values. Typically, the digital signal is a binary-weighted sum of signals having only two defined values of amplitude as illustrated in Fig. 1.1-1(b) and shown in Eq. (1). Figure 1.1-1(b) is a 3-bit representation of the analog signal shown in Fig. 1.1-1(a).

$$D = b_0\,2^{-1} + b_1\,2^{-2} + b_2\,2^{-3} + \cdots + b_{N-1}\,2^{-(N-1)} = \sum_{i=0}^{N-1} b_i 2^{-i} \qquad (1)$$

[1] The term "mixed-signal" is a widely-accepted term describing circuits with both analog and digital circuitry on the same silicon substrate.

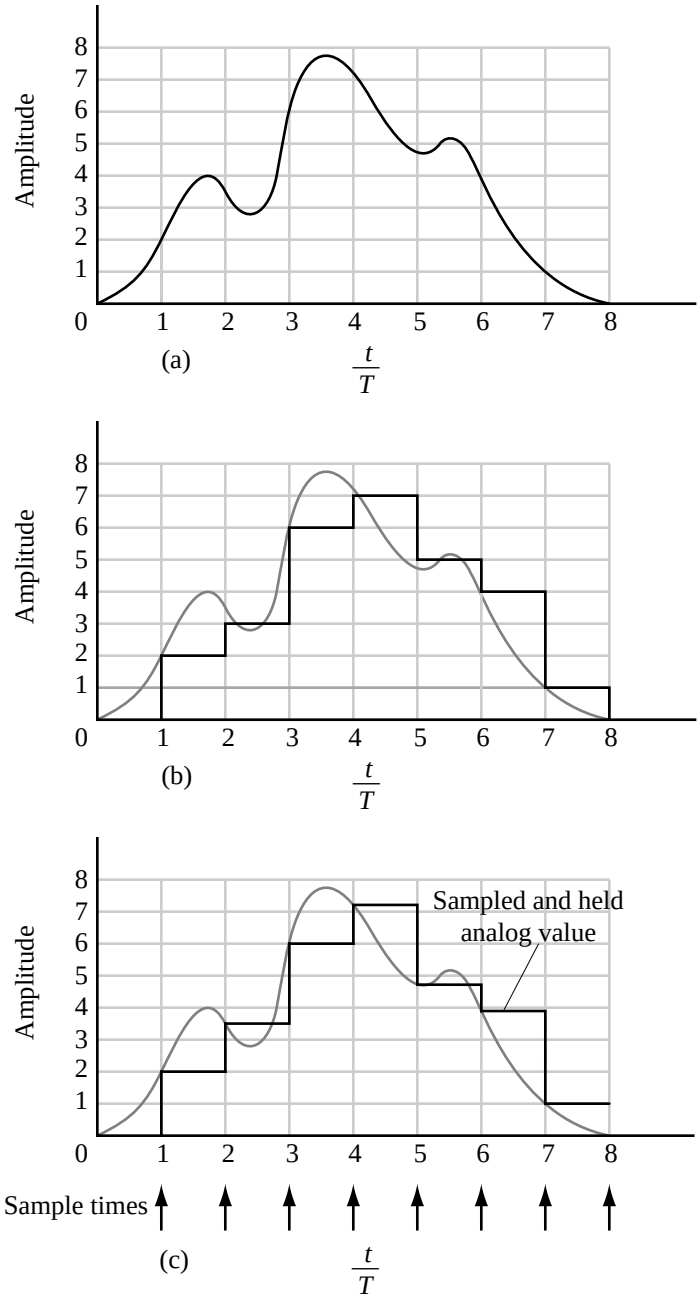

Figure 1.1-1 Signals. (a) Analog or continuous time. (b) Digital. (c) Analog sampled data or discrete time. T is the period of the digital or sampled signals.

The individual binary numbers, b_i, have a value of either zero or one. Consequently, it is possible to implement digital circuits using components that operate with only two stable states. This leads to a great deal of regularity and to an algebra that can be used to describe the function of the circuit. As a result, digital circuit designers have been able to adapt readily to the design of more complex integrated circuits.

Another type of signal encountered in analog integrated-circuit design is an analog *sampled-data* signal. An analog sampled-data signal is a signal that is defined over a continuous range of amplitudes but only at discrete points in time. Often the sampled

analog signal is held at the value present at the end of the sample period, resulting in a sampled-and-held signal. An analog sampled-and-held signal is illustrated in Fig. 1.1-1(c).

Circuit design is the creative process of developing a circuit that solves a particular problem. Design can be better understood by comparing it to analysis. The analysis of a circuit, illustrated in Fig. 1.1-2(a), is the process by which one starts with the circuit and finds its properties. An important characteristic of the analysis process is that the solution or properties are unique. On the other hand, the *synthesis* or design of a circuit is the process by which one starts with a desired set of properties and finds a circuit that satisfies them. In a design problem the solution is not unique thus giving opportunity for the designer to be creative. Consider the design of a $1.5\,\Omega$ resistance as a simple example. This resistance could be realized as the series connection of three $0.5\,\Omega$ resistors, the combination of a $1\,\Omega$ resistor in series with two $1\,\Omega$ resistors in parallel, and so forth. All would satisfy the requirement of $1.5\,\Omega$ resistance although some might exhibit other properties that would favor their use. Figure 1.1-2 illustrates the difference between synthesis (design) and analysis.

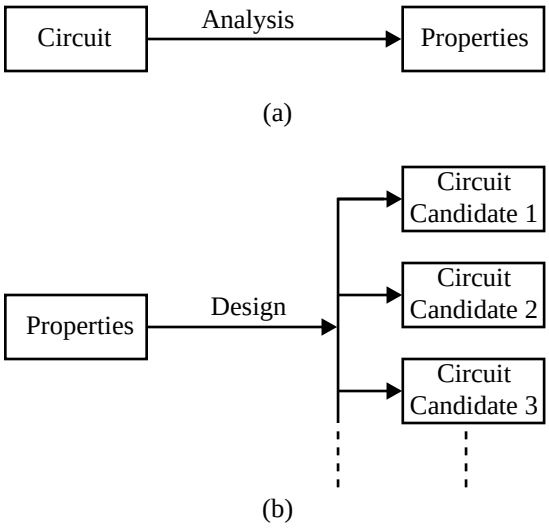

Figure 1.1-2 (a) The analysis process. (b) The design process.

The differences between integrated and discrete analog circuit design are important. Unlike integrated circuits, discrete circuits use active and passive components that are not on the same substrate. A major benefit of components sharing the same substrate in close proximity is that component matching can be used as a tool for design. Another difference between the two design methods is that the geometry of active devices and passive components in integrated circuit design are under the control of the designer. This control over geometry gives the designer a new degree of freedom in the design process. A second difference is due to the fact that it is impractical to breadboard the integrated-circuit design. Consequently, the designer must turn to computer simulation methods to confirm the design's performance. Another difference between integrated and discrete analog design is that the integrated-circuit designer is restricted to a more limited class of components that are compatible with the technology being used.

The task of designing an analog integrated circuit includes many steps. Figure 1.1-3 illustrates the general approach to the design of an integrated circuit. The major steps in the design process are:

1. Definition
2. Synthesis or implementation
3. Simulation or modeling
4. Geometrical description
5. Simulation including the geometrical parasitics
6. Fabrication
7. Testing and verification

The designer is responsible for all of these steps except fabrication. The first steps are to define and synthesize the function. These steps are crucial since they determine the performance capability of the design. When these steps are completed, the designer must be able to confirm the design before it is fabricated. The next step is to simulate the circuit to predict the performance of the circuit. The designer makes approximations about the physical definition of the circuit initially. Later, once the layout is complete, simulations are checked using parasitic information derived from the layout. At this point, the designer may iterate using the simulation results to improve the circuit's performance. Once satisfied with this performance, the designer can address the next step—the geometrical description (layout) of the circuit. This geometrical description typically consists of a computer database of variously shaped rectangles or polygons (in the *x*-*y* plane) at different levels (in the *z*-direction); it is intimately connected with the electrical performance of the circuit. As stated earlier, once the layout is finished, it is necessary to include the geometrical effects in additional simulations. If results are satisfactory, the circuit is ready for fabrication. After fabrication, the designer is faced with the last step—determining whether the fabricated circuit meets the design specifications. If the designer has not carefully considered this step in the overall design process, it may be difficult to test the circuit and determine whether or not specifications have been met.

As mentioned earlier, one distinction between discrete and integrated analog-circuit design is that it may be impractical to breadboard the integrated circuit. Computer simulation techniques have been developed that have several advantages, provided the models are adequate. These advantages include:

- the elimination of the need for breadboards.
- the ability to monitor signals at any point in the circuit.
- the ability to open a feedback loop.
- the ability to easily modify the circuit.
- the ability to analyze the circuit at different processes and temperatures.

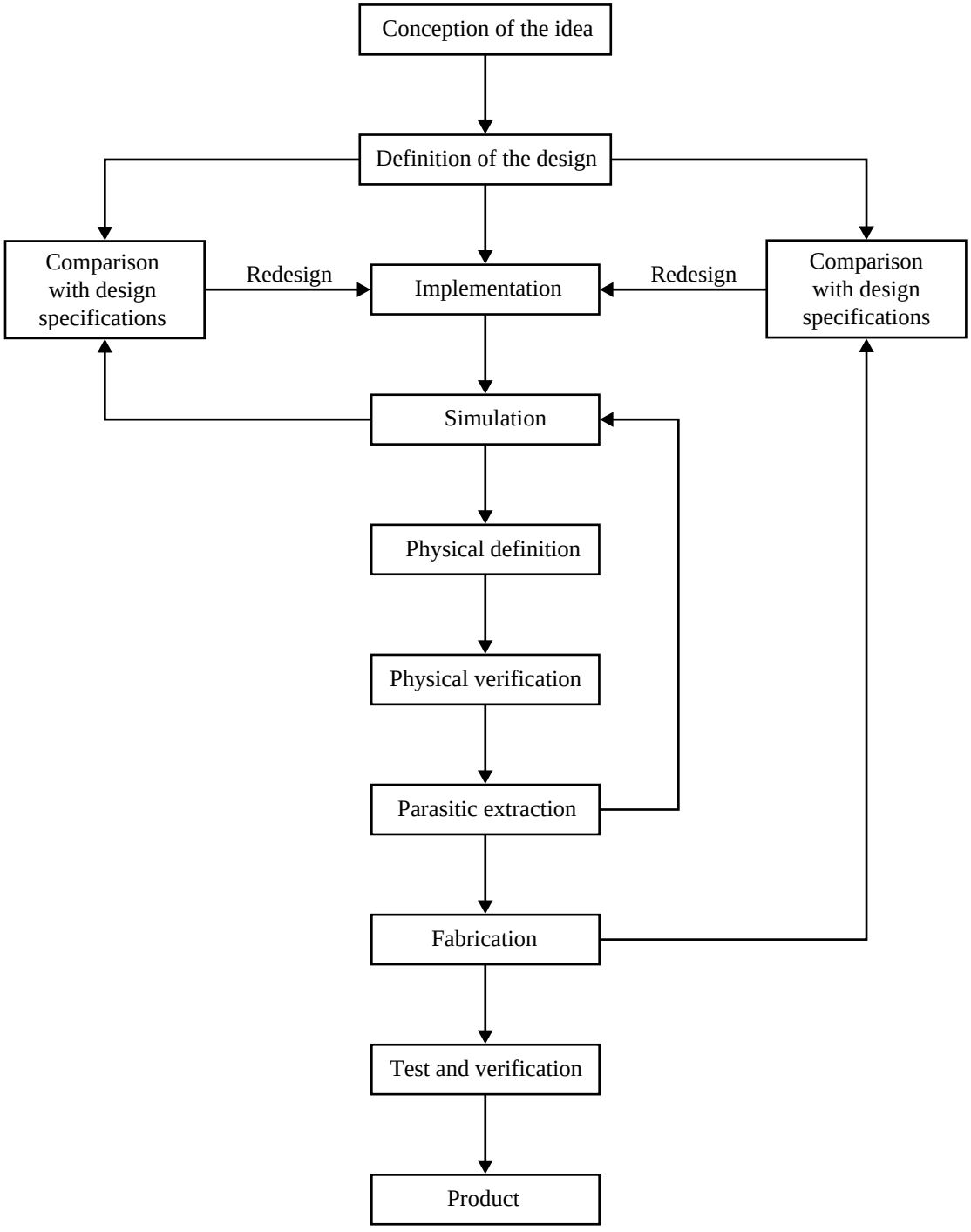

Figure 1.1-3 The design process for analog integrated circuits.

Disadvantages of computer simulation include:

- the accuracy of models.
- the failure of the simulation program to converge to a solution.
- the time required to perform simulations of large circuits.
- the use of the computer as a substitute for thinking.

Because simulation is closely associated with the design process, it will be included in the text where appropriate.

In accomplishing the design steps described above, the designer works with three different types of description formats. These include: the design description, the physical description, and the model/simulation description. The format of the design description is the way in which the circuit is specified; the physical description format is the geometrical definition of the circuit; the model/simulation format is the means by which the circuit can be simulated. The designer must be able to describe the design in each of these formats. For example, the first steps of analog integrated-circuit design could be carried out in the design description format. The geometrical description obviously uses the geometrical format. The simulation steps would use the model/simulation format.

Analog integrated-circuit design can also be characterized from the viewpoint of hierarchy. Table 1.1-1 shows a vertical hierarchy consisting of devices, circuits, and systems, and horizontal description formats consisting of design, physical, and model. The device level is the lowest level of design. It is expressed in terms of device specifications, geometry, or model parameters for the design, physical, and model description formats, respectively. The circuit level is the next higher level of design and can be expressed in terms of devices. The design, physical, and model description formats typically used for the circuit level include voltage and current relationships, parameterized layouts, and macromodels. The highest level of design is the systems level—expressed in terms of circuits. The design, physical, and model description formats for the systems level include mathematical or graphical descriptions, a chip floor plan, and a behavioral model.

Table 1.1-1 Hierarchy and Description of the Analog Circuit Design Process.

Hierarchy	Design	Physical	Model
Systems	System Specifications	Floor plan	Behavioral Model
Circuits	Circuit Specifications	Parameterized Blocks/Cells	Macromodels
Devices	Device Specifications	Geometrical Description	Device Models

This book has been organized to emphasize the hierarchical viewpoint of integrated-circuit design, as illustrated in Table 1.1-2. At the device level, Chapters 2 and 3 deal with CMOS technology, and models. In order to design CMOS analog integrated circuits the designer must understand the technology, so Chapter 2 gives an overview of CMOS technology, along with the design rules that result from technological considerations. This information is important for the designer's appreciation of the constraints and limits of the technology. Before starting a design, one must have access to the process and electrical parameters of the device model. Modeling is a key aspect of both the synthesis and simulation steps and is covered in Chapter 3. The designer must also be able to characterize

the actual model parameters in order to confirm the assumed model parameters. Ideally, the designer has access to a test chip from which these parameters can be measured. Finally, the measurement of the model parameters after fabrication can be used in testing the completed circuit. Device-characterization methods are covered in Appendix B.

Table 1.1-2 Relationship of the Book Chapters to Analog Circuit Design.

Design Level	CMOS Technology		
Systems	Chapter 9 Switched Capacitor Circuits	Chapter 10 D/A and A/D Converters	
Complex Circuits	Chapter 6 Simple Operational Amplifiers	Chapter 7 Complex Operational Amplifiers	Chapter 8 Comparators
Simple Circuits	Chapter 4 Analog Subcircuits		Chapter 5 Amplifiers
Devices	Chapter 2 Technology	Chapter 3 Modeling	Appendix B Characterization

Chapters 4 and 5 cover circuits consisting of two or more devices that are classified as simple circuits. These simple circuits are used to design more complex circuits, which are covered in Chapters 6 through 8. Finally, the circuits presented in Chapters 6 through 8 are used in Chapters 9 and 10 to implement analog systems. Some of the dividing lines between the various levels will at times be unclear. However, the general relationship is valid and should leave the reader with an organized viewpoint of analog integrated circuit design.

1.2 Notation, Symbology, and Terminology

To help the reader have a clear understanding of the material presented in this book, this section dealing with notation, symbology, and terminology is included. The conventions chosen are consistent with those used in undergraduate electronic texts and with the standards proposed by technical societies. The International System of Units has been used throughout. Every effort has been made in the remainder of this book to use the conventions here described.

The first item of importance is the notation (the symbols) for currents and voltages. Signals will generally be designated as a quantity with a subscript. The quantity and the subscript will be either upper or lower case according to the convention illustrated in Table 1.2-1. Figure 1.2-1 shows how the definitions in Table 1.2-1 would be applied to a periodic signal superimposed upon a dc value.

Table 1.2-1 Definition of the Symbols for Various Signals.

Signal Definition	Quantity	Subscript	Example
Total instantaneous value of the signal	Lowercase	Uppercase	q_A
dc value of the signal	Uppercase	Uppercase	Q_A
ac value of the signal	Lowercase	Lowercase	q_a
Complex variable, phasor, or rms value of the signal	Uppercase	Lowercase	Q_a

This notation will be of help when modeling the devices. For example, consider the portion of the MOS model that relates the drain-source current to the various terminal voltages. This model will be developed in terms of the total instantaneous variables (i_D). For biasing purposes, the dc variables (I_D) will be used; for small signal analysis, the ac variables (i_d); and finally, the small signal frequency discussion will use the complex variable (I_d).

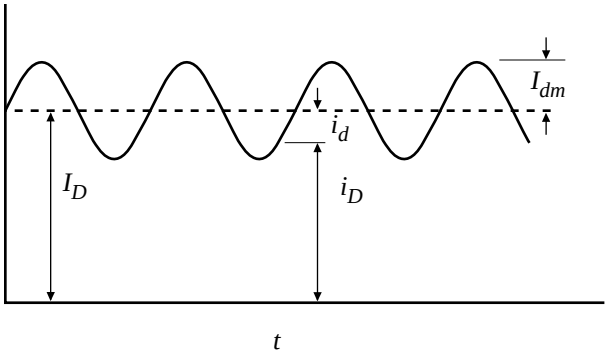

Figure 1.2-1 Notation for signals.

The second item to be discussed here is what symbols are used for the various components. (Most of these symbols will already be familiar to the reader. However, inconsistencies exist about the MOS symbol shown in Fig. 1.2-2.) The symbols shown in Figs. 1.2-2(a) and 1.2-2(b) are used for enhancement-mode MOS transistors when the substrate or bulk (*B*) is connected to the appropriate supply. Most often, the appropriate supply is the most positive one for p-channel transistors and the most negative one for n-channel transistors. Although the transistor operation will be explained later, the terminals are called *drain* (*D*), *gate* (*G*), and *source* (*S*). If the bulk is not connected to the appropriate supply, then the symbols shown in Fig. 1.2-2(c) and Fig. 1.2-2(d) are used for the enhancement-mode MOS transistors. It will be important to know where the bulk of the MOS transistor is connected when it is used in circuits.

Figure 1.2-3 shows another set of symbols that should be defined. Figure 1.2-3(a) represents a differential-input operational amplifier, or in some instances, a comparator which may have a gain approaching that of the operational amplifier. Figures 1.2-3(b) and (c) represent an independent voltage and current source. Sometimes, the battery symbol is used instead of Fig. 1.2-3(b). Finally, Figures 1.2-3(d) through (g) represent the four types of ideal controlled sources. Figure 1.2-3(d) is a voltage-controlled, voltage source (VCVS), Fig. 1.2-3(e) is a voltage-controlled, current source (VCCS), Fig. 1.2-3(f) is a current-

controlled, voltage source (CCVS), and Fig. 1.2-3(g) is a current-controlled, current source (CCCS). The gains of each of these controlled sources are given by the symbols A_v, G_m, R_m, and A_i (for the VCVS, VCCS, CCVS, and CCCS, respectively).

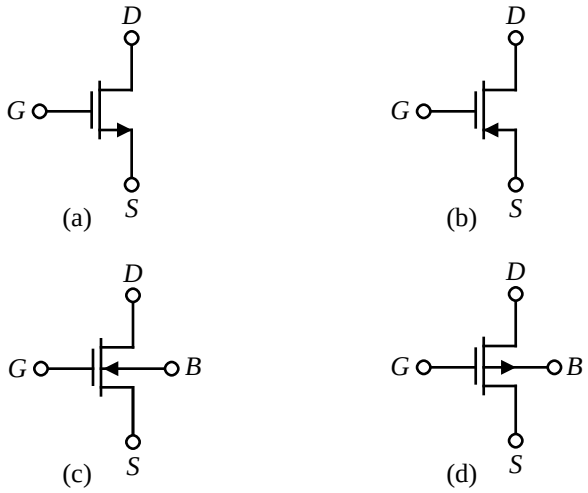

Figure 1.2-2 MOS device symbols. (a) Enhancement n-channel transistor with bulk connected to most negative supply. (b) Enhancement p-channel transistor with bulk connected to most positive supply. (c) and (d) same as (a) and (b) except bulk connection is not constrained to respective supply.

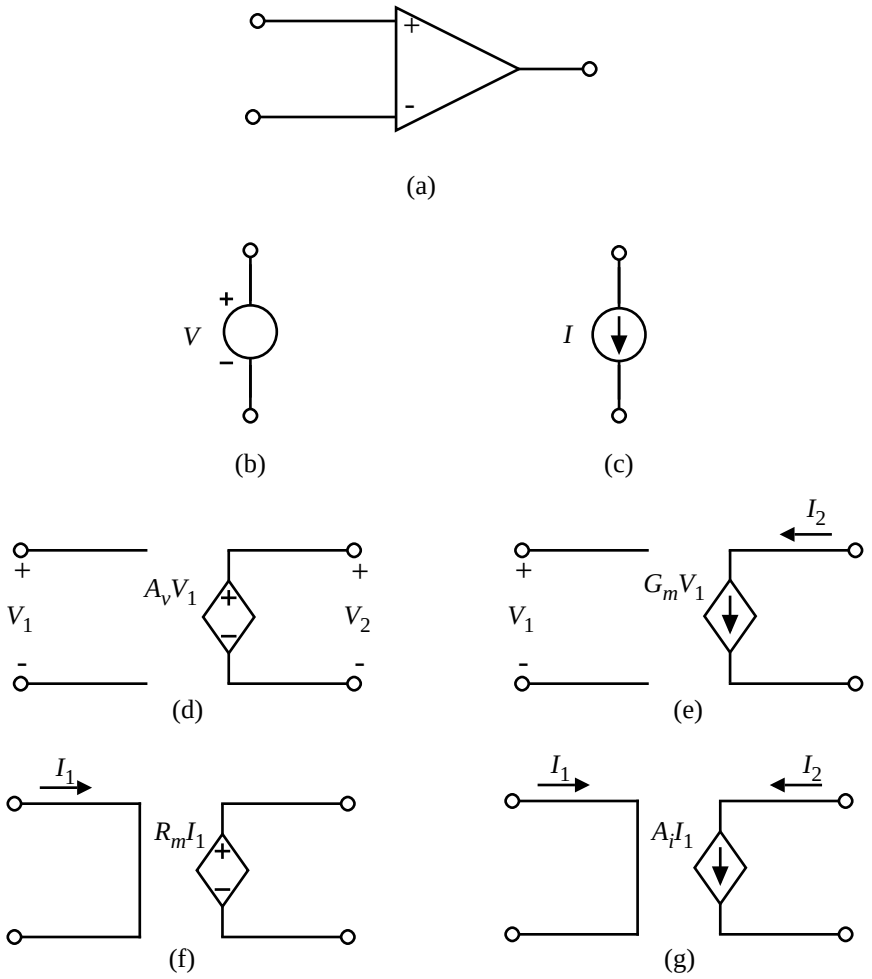

Figure 1.2-3 (a) Symbol for an operational amplifier. (b) Independent voltage source. (c) Independent current source. (d) Voltage-controlled voltage source (VCVS). (e) Voltage-controlled current source (VCCS). (f) Current-controlled voltage source (CCVS). (g) Current-controlled current source (CCCS).

1.3 Analog Signal Processing

Before beginning an in-depth study of analog-circuit design, it is worthwhile considering the application of such circuits. The general subject of analog signal processing includes most of the circuits and systems that will be presented in this text. Figure 1.3-1 shows a simple block diagram of a typical signal-processing system. In the past, such a signal-processing system required multiple integrated circuits with considerable additional passive components. However, the advent of analog sampled-data techniques and MOS technology has made viable the design of a general signal processor using both analog and digital techniques on a single integrated circuit [2].

The first step in the design of an analog signal-processing system is to examine the specifications and decide what part of the system should be analog and what part should be digital. In most cases, the input signal is analog. It could be a speech signal, a sensor output, a radar return, and so forth. The first block of Fig. 1.3-1 is a preprocessing block. Typically, this block will consist of filters, an automatic-gain-control circuit, and an analog-

to-digital converter (ADC or A/D). Often, very strict speed and accuracy requirements are placed on the components in this block. The next block of the analog signal processor is a digital signal processor. The advantage of performing signal processing in the digital domain are numerous. One advantage is due to the fact that digital circuitry is easily implemented in the smallest geometry processes available providing a cost and speed advantage. Another advantage relates to the additional degrees of freedom available in digital signal processing (e.g., linear-phase filters). Additional advantages lie in the ability to easily program digital devices. Finally, it may be necessary to have an analog output. In this case, a postprocessing block is necessary. It will typically contain a digital-to-analog converter (DAC or D/A), amplification, and filtering.

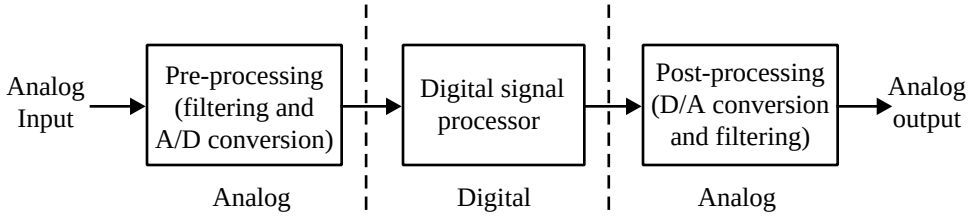

Figure 1.3-1 A typical signal-processing system block diagram.

In a signal processing system, one of the important system consideration is the bandwidth of the signal to be processed. A graph of the operating frequency of a variety of signals is given in Fig. 1.3-2. At the low end are seismic signals, which do not extend much below 1 Hz because of the absorption characteristics of the earth. At the other extreme are microwave signals. These are not used much above 30 GHz because of the difficulties in performing even the simplest forms of signal processing at higher frequencies.

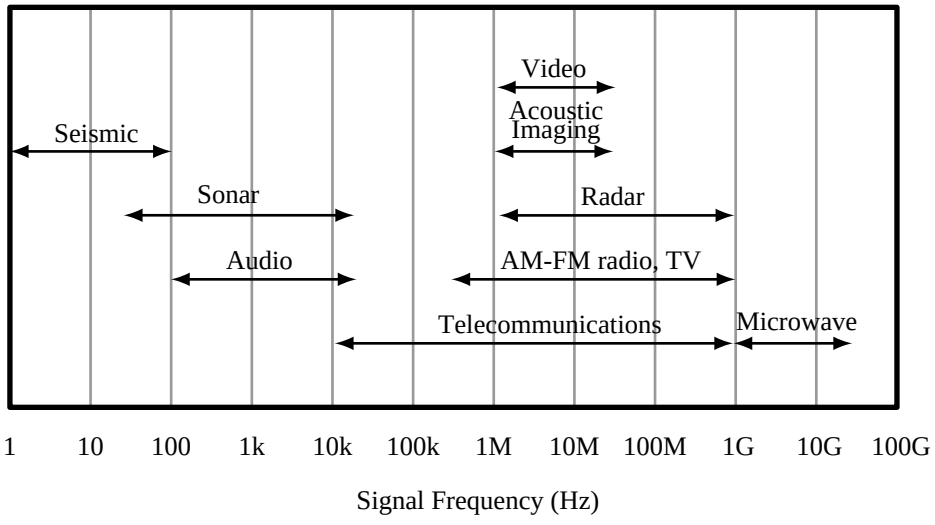

Figure 1.3-2 Frequency of signals used in signal processing applications.

To address any particular application area illustrated in Fig 1.3-2 a technology that can support the required signal bandwidth must be used. Figure 1.3-3 illustrates the speed capabilities of the various process technologies available today. Bandwidth requirements and speed are not the only considerations when deciding which technology to use for an

integrated circuit addressing an application area. Other considerations are cost and integration. The clear trend today is to use CMOS digital combined with CMOS analog (as needed) whenever possible because significant integration can be achieved thus providing highly reliable compact system solutions.

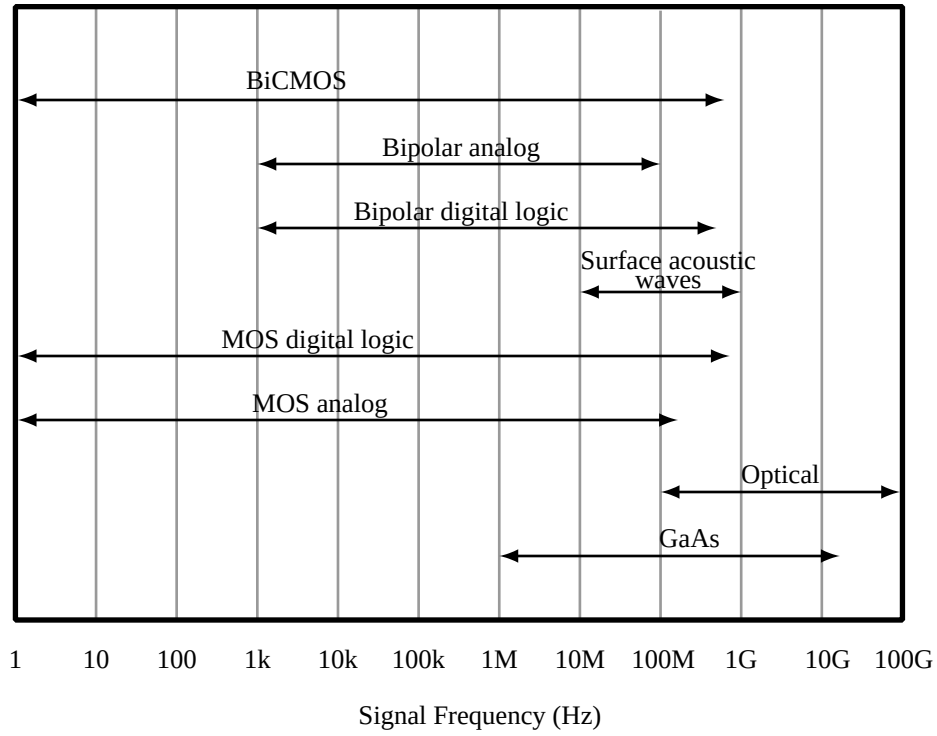

Figure 1.3-3 Frequencies that can be processed by present-day technologies.

1.4 Example of Analog VLSI Mixed-Signal Circuit Design

Analog circuit design methodology is best illustrated by example. Figure 1.4-1 shows the block diagram of a fully-integrated digital read/write channel for disk drive recording applications. The device employs partial response maximum likelihood (PRML) sequence detection when reading data to enhance bit-error-rate versus signal-to-noise ratio performance. The device supports data rates up to 64 Mbits/sec and is fabricated in a 0.8 μm double-metal CMOS process.

In a typical application, this IC receives a fully-differential analog signal from an external preamplifier which senses magnetic transitions on a spinning disk-drive platter. This differential read pulse is first amplified by a variable gain amplifier (VGA) under control of a real-time digital gain-control loop. After amplification, the signal is passed to a 7-pole 2-zero equiripple-phase low-pass filter. The zeros of the filter are real and symmetrical about the imaginary axis. The location of the zeros relative to the location of the poles is programmable and are designed to boost filter gain at high frequencies and thus narrow the width of the read pulse.

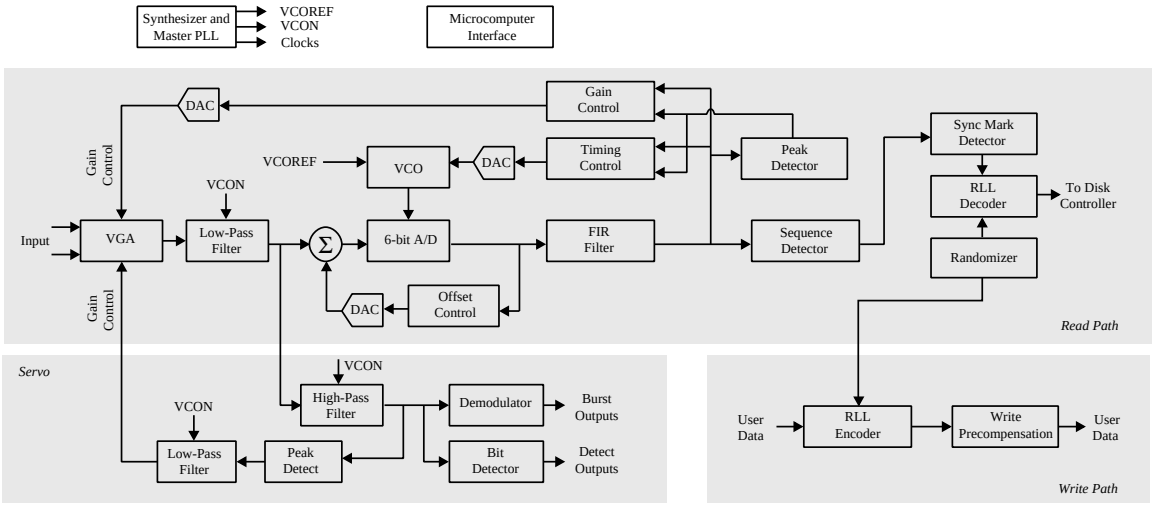

Figure 1.4-1 Read/Write channel integrated circuit block diagram.

The low-pass filter is constructed from transconductance stages (g_m stages) and capacitors. A one-pole prototype illustrating the principles embodied in the low-pass filter design is shown in Fig. 1.4-2. While the relative pole arrangement is fixed, two mechanisms are available for scaling the low-pass filter's frequency response. The first is via a control voltage (labeled "VCON") which is common to all of the transconductance stages in the filter. This control voltage is applied to the gate of an n-channel transistor in each of the transconductance stages. The conductance of each of these transistors determines the overall conductance of its associated stage and can be continuously varied by the control voltage. The second frequency response control mechanism is via the digital control of the value of the capacitors in the low-pass filter. All capacitors in the low-pass filter are constructed identically, and each consists of a programmable array of binarily weighted capacitors.

The continuous control capability via VCON designed into the transconductance stage provides for a means to compensate for variations in the low-pass filter's frequency response due to process, temperature, and supply voltage changes [3]. The control-voltage, VCON, is derived from the "Master PLL" composed of a replica of the filter configured as a voltage-controlled oscillator in a phase-locked-loop configuration as illustrated in Fig. 1.4-3. The frequency of oscillation is inversely proportional to the characteristic time constant, C/g_m , of the replica filter's stages. By forcing the oscillator to be phase and frequency-locked to an external frequency reference through variation of the VCON terminal voltage, the characteristic time constant is held fixed. To the extent that the circuit elements in the low-pass filter match those in the master filter, the characteristic time constants of the low-pass filter (and thus the frequency response) are also fixed.

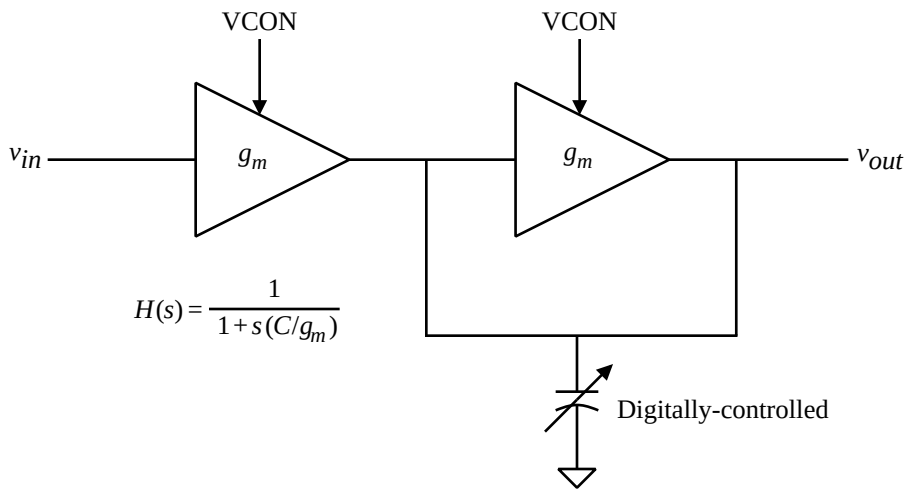

Figure 1.4-2 Single-pole low-pass filter.

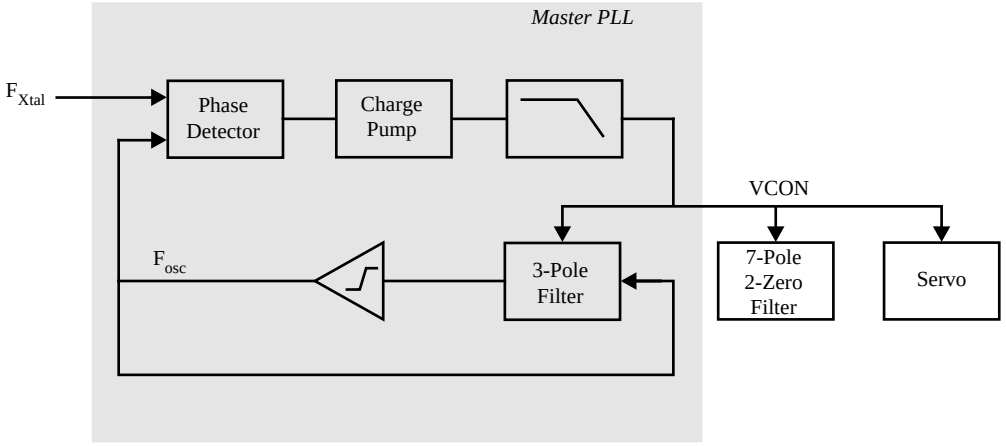

Figure 1.4-3 Master filter phase-locked loop.

The normal output of the low-pass filter is passed through a buffer to a 6-bit one-step-flash sampling A/D converter. The A/D is clocked by a voltage-controlled oscillator (VCO) whose frequency is controlled by a digital timing-recovery loop. Each of the sixty-three comparators in the flash A/D converter contains capacitors to sample the buffered analog signal from the low-pass filter. While sampling the signal each capacitor is also absorbing the comparator's offset voltage to correct for distortion errors these offsets would otherwise cause [4]. The outputs from the comparators are passed through a block of logic that checks for invalid patterns, which could cause severe conversion errors if left unchecked [5]. The outputs of this block are then encoded into a 6-bit word.

As illustrated in Fig. 1.4-1, after being digitized, the 6-bit output of the A/D converter is filtered by a finite-impulse-response (FIR) filter. The digital gain and timing control loops mentioned above monitor the raw digitized signal or the FIR filter output for gain and timing errors. Because these errors can only be measured when signal pulses occur, a digital transition detector is provided to detect pulses and activate the gain and timing error detectors. The gain and timing error signals are then passed through digital low-pass filters and subsequently to D/A converters in the analog circuitry to adjust the VGA gain and A/D VCO frequency, respectively.

The heart of the read channel IC is the sequence detector. The detector's operation is based on the Viterbi algorithm, which is generally used to implement maximum likelihood detection. The detector anticipates linear inter-symbol interference and after processing the received sequence of values deduces the most likely transmitted sequence (i.e., the data read from the media) as in [6]. The bit stream from the sequence detector is passed to the run-length-limited (RLL) decoder block where it is decoded. If the data written to the disk were randomized before being encoded, the inverse process is applied before the bit stream appears on the read channel output pins.

The write-path is illustrated in detail in Fig. 1.4-4. In write mode, data is first encoded by an RLL encoder block. The data can optionally be randomized before being sent to the encoder. When enabled, a linear feedback shift register is used to generate a pseudo-random pattern that is XOR'd with the input data. Using the randomizer insures that bit patterns that may be difficult to read occur no more frequently than would be expected from random input data.

A write clock is synthesized to set the data rate by a VCO placed in a phase-locked-loop. The VCO clock is divided by a programmable value "M," and the divided clock is phase-locked to an external reference clock divided by two and a programmable value "N." The result is a write clock at a frequency M/2N times the reference clock frequency. The values for M and N can each range from 2 to 256, and write clock frequencies can be synthesized to support zone-bit-recording designs, wherein zones on the media having different data rates are defined.

Encoded data are passed to the write precompensation circuitry. While linear bit-shift effects caused by inter-symbol interference need not be compensated in a PRML channel, non-linear effects can cause a shift in the location of a magnetic transition caused by writing a one in the presence of other nearby transitions. Although the particular RLL code implemented prohibits two consecutive 'ones' (and therefore two transitions in close proximity) from being written, a 'one/zero/one' pattern can still create a measurable shift in the second transition. The write precompensation circuitry delays the writing of the second 'one' to counter the shift. The synthesized write clock is input to two delay lines, each constructed from stages similar to those found in the VCO. Normally the signal from one delay line is used to clock the channel data to the output drivers. However, when a 'one/zero/one' pattern is detected, the second 'one' is clocked to the output drivers by the signal from the other delay line. This second delay line is current-starved, thus exhibiting a longer delay than the first, and the second 'one' in the pattern is thereby delayed. The amount of delay is programmable.

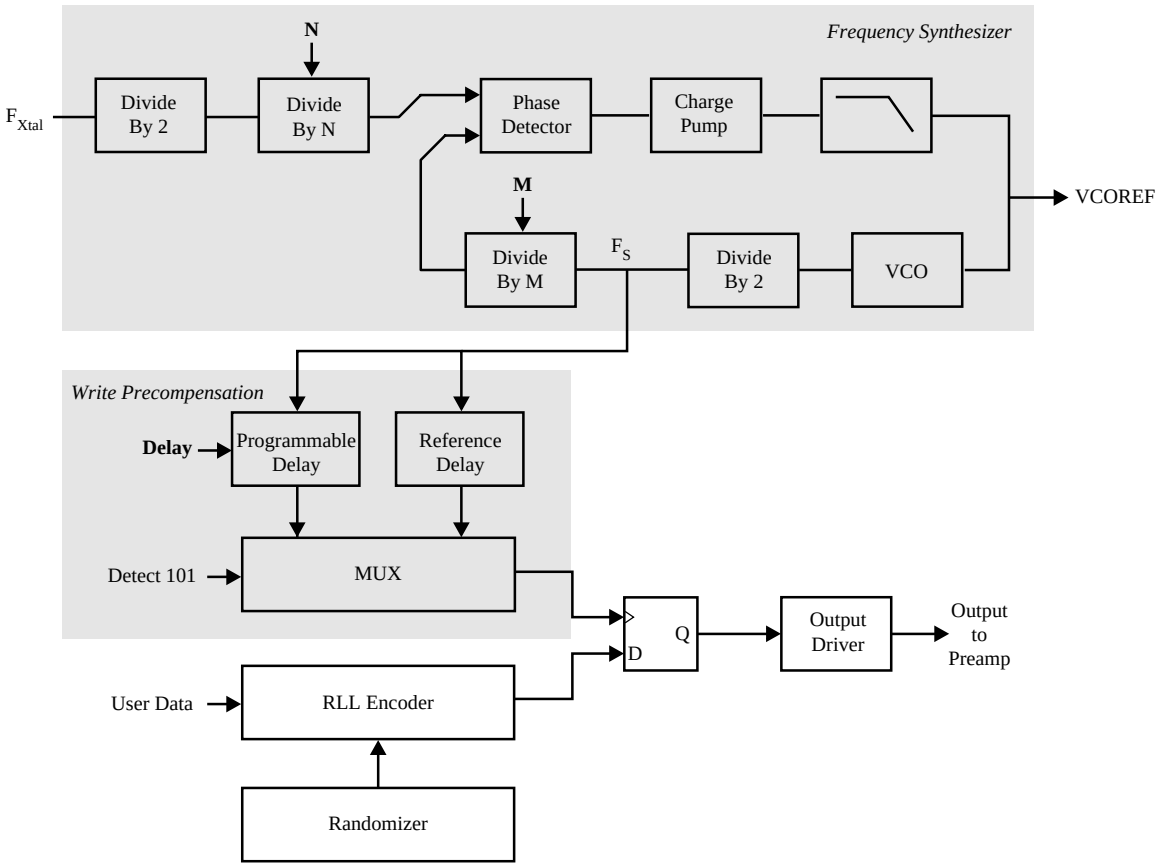

Figure 1.4-4 Frequency synthesizer and write-data path.

The servo channel circuitry, shown in Fig. 1.4-5, is used for detecting embedded head positioning information. There are three main functional blocks in the servo section. They are:

- Automatic gain control loop (AGC)
- Bit detector
- Burst demodulator

Time constants and charge rates in the servo section are programmable and controlled by the master filter to avoid variation due to supply voltage, process, and temperature. All blocks are powered down between servo fields to conserve power.

The AGC loop feedback around the VGA forces the output of the high-pass filter to a constant level during the servo preamble. The preamble consists of an alternating bit pattern and defines the 100% full-scale level. To avoid the need for timing acquisition, the servo AGC loop is implemented in the analog domain. The peak amplitude at the output of the high-pass filter is detected with a rectifying peak detector. The peak detector either charges or discharges a capacitor, depending on whether the input signal is above or below the held value on the capacitor. The output of the peak detector is compared to a full-scale reference and integrated to control the VGA gain. The relationship between gain and control voltage for the VGA is an exponential one, thus the loop dynamics are independent of gain. The

burst detector is designed to detect and hold the peak amplitude of up to four servo positioning bursts, indicating the position of the head relative to track center.

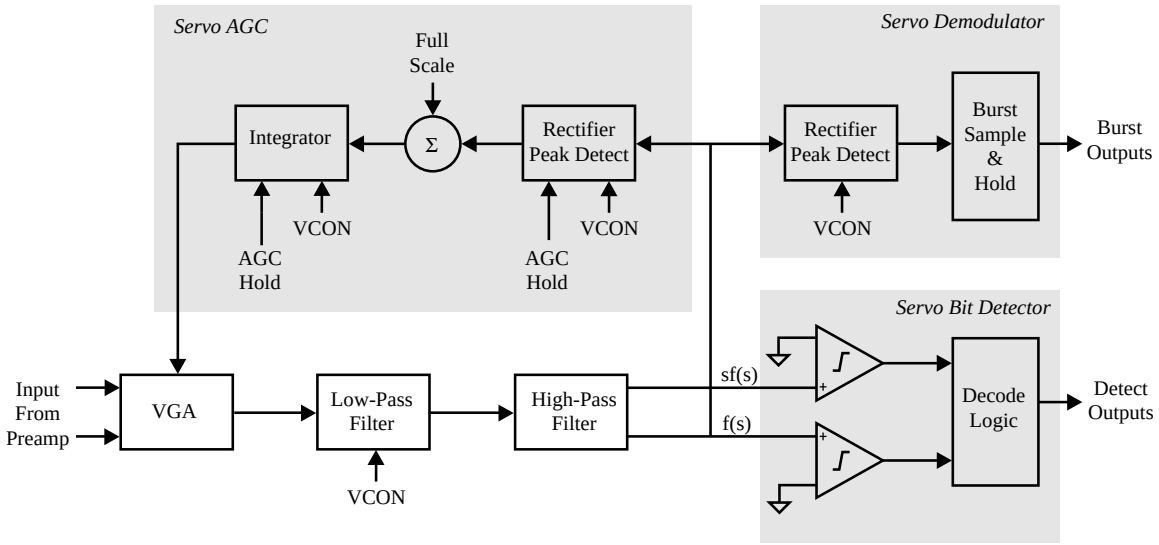

Figure 1.4-5 Servo channel block diagram.

An asynchronous bit detector is included to detect the servo data information and address mark. Input pulses are qualified with a programmable threshold comparator such that a pulse is detected only for those pulses whose peak amplitude exceeds the threshold. The servo bit detector provides outputs indicating both zero-crossing events and the polarity of the detected event.

Figure 1.4-6 shows a photomicrograph of the read-channel chip described. The circuit was fabricated in a single-polysilicon, double-metal, 0.8 μm CMOS process.

1.5 Summary

This chapter has presented an introduction to the design of CMOS analog integrated circuits. Section 1.1 gave a definition of signals in analog circuits and defined analog, digital, and analog sampled-data signals. The difference between analysis and design was discussed. The design differences between discrete and integrated analog circuits are primarily due to the designer's control over circuit geometry and the need to computer-simulate rather than build a breadboard. The first section also presented an overview of the text and showed in Table 1.1-2 how the various chapters tied together. It is strongly recommended that the reader refer to Table 1.1-2 at the beginning of each chapter.

Section 1.2 discussed notation, symbology, and terminology. Understanding these topics is important to avoid confusion in the presentation of the various subjects. The choice of symbols and terminology has been made to correspond with standard practices and definitions. Additional topics concerning the subject in this section will be given in the text at the appropriate place.

An overview of analog signal processing was presented in Section 1.3. The objective of most analog circuits was seen to be the implementation of some sort of analog signal processing. The important concepts of circuit application, circuit technology, and system bandwidth were introduced and interrelated, and it was pointed out that analog circuits rarely stand alone but are usually combined with digital circuits to accomplish some form

of signal processing. The boundaries between the analog and digital parts of the circuit depend upon the application, the performance, and the area.

Section 1.4 gave an example of the design of a fully-integrated disk-drive read-channel circuit. The example emphasized the hierarchical structure of the design and showed how the subjects to be presented in the following chapters could be used to implement a complex design.

Before beginning the study of the following chapters, the reader may wish to study Appendix A, which presents material that should be mastered before going further. It covers the subject of circuit analysis for analog-circuit design, and some of the problems at the end of this chapter refer to this material. The reader may also wish to review other subjects, such as electronic modeling, computer-simulation techniques, Laplace and *z*-transform theory, and semiconductor-device theory.

PROBLEMS

1. Using Eq. (1) of Sec 1.1, give the base-10 value for the 5-bit binary number 11010 (b_4 b_3 b_2 b_1 b_0 ordering).
2. Process the sinusoid in Fig. P1.2 through an analog sample and hold. The sample points are given at each integer value of t/T.

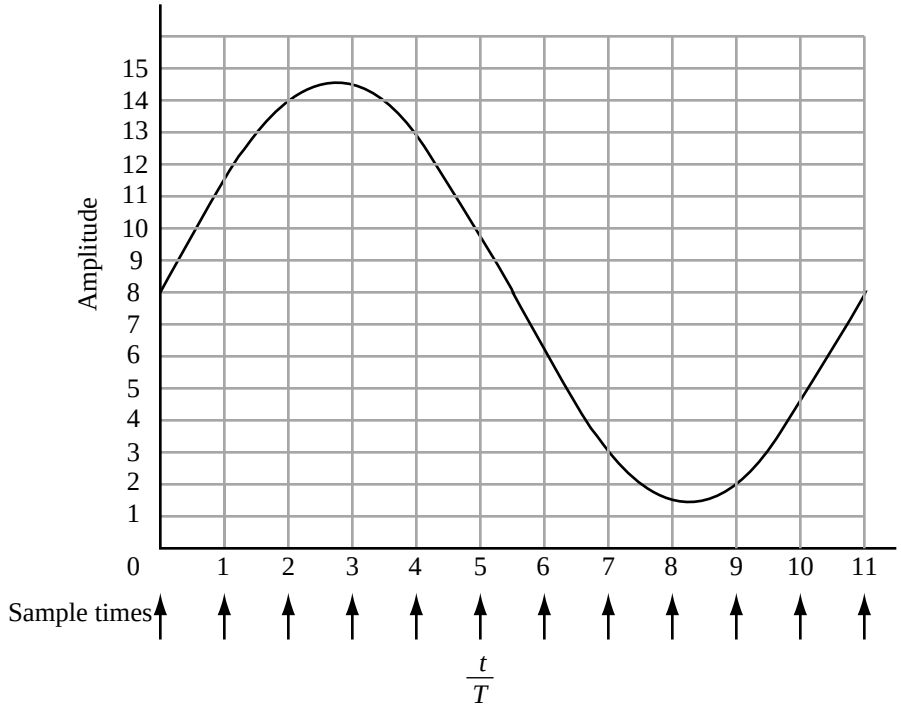

Figure P1.2

3. Digitize the sinusoid given in Fig. P1.2 according to Eq. (1) in Sec. 1.1 using a four-bit digitizer.

The following problems refer to material in Appendix A.

4. Use the nodal equation method to find v_{out}/v_{in} of Fig. P1.4.

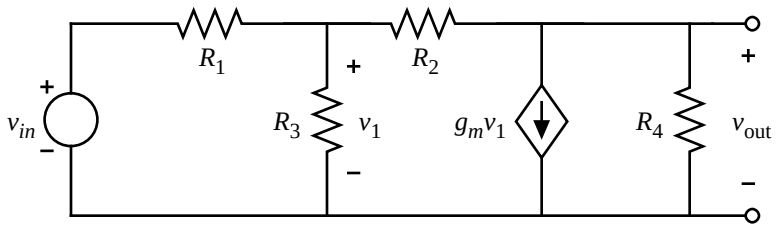

Figure P1.4

5. Use the mesh equation method to find v_{out}/v_{in} of Fig. P1.4.
6. Use the source rearrangement and substitution concepts to simplify the circuit shown in Fig. P1.6 and solve for i_{out}/i_{in} by making chain-type calculations only.

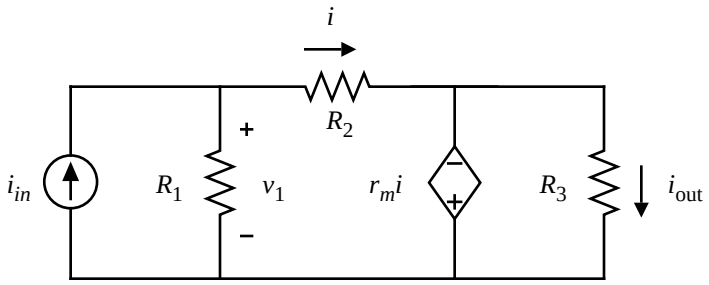

Figure P1.6

7. Find v_2/v_1 and v_1/i_1 of Fig. P1.7.

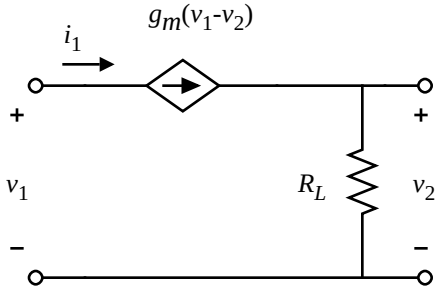

Figure P1.7

8. Use the circuit-reduction technique to solve for v_{out}/v_{in} of Fig. P1.8.

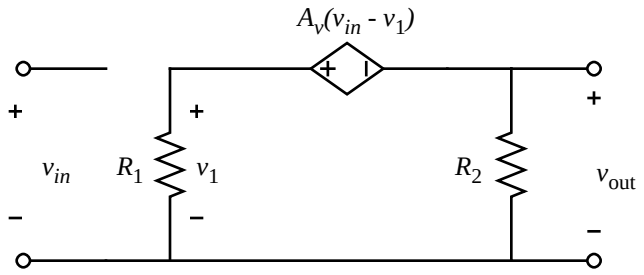

Figure P1.8

9. Use the Miller simplification concept to solve for v_{out}/v_{in} of Fig. A-3 (see Appendix A).
10. Find v_{out}/i_{in} of Fig. A-12 and compare with the results of Example A-1.
11. Use the Miller simplification technique described in Appendix A to solve for the output resistance, v_o/i_o, of Fig. P1.4. Calculate the output resistance not using the Miller simplification and compare your results.
12. Consider an ideal voltage amplifier with a voltage gain of $A_v = 0.99$. A resistance R = 50 kΩ is connected from the output back to the input. Find the input resistance of this circuit by applying the Miller simplification concept.

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Chapter 2 CMOS Technology

The two most prevalent integrated-circuit technologies are bipolar and MOS. Within each of these families are various subgroups as illustrated in Fig. 2.0-1, which shows a family tree of some of the more widely used silicon integrated-circuit technologies. For many years the dominant silicon integrated-circuit technology was bipolar, as evidenced by the ubiquitous monolithic operational amplifier and the TTL (transistor-transistor logic) family. In the early 1970s MOS technology was demonstrated to be viable in the area of dynamic random-access memories (DRAMs), microprocessors, and the 4000-series logic family. By the end of the 1970s, driven by the need for density, it was clear that MOS technology would be the vehicle for growth in the digital VLSI area. At this same time, several organizations were attempting analog circuit designs using MOS [1,2,3,4]. NMOS technology was the early technology of choice for the majority of both digital and analog MOS designs. The early 1980s saw the movement of the VLSI world toward silicon-gate CMOS which has been the dominant technology for VLSI digital and mixed-signal designs ever since [5,6]. Recently, processes that combine both CMOS and bipolar (BiCMOS) have proven themselves to be both a technological and market success where the primary market force has been improved speed for digital circuits (primarily in static random-access memories, SRAMs). BiCMOS has potential as well in analog design due to the enhanced performance that a bipolar transistor provides in the context of CMOS technology. This book focuses on the use of CMOS for analog and mixed-signal circuit design.

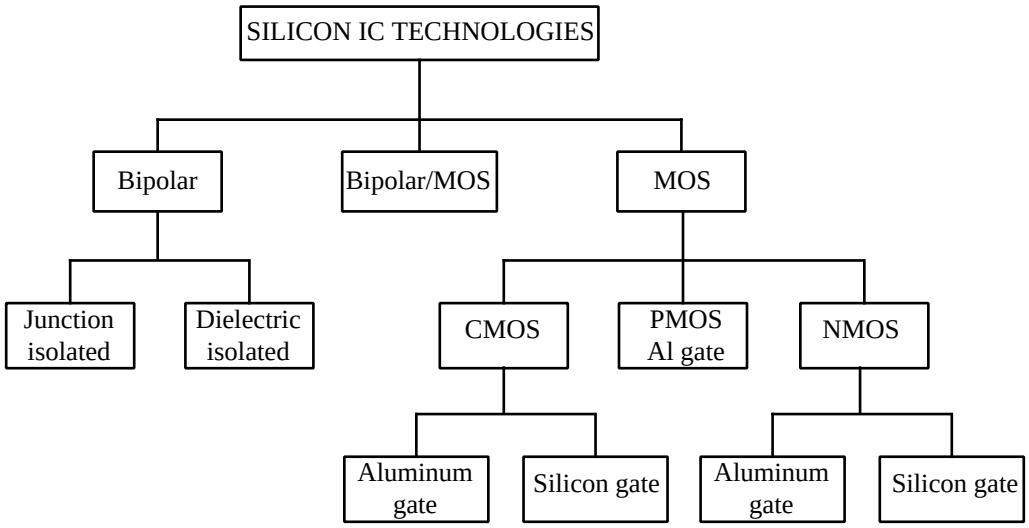


Figure 2.0-1 Categories of silicon technology

There are numerous references that develop the details of the physics of MOS device operation [7,8]. Therefore, this book covers only the aspects of this theory which are pertinent to the viewpoint of the circuit designer. The objective is to be able to appreciate the limits of the MOS circuit models developed in the next chapter and to understand the physical constraints on electrical performance.

This chapter covers various aspects of the CMOS process from a physical point of view. In order to understand CMOS technology, a brief review of the basic semiconductor fabrication processes is presented, followed by a description of the

fabrication steps required to build the basic CMOS process. Next, the pn junction is presented and characterized. This discussion is followed by a description of how active and passive components compatible with the CMOS technology are built. Next, important limitations on the performance of CMOS technology including latch-up, temperature dependence, and noise are covered. Finally, this chapter deals with the topological rules employed when drawing the integrated circuit for subsequent fabrication.

2.1 Basic MOS Semiconductor Fabrication Processes

Semiconductor technology is based on a number of well-established process steps, which are the means of fabricating semiconductor components. In order to understand the fabrication process, it is necessary to understand these steps. The process steps described here include: *oxidation, diffusion, ion implantation, deposition, and etching.* The means of defining the area of the semiconductor subject to processing is called *photolithography*.

All processing starts with single-crystal silicon material. There are two methods of growing such crystals [9]. Most of the material is grown by a method based on that developed by Czochralski in 1917. A second method, called the float zone technique, produces crystals of high purity and is often used for power devices. The crystals are normally grown in either a <100> or <111> crystal orientation. The resulting crystals are cylindrical and have a diameter of 75-200 mm and a length of 1 m. The cylindrical crystals are sliced into wafers which are approximately 0.5 to 0.7 mm thick for wafers of size 100 mm to 150 mm respectively [10]. This thickness is determined primarily by the physical strength requirements. When the crystals are grown, they are doped with either an n-type or p-type impurity to form a n- or p-substrate. The substrate is the starting material in wafer form for the fabrication process. The doping level of most substrates is approximately 10^{15} impurity atoms/cm^3, which roughly corresponds to a resistivity of 3-5 Ω-cm for an n-substrate and 14-16 Ω-cm for a p-substrate [11].

An alternative to starting with a lightly-doped silicon wafer is to use a heavily-doped wafer that has a lightly-doped epitaxial on top of it where subsequent devices are formed. Although *epi* wafers are more expensive, they can provide some benefits by reducing sensitivity to latchup (discussed later) and reduce interference between analog and digital circuits on mixed-signal integrated circuits.

The five basic processing steps which are applied to the doped silicon wafer to fabricate semiconductor components (oxidation, diffusion, ion implantation, deposition, and etching) will be described in the following paragraphs.

Oxidation

The first basic processing step is oxide growth or oxidation [12]. Oxidation is the process by which a layer of silicon dioxide (SiO_2) is formed on the surface of the silicon wafer. The oxide grows both into as well as on the silicon surface as indicated in Fig. 2.1-1. Typically about 56% of the oxide thickness is above the original surface while about 44% is below the original surface. The oxide thickness, designated t_{ox}, can be grown using either dry or wet techniques, with the former achieving lower defect densities. Typically oxide thickness varies from less than 150 Å for gate oxides to more than 10,000 Å for field oxides. Oxidation takes place at temperatures ranging from 700 °C to 1100 °C with the resulting oxide thickness being proportional to the temperature at which it is grown (for a fixed amount of time).

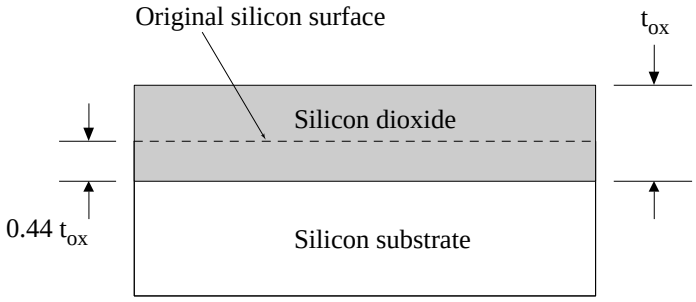


Figure 2.1-1 Silicon dioxide growth at the surface of a silicon wafer.

Diffusion

The second basic processing step is diffusion [13]. Diffusion in semiconductor material is the movement of impurity atoms at the surface of the material into the bulk of the material. Diffusion takes place at temperatures in the range of 800 °C to 1400 °C in the same way as a gas diffuses in air. The concentration profile of the impurity in the semiconductor is a function of the concentration of the impurity at the surface and the time in which the semiconductor is placed in a high-temperature environment. There are two basic types of diffusion mechanisms which are distinguished by the concentration of the impurity at the surface of the semiconductor. One type of diffusion assumes that there is an infinite source of impurities at the surface (N_0 cm^{-3}) during the entire time the impurity is allowed to diffuse. The impurity profile for an infinite-source impurity as a function of diffusion time is given in Fig. 2.1-2(a). The second type of diffusion assumes that there is a finite source of impurities at the surface of the material initially. At $t = 0$ this value is given by N_0. However, as time increases, the impurity concentration at the surface decreases as shown in Fig. 2.1-2(b). In both cases, N_B is the pre-diffusion impurity concentration of the semiconductor.

The infinite-source and finite-source diffusions are typical of predeposition and drive-in diffusions, respectively. The object of a predeposition diffusion is to place a large concentration of impurities near the surface of the material. There is a maximum impurity concentration that can be diffused into silicon depending upon the type of impurity. This maximum concentration is due to the solid solubility limit which is in the range of 5×10^{20} to 2×10^{21} atoms/cm^3. The drive-in diffusion follows the deposition diffusion and is used to drive the impurities deeper into the semiconductor. The crossover between the pre-diffusion impurity level and the diffused impurities of the opposite type defines the semiconductor junction. This junction is between a p-type and n-type material and is simply called a *pn junction*. The distance between the surface of the semiconductor and the junction is called the *junction depth*. Typical junction depths for diffusion can range from 0.1 μm for predeposition type diffusions to greater than 10 μm for drive-in type diffusions.

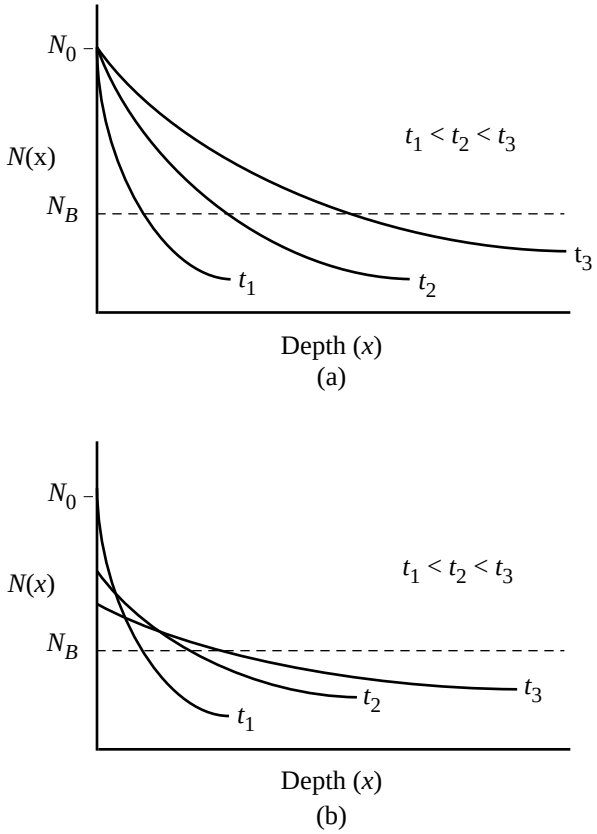


Figure 2.1-2 Diffusion profiles as a function of time for (a) infinite-source of impurities at the surface, and (b) a finite source of impurities at the surface.

Ion Implantation

The next basic processing step is ion implantation and is widely used in the fabrication of MOS components [14,15]. Ion implantation is the process by which ions of a particular dopant (impurity) are accelerated by an electric field to a high velocity and physically lodge within the semiconductor material. The average depth of penetration varies from 0.1 to 0.6 μm depending on the velocity and angle at which the ions strike the silicon wafer. The path of each ion depends upon the collisions it experiences. Therefore, ions are typically implanted off-axis from the wafer so that they will experience collisions with lattice atoms thus avoiding undesirable *channeling* of ions deep into the silicon. An alternative method to address channeling is to implant through silicon dioxide which randomizes the implant direction before the ions enter the silicon. The ion-implantation process causes damage to the semiconductor crystal lattice leaving many of the implanted ions electrically inactive. This damage can be repaired by an annealing process in which the temperature of the semiconductor after implantation is raised to around 800 °C to allow the ions to move to electrically active locations in the semiconductor crystal lattice.

Ion implantation can be used in place of diffusion since in both cases the objective is to insert impurities into the semiconductor material. Ion implantation has several advantages over thermal diffusion. One advantage is the accurate control of doping—to within ±5%. Reproducibility is very good, making it possible to adjust the thresholds of MOS devices or to create precise resistors. A second advantage is that ion implantation is

a room-temperature process, although annealing at higher temperatures is required to remove the crystal damage. A third advantage is that it is possible to implant through a thin layer. Consequently, the material to be implanted does not have to be exposed to contaminants during and after the implantation process. Unlike ion implantation, diffusion requires that the surface be free of silicon dioxide or silicon nitride layers. Finally, ion implantation allows control over the profile of the implanted impurities. For example, a concentration peak can be placed below the surface of the silicon if desired.

Deposition

The fourth basic semiconductor process is deposition. Deposition is the means by which films of various materials may be deposited on the silicon wafer. These films may be deposited using several techniques which include deposition by evaporation [16], sputtering [17], and chemical-vapor deposition (CVD) [18,19]. In evaporation deposition, a solid material is placed in a vacuum and heated until it evaporates. The evaporant molecules strike the cooler wafer and condense into a solid film on the wafer surface. Thickness of the deposited materiel is determined by the temperature and the amount of time evaporation is allowed to take place (a thickness of 1 μm is typical). The sputtering technique uses positive ions to bombard the cathode, which is coated with the material to be deposited. The bombarded or target material is dislodged by direct momentum transfer and deposited on wafers which are placed on the anode. The types of sputtering systems used for depositions in integrated circuits include dc, radio frequency (RF), or magnetron (magnetic field). Sputtering is usually done in a vacuum. Chemical vapor deposition uses a process in which a film is deposited by a chemical reaction or pyrolytic decomposition in the gas phase which occurs in the vicinity of the silicon wafer. This deposition process is generally used to deposit polysilicon, silicon dioxide (SiO_2), or silicon nitride (Si_3N_4). While the chemical vapor deposition is usually performed at atmospheric pressure, it can also be done at low pressures where the diffusivity increases significantly. This technique is called low-pressure chemical-vapor deposition (LPCVD).

Etching

The final basic semiconductor fabrication process considered here is etching. Etching is the process of removing exposed (unprotected) material. The means by which some material is exposed and some is not will be considered next in discussing the subject of photolithography. For the moment, we will assume that the situation illustrated in Fig. 2.1-3(a) exists. Here we see a top layer called a film and an underlying layer. A protective layer, called a mask[i], covers the film except in the area which is to be etched. The objective of etching is to remove just the section of the exposed film. To achieve this, the etching process must have two important properties: selectivity, and anisotropy. Selectivity is the characteristic of the etch whereby only the desired layer is etched with no effect on either the protective layer (masking layer) or the underlying layer. Selectivity can quantified as the ratio of the desired layer etch rate to the undesired layer etch rate as given below.

$$S_{A-B} = \frac{\text{Desired layer etch rate (A)}}{\text{Undesired layer etch rate (B)}} \qquad (1)$$

[i] A distinction is made between a deposited masking layer referred to as a “mask” and the photographic plate used in exposing the photoresist which is called a “photomask.”

Anisotropy is the property of the etch to manifest itself in one direction, i.e., a perfectly anisotropic etchant will etch in one direction only. The degree of anisotropy can be quantified by the relation given below.

$$A = 1 - \frac{\text{Lateral etch rate}}{\text{Vertical etch rate}} \tag{2}$$

Reality is such that neither perfect selectivity nor perfect anisotropy can be achieved in practice, resulting in undercutting effects and partial removal of the underlying layer as illustrated in Fig. 2.1-3(b). As illustrated, the lack of selectivity with respect to the mask is given by dimension "a." Lack of selectivity with respect to the underlying layer is given by dimension "b." Dimension "c" shows the degree of anisotropy. There are preferential etching techniques which achieve high degrees of anisotropy and thus minimize undercutting effects, as well as maintain high selectivity. Materials which are normally etched include polysilicon, silicon dioxide, silicon nitride, and aluminum.

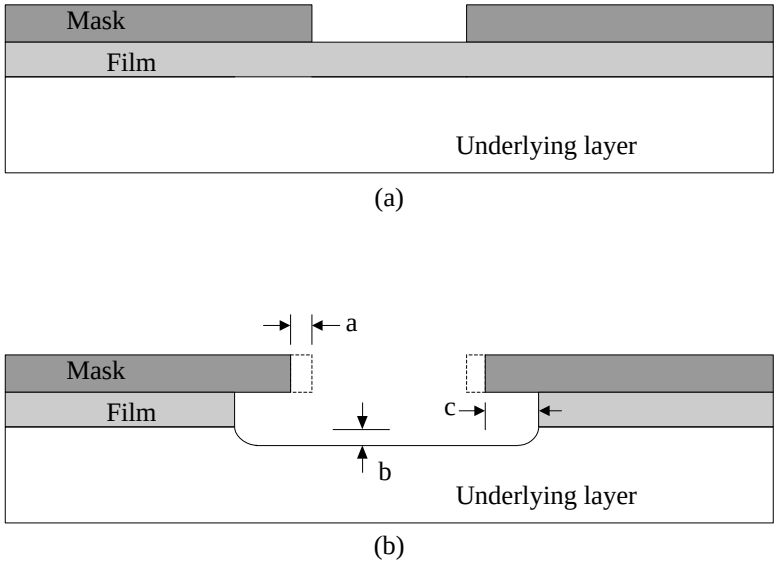


Figure 2.1-3 (a) Portion of the top layer ready for etching. (b) Result of etching indicating horizontal etching and etching of underlying layer.

There are two basic types of etching techniques. *Wet etching* uses chemicals to remove the material to be etched. Hydrofluoric acid (HF) is used to etch silicon dioxide; phosphoric acid (H_3PO_4) is used to remove silicon nitride; nitric acid, acetic acid, or hydrofluoric acid is used to remove polysilicon, potassium hydroxide is used to etch silicon; and a phosphoric acid mixture is used to remove metal. The wet-etching technique is strongly dependent upon time and temperature, and care must be taken with the acids used in wet etching as they represent a potential hazard. *Dry etching* or *plasma etching* uses ionized gases that are rendered chemically active by an RF-generated plasma. This process requires significant characterization to optimize pressure, gas flow rate, gas mixture, and RF power. Dry etching is very similar to sputtering and in fact the same equipment can be used. Reactive ion etching (RIE) induces plasma etching accompanied by ionic bombardment. Dry etching is used for submicron technologies since it achieves anisotropic profiles (no undercutting).

Photolithography

Each of the basic semiconductor fabrication processes discussed thus far is only applied to selected parts of the silicon wafer with the exception of oxidation and deposition. The selection of these parts is accomplished by a process called photolithography [12,20,21]. Photolithography refers to the complete process of transferring an image from a *photomask* or computer database to a wafer. The basic components of photolithography are the photoresist material and the photomask used to expose some areas of the photoresist to ultraviolet (UV) light while shielding the remainder. All integrated circuits consist of various layers which overlay to form the device or component. Each distinct layer must be physically defined as a collection of geometries. This can be done by physically drawing the layer on a large scale and optically reducing it to the desired size. However, the usual technique is to draw the layer using a computer-aided design (CAD) system and store the layer description in electronic data format.

The photoresist is an organic polymer whose characteristics can be altered when exposed to ultraviolet light. Photoresist is classified into positive and negative photoresist. *Positive photoresist* is used to create a mask where patterns exist (where the photomask is opaque to UV light). *Negative photoresist* creates a mask where patterns do not exist (where the photomask is transparent to UV light). The first step in the photolithographic process is to apply the photoresist to the surface to be patterned. The photoresist is applied to the wafer and the wafer spun at several thousand revolutions per minute in order to disperse the photoresist evenly over the surface of the wafer. The thickness of the photoresist depends only upon the angular velocity of the spinning wafer. The second step is to “soft bake” the wafer to drive off solvents in the photoresist. The next step selectively exposes the wafer to UV light. Using positive photoresist, those areas exposed to UV light can be removed with solvents leaving only those areas that were not exposed. Conversely, if negative photoresist is used, those areas exposed to UV light will be made impervious to solvents while the unexposed areas will be removed. This process of exposing and then selectively removing the photoresist is called *developing.* The developed wafer is then “hard baked” at a higher temperature to achieve maximum adhesion of the remaining photoresist. The hardened photoresist protects selected areas from the etch plasma or acids used in the etching process. When its protective function is complete, the photoresist is removed with solvents or plasma ashing that will not harm underlying layers. This process must be repeated for each layer of the integrated circuit. Fig. 2.1-4 shows, by way of example, the basic photolithographic steps in defining a polysilicon geometry using positive photoresist.

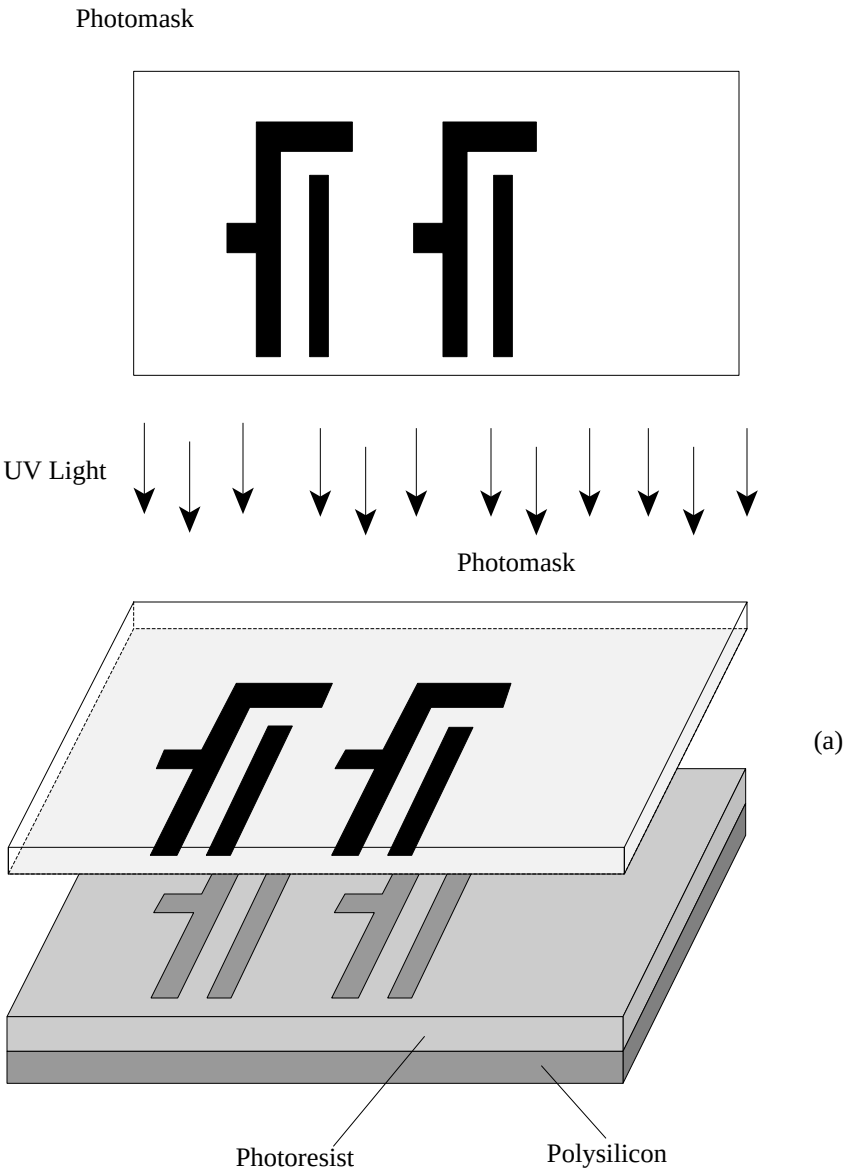


Figure 2.1-4 Basic photolithographic steps to define a polysilicon geometry.
(a) Expose (b) Develop (c) Etch (d) Remove photoresist

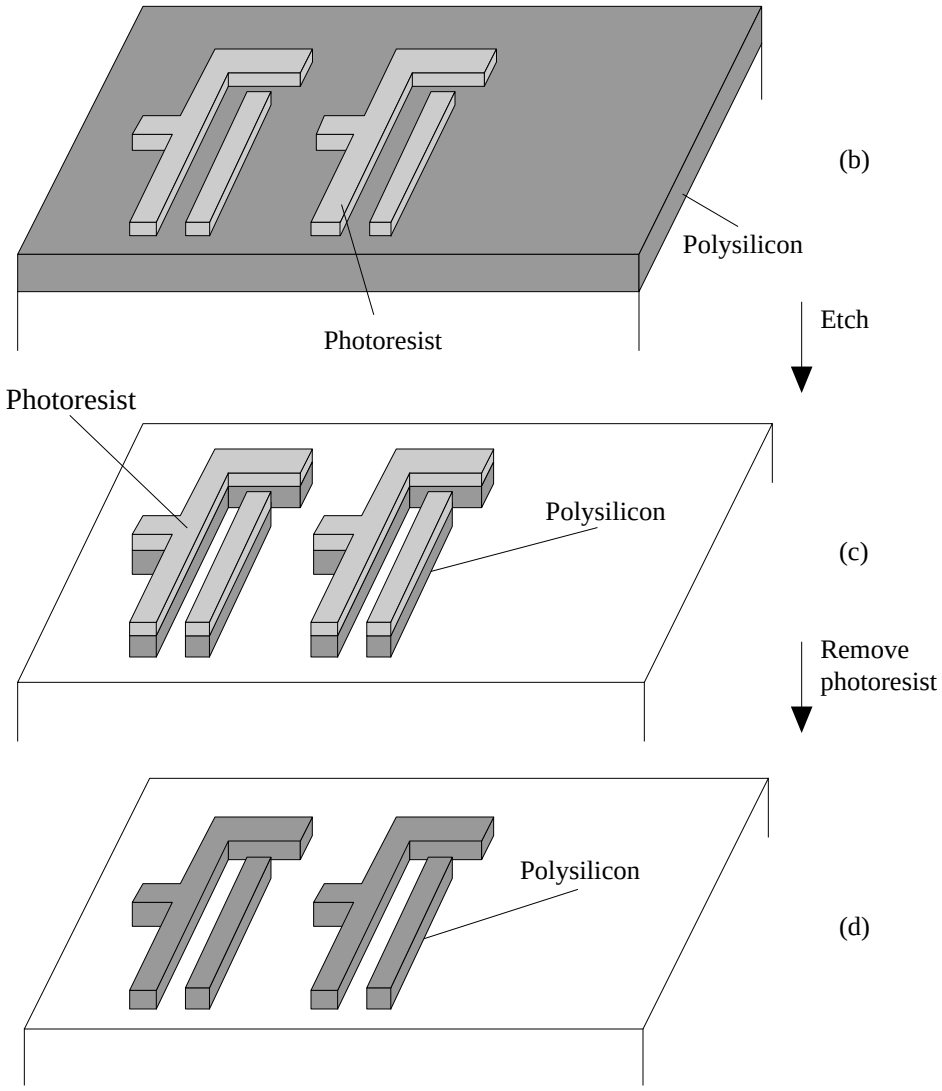


Figure 2.1-4 Basic photolithographic steps to define a polysilicon geometry (cont'd).
(a) Expose (b) Develop (c) Etch (d) Remove photoresist

The process of exposing selective areas of a wafer to light through a photomask is called *printing*. There are three basic types of printing systems used. They are listed below:

- Contact printing
- Proximity printing
- Projection printing

The simplest and most accurate method is *contact printing.* This method uses a glass plate a little larger than the size of the actual wafer with the image of the desired pattern on the side of the glass that comes in physical contact with the wafer. This glass plate is commonly called a *photomask.* The system results in high resolution, high throughput, and low cost. Unfortunately, because of the direct contact, the photomask wears out and

has to be replaced after 10-25 exposures. This method also introduces impurities and defects, because of the physical contact. For these reasons, contact printing is not used in modern VLSI.

A second exposure system is called *proximity printing.* In this system, the photomask and wafer are placed very close to one another but not in intimate contact. As the gap between the photomask and the wafer increases, resolution decreases. In general, this method of patterning is not useful where minimum feature size is below 2 μm. Therefore, proximity printing is not used in present-day VLSI.

The projection printing method separates the wafer from the photomask by a relatively large distance. Lenses or mirrors are used to focus the photomask image on the surface of the wafer. There are two approaches used for projection printing: *scanning*, and *step and repeat*. The scanning method passes light through the photomask which follows a complex optical path reflecting off multiple mirrors imaging the wafer with an arc of illumination optimized for minimum distortion. The photomask and wafer scan the illuminated arc. Minimum feature size for this method is ≈2-3μm.

The projection printing system most used today is step-and-repeat. This method is applied in two ways: reduction, and non-reduction. Reduction projection printing uses a scaled image, typically 5X, on the photomask. One benefit of this method is that defects are reduced by the scale amount. Non-reduction systems do not have this benefit and thus greater burden for low defect densities is placed on the manufacture of the photomask itself.

Electron beam exposure systems are often used to generate the photomasks for projection printing systems because of its high resolution (less than 1 μm). However, the electron beam can be used to directly pattern photoresist without using a photomask. The advantages of using the electron beam as an exposure system are accuracy and the ability to make software changes. The disadvantages are high cost and low throughput.

N-Well CMOS Fabrication Steps

It is important for a circuit designer to understand some of the basic steps involved in fabricating a CMOS circuit. The fabrication steps of one of the more popular CMOS silicon-gate processes will be described in detail. The first step in the n-well silicon-gate CMOS process is to grow a thin silicon-dioxide region on a p^- substrate (wafer). Subsequent to this, the regions where n-wells are to exist are defined in a masking step by depositing a photoresist material on top of the oxide. After exposing and developing the photoresist, n-type impurities are implanted into the wafer as illustrated in Fig. 2.1-5(a). Next, photoresist is removed and a high-temperature oxidation/drive-in step is performed causing the implanted ions to diffuse into the p^- substrate. This is followed by oxide removal and subsequent growth of a thin pad oxide layer. [The purpose of the pad oxide is to protect the substrate from stress due to the difference in the thermal expansion of silicon and silicon nitride.] Then a layer of silicon nitride is deposited over the entire wafer as illustrated in Fig. 2.1-5(b). Photoresist is deposited, patterned, and developed as before, and the silicon nitride is removed from the areas where it has been patterned. The silicon nitride and photoresist remain in the areas where active devices will reside. These regions where silicon nitride remain are called *active area* or *moat.*

Next, a global n-type field (channel stop) implant is performed as illustrated in Fig. 2.1-5(c). The purpose of this is to insure that parasitic p-channel transistors do not turn on under various interconnect lines. Photoresist is removed, re-deposited and patterned using the p-type field (channel stop) implant mask followed by a p^- field-implant step as

shown in Fig. 2.1-5(d). This is to insure that parasitic n-channel transistors do not turn on under various interconnect lines. Next, to achieve isolation between active regions, a thick silicon-dioxide layer is grown over the entire wafer except where silicon nitride exists (silicon nitride impedes oxide growth). This particular way of building isolation between devices is called LOCOS isolation. One of the non-ideal aspects of LOCOS isolation is due to the oxide growth encroaching under the edges of the silicon nitride resulting in a reduced active-area region (the well-known "bird's beak"). Figure 2.1-4(e) shows the results of this step. Once the thick field oxide (FOX) is grown, the remaining silicon nitride is removed and a thin oxide, which will be the gate oxide, is grown followed by a polysilicon deposition step (Fig. 2.1-5(f)). Polysilicon is then patterned and etched, leaving only what is required to make transistor gates and interconnect lines.

At this point, the drain and source areas have not been diffused into the substrate. Modern processes employ lightly-doped drain/source (LDD) diffusions to minimize impact ionization. The LDD structure is built by depositing a spacer oxide over the patterned polysilicon followed by an anisotropic oxide etch leaving spacers on each side of the polysilicon gate as shown in Fig. 2.1-5(g). To make n^+ sources and drains, photoresist is applied and patterned everywhere n-channel transistors are required; n^+ is also required where metal connections are to be made to n^- material such as the n-well. After developing, the n^+ areas are implanted as illustrated in Fig. 2.1-5(h). The photoresist acts as a barrier to the implant as does the polysilicon and spacer. As a result, the n^+ regions that result are properly aligned with the spacer oxide. The spacer is etched next, followed by a lighter n^- implant (Fig. 2.1-5(i)) producing the higher resistivity source/drain regions aligned with the polysilicon gate. These steps are repeated for the p-channel transistors resulting in the cross section illustrated in Fig. 2.1-5(j). Annealing is performed in order to activate the implanted ions. At this point, as shown in Fig. 2.1-5(k), n- and p-channel LDD transistors are complete except for the necessary terminal connections.

In preparation for the contact step, a new, thick oxide layer is deposited over the entire wafer (Fig. 2.1-5(l)). This layer is typically borophosphosilicate glass (BPSG) which has a low reflow temperature (and thus provides a more planar surface for subsequent layers)[22]. Contacts are formed by first defining their location using the photolithographic process applied in previous steps. Next, the oxide areas where contacts are to be made are etched down to the surface of the silicon. The remaining photoresist is removed and metal (aluminum) is deposited on the wafer. First metal (Metal 1) interconnect is then defined photolithographically and subsequently etched so that all unnecessary metal is removed. To prepare for a second metal, another interlayer dielectric is deposited (Fig. 2.1-5(m)). This is usually a sandwich of CVD SiO_2, spun-on glass (SOG), and CVD SiO_2 to achieve planarity. Intermetal connections (via's) are defined through the photolithographic process followed by an etch and the second metal (Metal 2) is then deposited (Fig. 2.1-5(n). A photolithographic step is applied to pattern the second layer metal, followed by a metal etch step.

In order to protect the wafer from chemical intrusion or scratching, a passivation layer of SiO_2 or SiN_3 is applied covering the entire wafer. Pad regions are then defined (areas where wires will be bonded between the integrated circuit and the package containing the circuit) and the passivation layer removed only in these areas. Figure 2.1-5(o) shows a cross section of the final circuit.

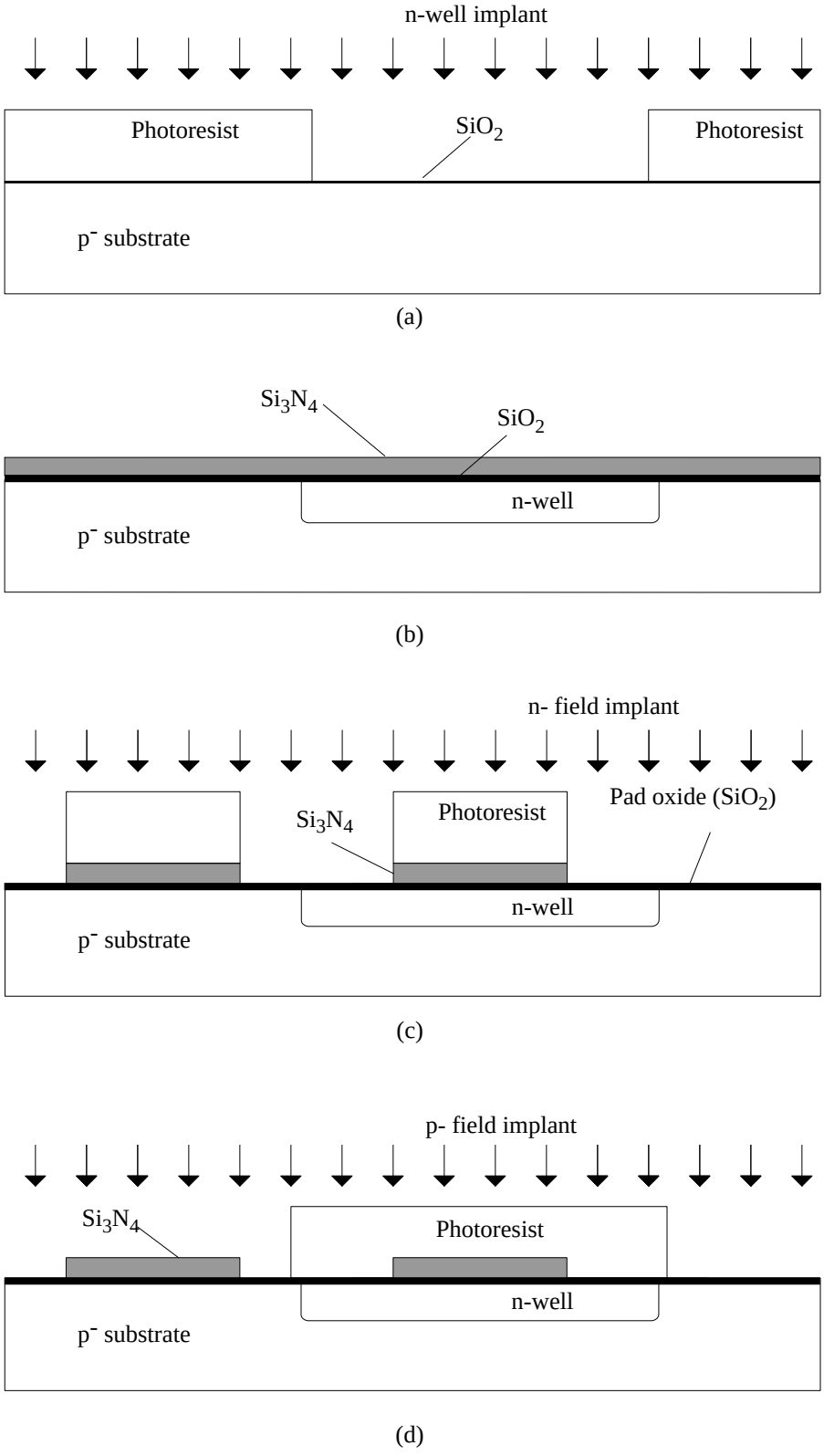
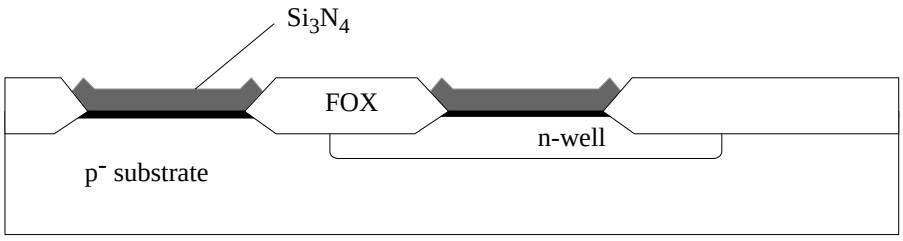
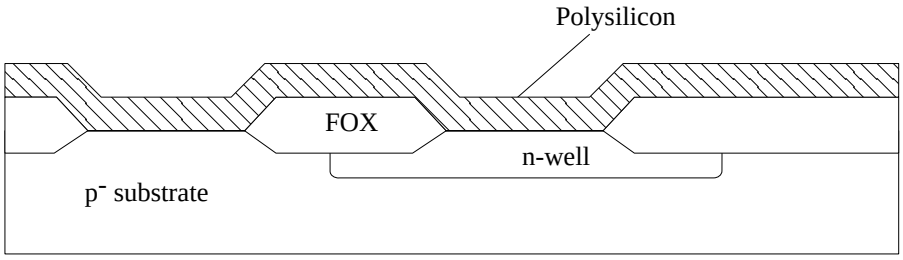


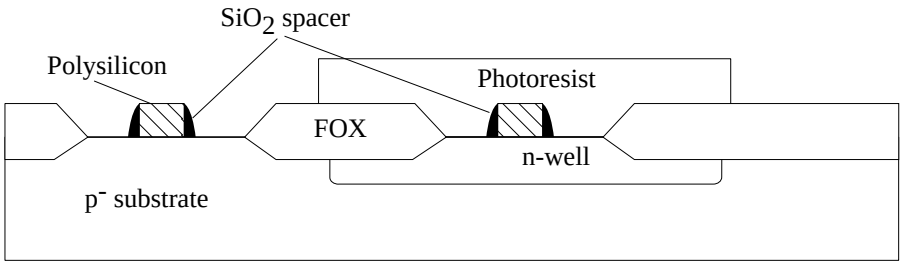
Figure 2.1-5 The major CMOS process steps.



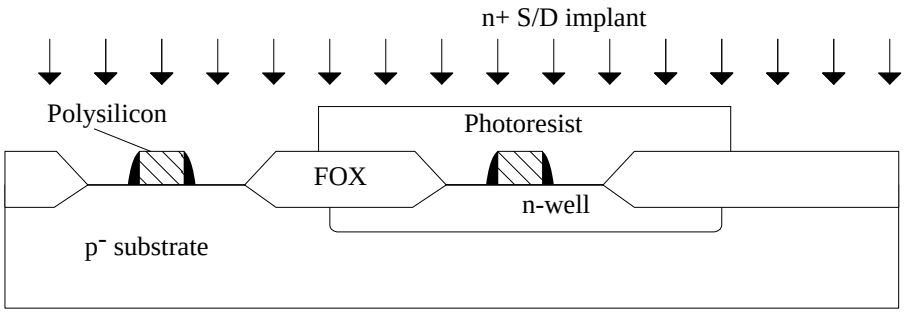
(e)



(f)

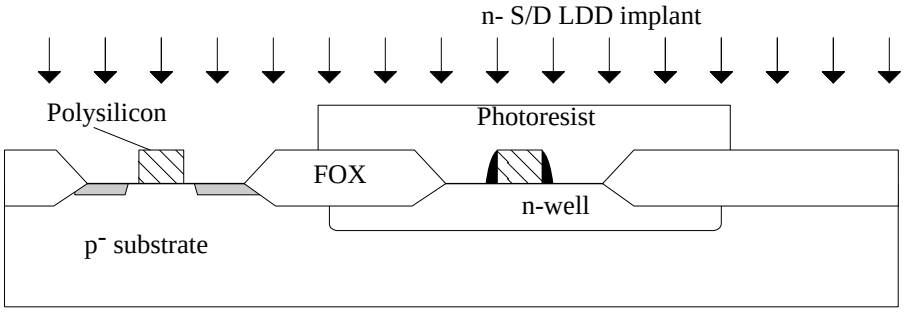


(g)

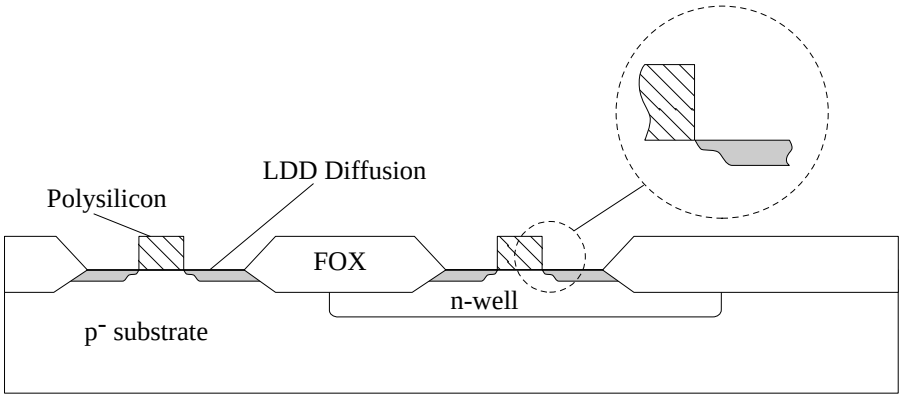


(h)

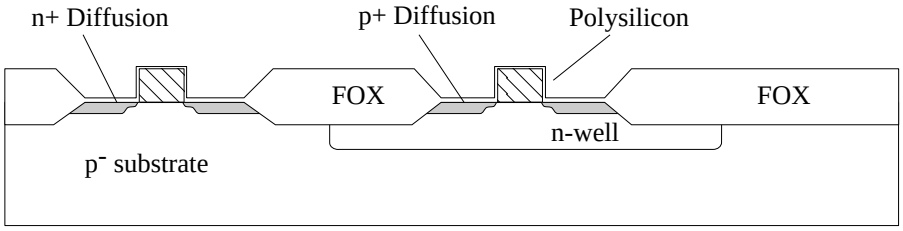
Figure 2.1-5 The major CMOS process steps (cont'd).



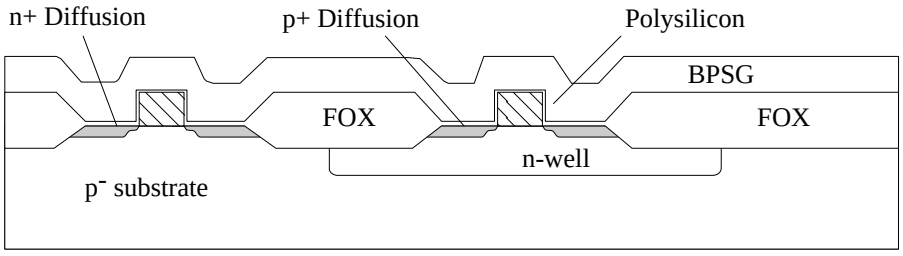
(i)



(j)

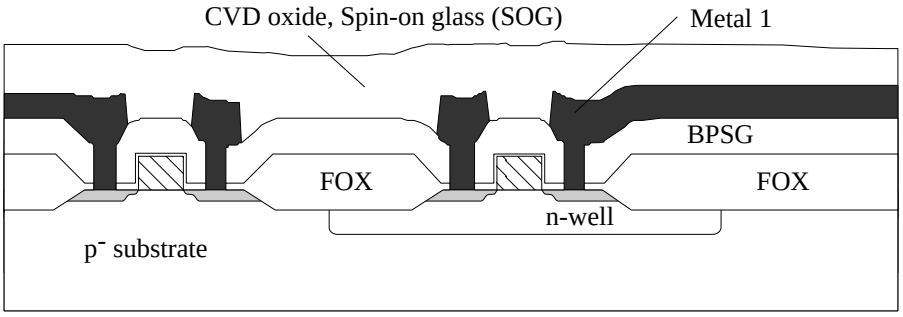


(k)

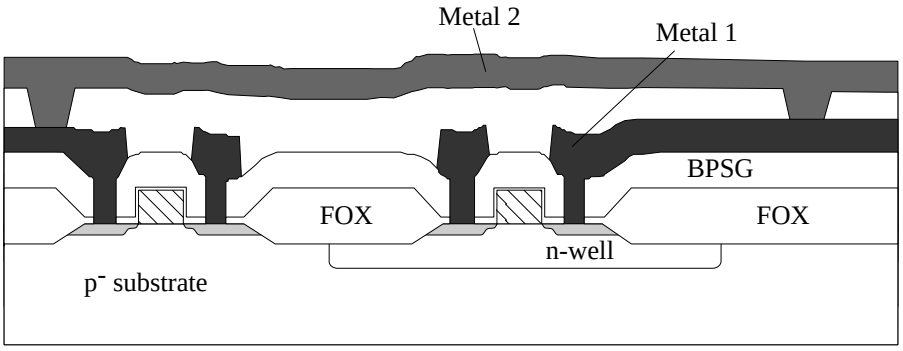


(l)

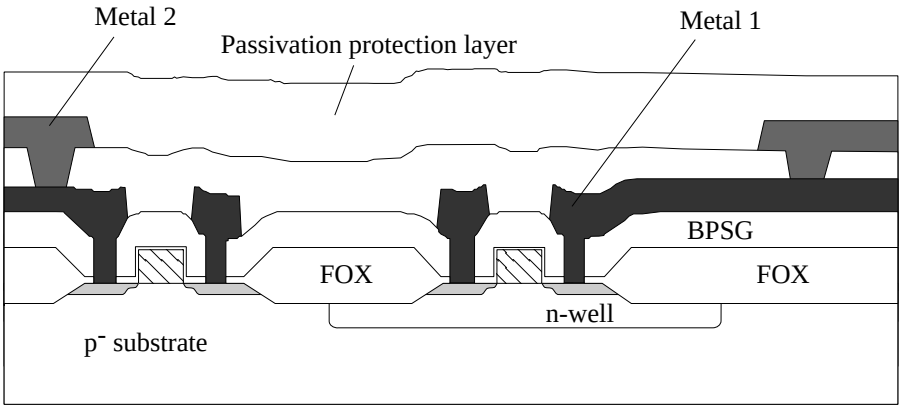
Figure 2.1-5 The major CMOS process steps (cont'd).



(m)



(n)



(o)

Figure 2.1-5 The major CMOS process steps (cont'd).

In order to illustrate the process steps in sufficient detail, actual relative dimensions are not given (i.e., the side-view drawings are not to scale). It is valuable to gain an appreciation of actual scale thus Fig. 2.1-6 is provided below to illustrate relative dimensions.

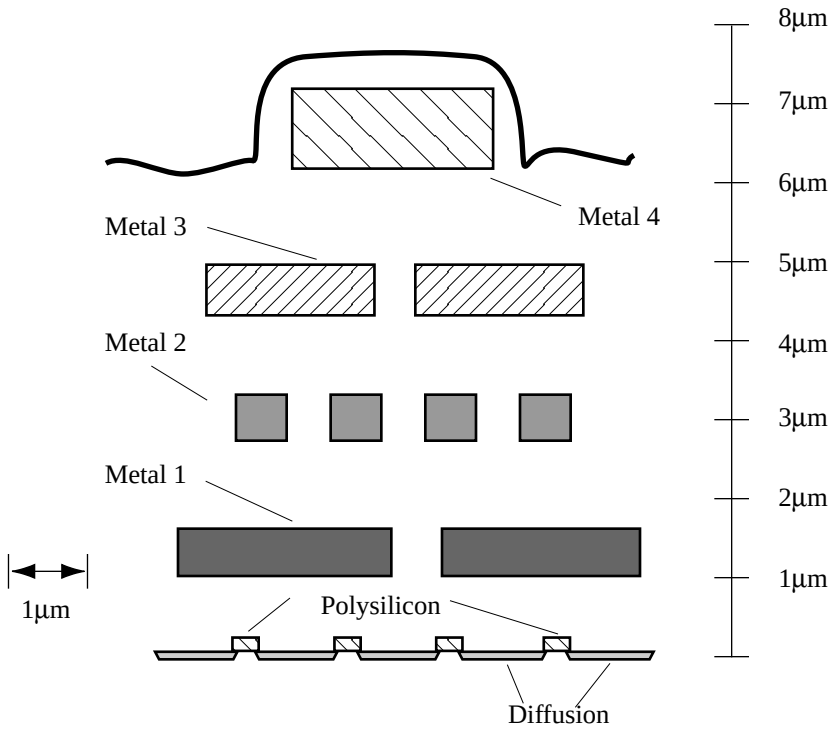


Figure 2.1-6 Side view of CMOS integrated circuit.

Thus far, the basic N-Well CMOS process has been described. There are a variety of enhancements that can be applied to this process to improve circuit performance. These will be covered in the following paragraphs.

Silicide/Salicide Technology

Silicide technology was born out of the need to reduce interconnect resistivity. For with it, a low-resistance silicide such as $TiSi_2$, WSi_2, $TaSi_2$ or several other candidate silicides, is placed on top of polysilcon so that the overall polysilicon resistance is greatly reduced without compromising the other salient benefits of using polysilicon as a transistor gate (well-known work-function and polysilicon-Si interface properties).

Salicide technology (**s**elf-**al**igned sil**icide**)[i] goes one step further by providing low-resistance source/drain connections as well as low-resistance polysilicon. Examples of silicide and salicide transistor cross-sections are illustrated in Fig. 2.1-7[23]. For analog designs, it is important to have available polysilicon and diffusion resistors that are not salicided, so a good mixed-signal process should provide a salicide block.

[i] The terms silicide and salicide are often interchanged. Moreover, *polycide* is used to refer to polysilicon with silicide.

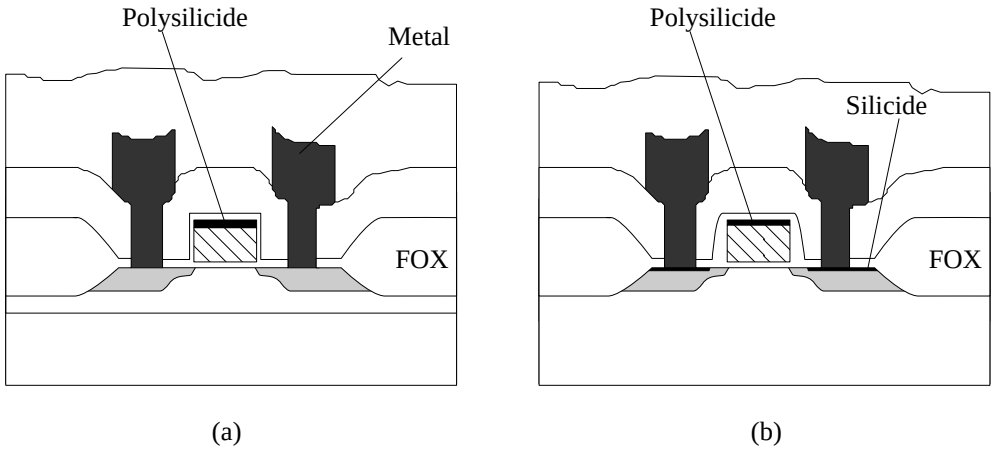


Figure 2.1-7 (a) Polycide structure and (b) Salicide structure.

There are many other details associated with CMOS processes that have not yet been described here. Furthermore, there are different variations on the basic CMOS process just described. Some of these provide multiple levels of polysilicon as well as additional layers of metal interconnect. Others provide good capacitors using either two layers of polysilicon, two layers of metal (MOM capacitors), or polysilicon on top of a heavily implanted (on the same order as a source or drain) diffusion. Still other processes start with a n^- substrate and implant p-wells (rather than n-wells in an p^- substrate). The latest processes also use shallow trench isolation (STI) instead of LOCOS to eliminate the problem of oxide encroachment into the width of a transistor. Newer processes also employ chemical mechanical polishing (CMP) to achieve maximum surface planarity.

2.2 The pn Junction

The pn junction plays an important role in all semiconductor devices. The objective of this section is to develop the concepts of the pn junction that will be useful to us later in our study. These include the depletion-region width, the depletion capacitance, reverse-bias or breakdown voltage, and the diode equation. Further information can be found in the references [24,25].

Fig. 2.2-1(a) shows the physical model of a pn junction. In this model it is assumed that the impurity concentration changes abruptly from N_D donors in the n-type semiconductor to N_A acceptors in the p-type semiconductor. This situation is called a step junction and is illustrated in Fig. 2.2-1(b). The distance x is measured to the right from the metallurgical junction at $x = 0$. When two different types of semiconductor materials are formed in this manner, the free carriers in each type move across the junction by the principle of diffusion. As these free carriers cross the junction, they leave behind fixed atoms which have a charge opposite to the carrier. For example, as the electrons near the junction of the n-type material diffuse across the junction they leave fixed donor atoms of opposite charge (+) near the junction of the n-type material. This is represented in Fig. 2.2-1(c) by the rectangle with a height of qN_D. Similarly, the holes which diffuse across the junction from the p-type material to the n-type material leave behind fixed acceptor atoms that are negatively charged. The electrons and holes that diffuse across the junction quickly recombine with the free majority carriers across the junction. As positive and negative fixed charges are uncovered near the junction by the diffusion of the free carriers, an electric field develops which creates an opposing carrier movement. When

the current due to the free carrier diffusion equals the current caused by the electric field, the pn junction reaches equilibrium. In equilibrium, both v_D and i_D of Fig. 2.2-1(a) are zero.

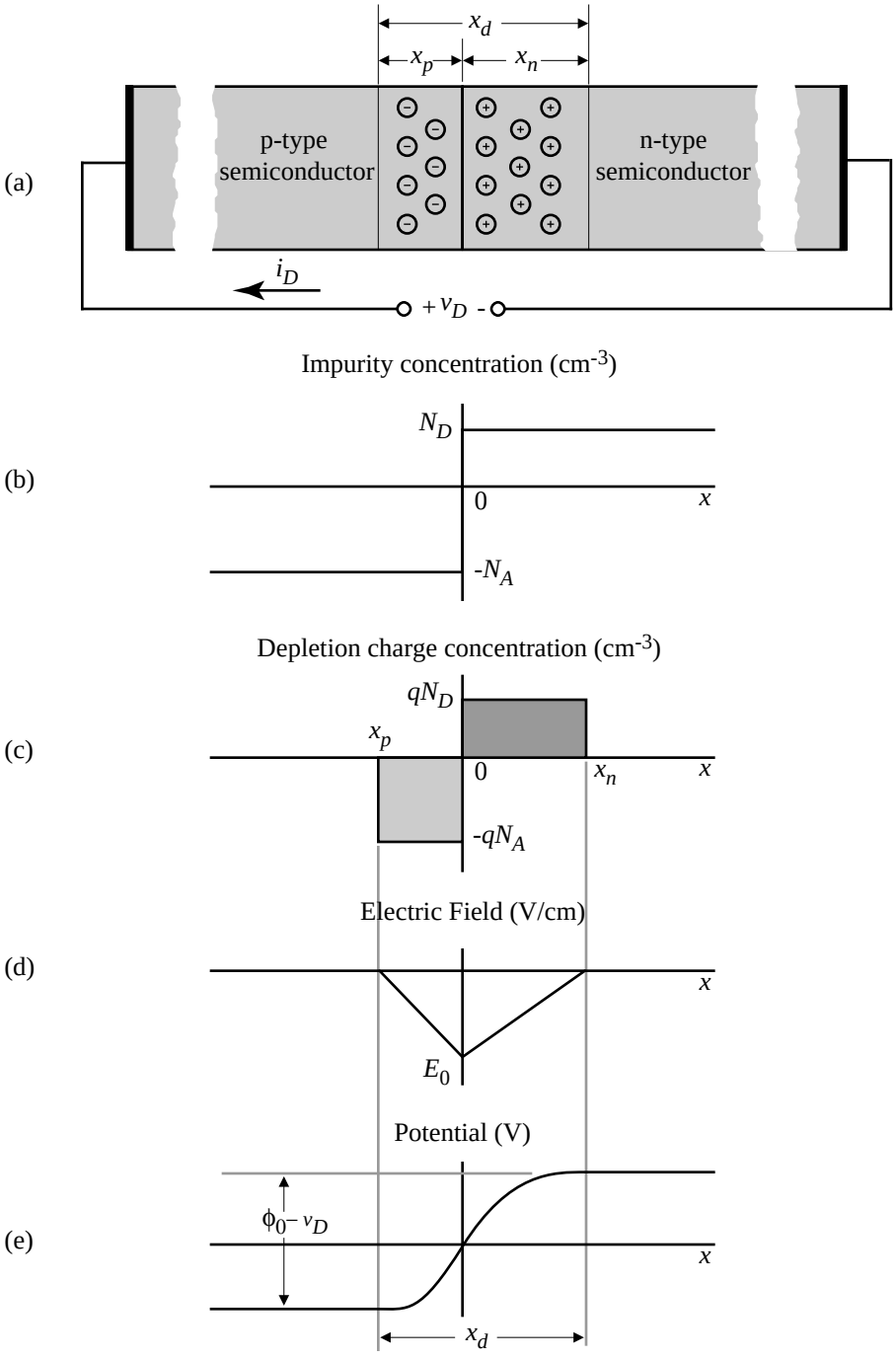


Figure 2.2-1 PN junction (a) Physical structure (b) Impurity concentration. (c) Depletion charge concentration (d) Electric field (e) Electrostatic potential

The distance over which the donor atoms have a positive charge (because they have lost their free electron) is designated as x_n in Fig. 2.2-1(c). Similarly, the distance over

which the acceptor atoms have a negative charge (because they have lost their free hole) is x_p. In this diagram, x_p is a negative number. The *depletion region* is defined as the region about the metallurgical junction which is depleted of free carriers. The depletion region is defined as

$$x_d = x_n - x_p \tag{1}$$

Note that $x_p<0$.

Due to electrical neutrality, the charge on either side of the junction must be equal. Thus,

$$qN_Dx_n = - qN_Ax_p \tag{2}$$

where q is the charge of an electron (1.60×10^{-19} C). The electric field distribution in the depletion region can be calculated using the point form of Gauss's law.

$$\frac{dE(x)}{dx} = \frac{qN}{\varepsilon_{si}} \tag{3}$$

By integrating either side of the junction, the maximum electric field that occurs at the junction, E_o, can be found. This is illustrated in Fig. 2.2-1(d). Therefore, the expression for E_o is

$$E_0 = \int_0^{E_o} dE = \int_{x_p}^{0} \frac{-qN_A}{\varepsilon_{si}} dx = \frac{qN_Ax_p}{\varepsilon_{si}} = \frac{-qN_Dx_n}{\varepsilon_{si}} \tag{4}$$

where ε_{si} is the dielectric constant of silicon and is $11.7\varepsilon_o$ (ε_o is 8.85×10^{-14} F/cm).

The voltage drop across the depletion region is shown in Fig. 2.2-1(e). The voltage is found by integrating the negative electric field resulting in

$$\phi_o - v_D = \frac{-E_o(x_n - x_p)}{2} \tag{5}$$

where v_D is an applied external voltage and ϕ_o is called the *barrier potential* and is given as

$$\phi_o = \frac{kT}{q} \ln\left(\frac{N_AN_D}{n_i^2}\right) = V_t \ln\left(\frac{N_AN_D}{n_i^2}\right) \tag{6}$$

Here, k is Boltzmann's constant (1.38×10^{-23} J/K) and n_i is the intrinsic concentration of silicon which is 1.45×10^{10}/cm^3 at 300 K. At room temperature, the value of V_t is 25.9 mV. It is important to note that the notation for kT/q is V_t rather than the conventional V_T. The reason for this is to avoid confusion with V_T which will be used to designate the threshold voltage of the MOS transistor (see Sec. 2.3). Although the barrier voltage exists with $v_D = 0$, it is not available externally at the terminals of the diode. When metal leads are attached to the ends of the diode a metal-semiconductor junction is formed. The barrier potentials of the metal-semiconductor contacts are exactly equal to ϕ_o so that the open circuit voltage of the diode is zero.

Equations (2), (4), and (5) can be solved simultaneously to find the width of the depletion region in the n-type and p-type semiconductor. These widths are found as

$$x_n = \left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_A}{qN_D(N_A + N_D)}\right]^{1/2} \tag{7}$$

and

$$x_p = -\left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_D}{qN_A(N_A + N_D)}\right]^{1/2} \tag{8}$$

The width of the depletion region, x_d, is found from Eqs. (1), (7) and (8) and is

$$x_d = \left[\frac{2\varepsilon_{si}(N_A + N_D)}{qN_AN_D}\right]^{1/2} (\phi_o - v_D)^{1/2} \tag{9}$$

It can be seen from Eq. (9) that the depletion width for the pn junction of Fig. 2.2-1 is proportional to the square root of the difference between the barrier potential and the externally-applied voltage. It can also be shown that x_d is approximately equal to x_n or x_p for $N_A >> N_D$ or $N_D >> N_A$, respectively. Consequently, the depletion region will extend further into the lightly-doped semiconductor than it will into the heavily-doped semiconductor.

It is also of interest to characterize the depletion charge Q_j which is equal to the magnitude of the fixed charge on either side of the junction. The depletion charge can be expressed from the above relationships as

$$Q_j = |AqN_Ax_p| = AqN_Dx_n = A\left[\frac{2\varepsilon_{si}qN_AN_D}{N_A + N_D}\right]^{1/2} (\phi_o - v_D)^{1/2} \tag{10}$$

where A is the cross-sectional area of the pn junction.

The magnitude of the electric field at the junction E_o can be found from Eqs. (4) and (7) or (8). This quantity is expressed as

$$E_o = \left[\frac{2qN_AN_D}{\varepsilon_{si}(N_A + N_D)}\right]^{1/2} (\phi_o - v_D)^{1/2} \tag{11}$$

Equations (9), (10), and (11) are key relationships in understanding the pn junction.

The depletion region of a pn junction forms a capacitance called the *depletion-layer capacitance.* It results from the dipole formed by uncovered fixed charges near the junction and will vary with the applied voltage. The depletion-layer capacitance C_j can be found from Eq. (10) using the following definition of capacitance.

$$C_j = \frac{dQ_j}{dv_D} = A\left[\frac{\varepsilon_{si}qN_AN_D}{2(N_A + N_D)}\right]^{1/2} \frac{1}{(\phi_o - v_D)^{1/2}} = \frac{C_{j0}}{[1 - (v_D/\phi_o)]^m} \tag{12}$$

C_{j0} is the depletion-layer capacitance when $v_D = 0$ and m is called a grading coefficient. The coefficient m is 1/2 for the case of Fig. 2.2-1 which is called a step junction. If the junction is fabricated using diffusion techniques described in Sec. 2.1, Fig. 2.2-1(b) will become more like the profile of Fig. 2.2-2. It can be shown for this case that m is 1/3. The range of values of the grading coefficient will fall between 1/3 and 1/2.

Fig. 2.2-3 shows a plot of the depletion layer capacitance for a pn junction. It is seen that when v_D is positive and approaches ϕ_o, the depletion-layer capacitance approaches infinity. At this value of voltage, the assumptions made in deriving the above equations are no longer valid. In particular, the assumption that the depletion region is free of charged carriers is not true. Consequently, the actual curve bends over and C_j decreases as v_D approaches ϕ_o [26].

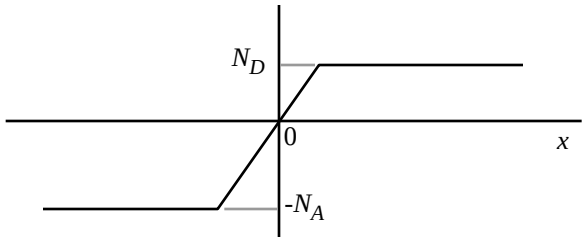


Figure 2.2-2 Impurity concentration profile for diffused pn junction.

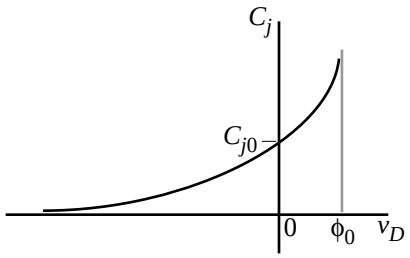


Figure 2.2-3 Depletion capacitance as a function of externally-applied junction voltage.

Example 2.2-1 Characteristics of a pn Junction

Find x_p, x_n, x_d, ϕ_o, C_{j0}, and C_j for an applied voltage of −4 V for a pn diode with a step junction, $N_A = 5 \times 10^{15}/\text{cm}^3$, $N_D = 10^{20}/\text{cm}^3$, and an area of 10 μm by 10 μm.

At room temperature, Eq. (6) gives the barrier potential as 0.917 V. Equations (7) and (8) give $x_n \cong 0$ and $x_p = 1.128$ μm. Thus, the depletion width is approximately x_p or 1.128 μm. Using these values in Eq. (12) we find that C_{j0} is 20.3 fF and at a voltage of – 4 V, C_j is 9.18 fF.

The voltage breakdown of a reverse biased ($v_D < 0$) pn junction is determined by the maximum electric field $E_{\max}$ that can exist across the depletion region. For silicon, this maximum electric field is approximately 3×10^5 V/cm. If we assume that $|v_D| > \phi_o$, then substituting $E_{\max}$ into Eq. (11) allows us to express the maximum reverse-bias voltage or breakdown voltage (BV) as

$$BV \cong \frac{\varepsilon_{si}(N_A + N_D)}{2qN_AN_D} E_{\max}^2 \tag{13}$$

Substituting the values of Example 2.2-1 in Eq. (13) and using a value of 3×10^5 V/cm for $E_{\max}$ gives a breakdown voltage of 58.2 volts. However, as the reverse bias voltage starts to approach this value, the reverse current in the pn junction starts to increase. This increase is due to two conduction mechanisms that can take place in a reverse-biased junction between two heavily-doped semiconductors. The first current mechanism is called avalanche multiplication and is caused by the high electric fields present in the pn junction; the second is called Zener breakdown. Zener breakdown is a direct disruption of valence bonds in high electric fields. However, the Zener mechanism does not require the presence of an energetic ionizing carrier. The current in most breakdown diodes will be a combination of these two current mechanisms.

If i_R is the reverse current in the pn junction and v_R is the reverse-bias voltage across the pn junction, then the actual reverse current i_{RA} can be expressed as

$$i_{RA} = M\, i_R = \left[\frac{1}{1 - (v_R/BV)^n}\right] i_R \tag{14}$$

M is the avalanche multiplication factor and n is an exponent which adjusts the sharpness of the "knee" of the curve shown in Fig. 2.2-4. Typically, n varies between 3 and 6. If both sides of the pn junction are heavily doped, the breakdown will take place by tunneling, leading to the Zener breakdown, which generally occurs at voltages less than 6 volts. Zener diodes can be fabricated where an n^+ diffusion overlaps with a p^+ diffusion. Note that the Zener diode is compatible with the basic CMOS process although one terminal of the Zener must be either on the lowest power supply, V_{SS}, or the highest power supply, V_{DD}.

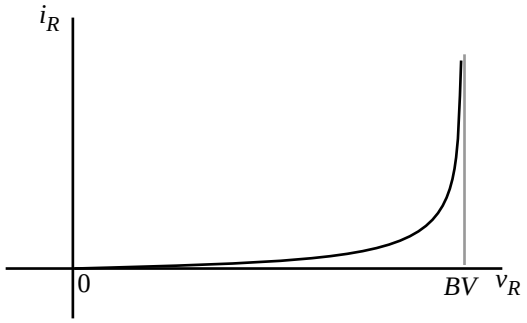


Figure 2.2-4 Reverse-bias volgate-current characteristics of the pn junction illustrating voltage breakdown.

The diode voltage-current relationship can be derived by examining the minority-carrier concentrations in the pn junction. Fig. 2.2-5 shows the minority-carrier concentration for a forward-biased pn junction. The majority-carrier concentrations are much larger and are not shown on this figure. The forward bias causes minority carriers to move across the junction where they recombine with majority carriers on the opposite side. The excess of minority-carrier concentration on each side of the junction is shown by the cross-hatched regions. We note that this excess concentration starts at a maximum value at $x = 0$ ($x' = 0$) and decreases to the equilibrium value as x (x') becomes large. The value of the excess concentration at $x = 0$, designated as $p_n(0)$, or $x' = 0$, designated as $n_p(0)$, is expressed in terms of the forward-bias voltage v_D as

$$p_n(0) = p_{no} \exp\left(\frac{v_D}{V_t}\right) \tag{15}$$

and

$$n_p(0) = n_{po} \exp\left(\frac{v_D}{V_t}\right) \tag{16}$$

where p_{no} and n_{po} are the equilibrium concentrations of the minority carriers in the n-type and p-type semiconductors, respectively. We note that these values are essentially equal to the intrinsic concentration squared divided by the donor or acceptor impurity atom concentration, as shown on Fig. 2.2-5. As v_D is increased, the excess minority concentrations are increased. If v_D is zero, there is no excess minority concentration. If v_D is negative (reverse-biased) the minority-carrier concentration is depleted below its equilibrium value.

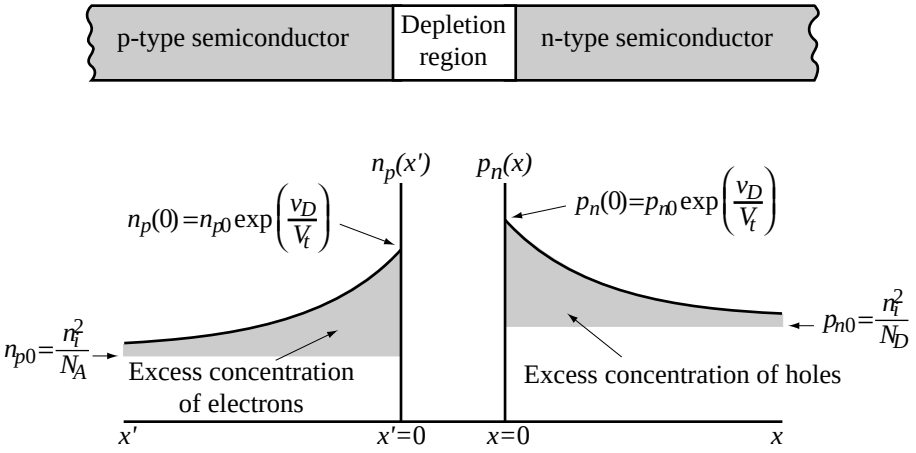


Figure 2.2-5 Impurity concentration profile for diffused pn junction.

The current that flows in the pn junction is proportional to the slope of the excess minority-carrier concentration at $x = 0$ ($x' = 0$). This relationship is given by the diffusion equation expressed below for holes in the n-type material.

$$J_p(x) = -qD_p \left.\frac{dp_n(x)}{dx}\right|_{x=0} \tag{17}$$

where the D_p is the diffusion constant of holes in *n*-type semiconductor. The excess holes in the n-type material can be defined as

$$p'_n(x) = p_n(x) - p_{no} \tag{18}$$

The decrease of excess minority carriers away from the junction is exponential and can be expressed as

$$p'_n(x) = p'_n(0) \exp\left(\frac{-x}{L_p}\right) = [p_n(0) - p_{no}] \exp\left(\frac{-x}{L_p}\right) \tag{19}$$

where L_p is the diffusion length for holes in an n-type semiconductor. Substituting Eq. (15) into Eq. (19) gives

$$p'_n(x) = p_{no}\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right]\exp\left(\frac{-x}{L_p}\right) \tag{20}$$

The current density due to the excess-hole concentration in the n-type semiconductor is found by substituting Eq. (20) in Eq. (17) resulting in

$$J_p(0) = \frac{qD_p p_{no}}{L_p}\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] \tag{21}$$

Similarly, for the excess electrons in the p-type semiconductor we have

$$J_n(0) = \frac{qD_n n_{po}}{L_n}\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] \tag{22}$$

Assuming negligible recombination in the depletion region leads to an expression for the total current density of the pn junction given as

$$J(0) = J_p(0) + J_n(0) = q\left[\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right]\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] \tag{23}$$

Multiplying Eq. (23) by the pn junction area A gives the total current as

$$i_D = qA\left[\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right]\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] = I_s\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] \tag{24}$$

I_S is a constant called the *saturation current.* Equation (24) is the familiar voltage-current relationship that characterizes the pn junction diode.

Example 2.2-2 Calculation of the Saturation Current

Calculate the saturation current of a pn junction diode with $N_A = 5 \times 10^{15}/\text{cm}^3$, $N_D = 10^{20}/\text{cm}^3$, $D_n = 20\ \text{cm}^2/\text{s}$, $D_p = 10\ \text{cm}^2/\text{s}$, $L_n = 10\ \mu\text{m}$, $L_p = 5\ \mu\text{m}$, and $A = 1000\ \mu\text{m}^2$.

From Eq. (24), the saturation current is defined as

$$I_s = qA\left[\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right]$$

p_{no} is calculated from n_i^2/N_D to get $2.103/\text{cm}^3$; n_{po} is calculated from n_i^2/N_A to get $4.205 \times 10^4/\text{cm}^3$. Changing the units of area from μm^2 to cm^2 results in a saturation current magnitude of 1.346×10^{-15} A or 1.346 fA.

This section has developed the depletion-region width, depletion capacitance, breakdown voltage, and the voltage-current characteristics of the pn junction. These concepts will be very important in determining the characteristics and performance of MOS active and passive components.

2.3 The MOS Transistor

The structure of an n-channel and p-channel MOS transistor using an n-well technology is shown in Fig. 2.3-1. The p-channel device is formed with two heavily-doped p^+ regions diffused into a lighter doped n^- material called the well. The two p^+ regions are called drain and source, and are separated by a distance, L (referred to as the

device length). At the surface between the drain and source lies a gate electrode that is separated from the silicon by a thin dielectric material (silicon dioxide). Similarly, the n-channel transistor is formed by two heavily doped n^+ regions within a lightly doped p^- substrate. It, too, has a gate on the surface between the drain and source separated from the silicon by a thin dielectric material (silicon dioxide). Essentially, both types of transistors are four-terminal devices as shown in Fig. 1.2-2(c,d). The *B* terminal is the bulk, or substrate, which contains the drain and source diffusions. For an n-well process, the p-bulk connection is common throughout the integrated circuit and is connected to V_{SS} (the most negative supply). Multiple n-wells can be fabricated on a single circuit, and they can be connected to different potentials in various ways depending upon the application.

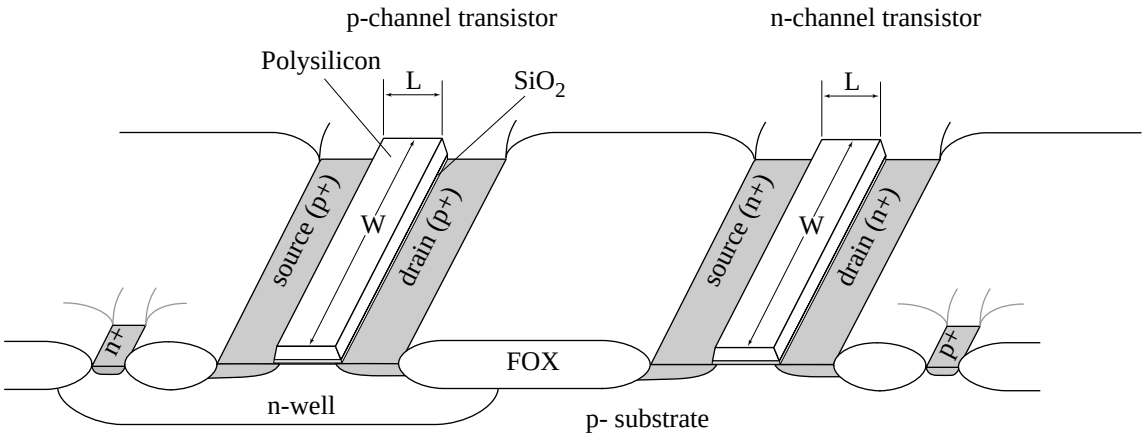


Figure 2.3-1 Physical structure of an n-channel and p-channel transistor in an n-well technology.

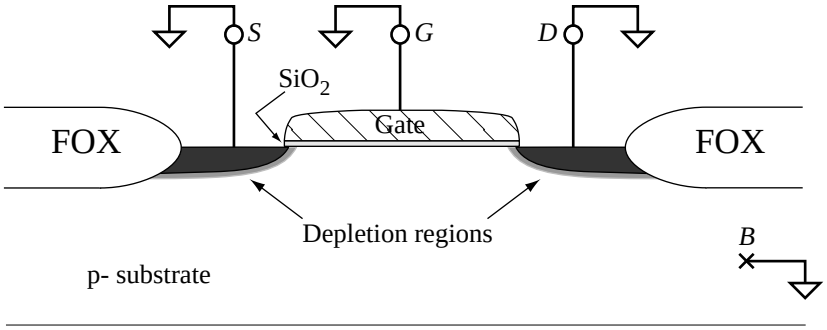


Figure 2.3-2 Cross-section of an n-channel transistor with all terminals grounded.

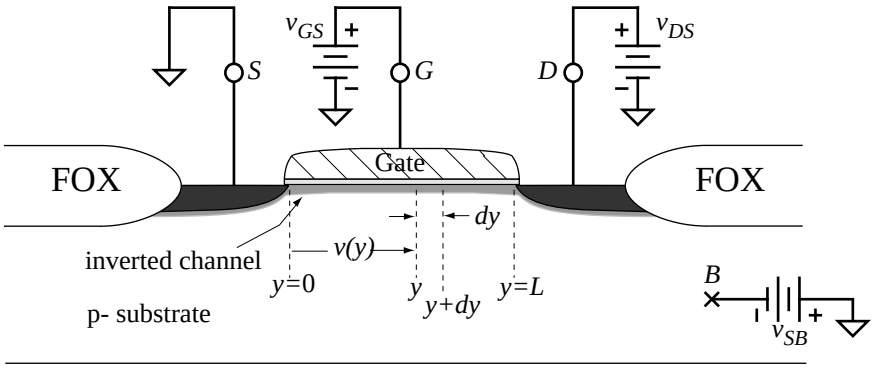


Figure 2.3-3 Cross-section of an n-channel transistor with small v_{DS} and $v_{GS} > V_T$.

Figure 2.3-2 shows an n-channel transistor with all four terminals connected to ground. At equilibrium, the p^- substrate and the n^+ source and drain form a pn junction. Therefore a depletion region exists between the n^+ source and drain and the p^- substrate. Since the source and drain are separated by back-to-back pn junctions, the resistance between the source and drain is very high ($>10^{12}\ \Omega$). The gate and the substrate of the MOS transistor form the parallel plates of a capacitor with the SiO_2 as the dielectric. This capacitance divided by the area of the gate is designated as C_{ox}[i] When a positive potential is applied to the gate with respect to the source a *depletion region* is formed under the gate resulting from holes being pushed away from the silicon-silicon dioxide interface. The depletion region consists of fixed ions which have a negative charge. Using one-dimensional analysis, the charge density, ρ, of the depletion region is given by

$$\rho = q(-N_A) \tag{1}$$

Applying the point form of Gauss's law, the electric field resulting from this charge is

[i] The symbol "C" normally has units of farads, however, in the field of MOS devices it often has units of farads per unit area (e.g., F/m^2).

$$E(x) = \int \frac{\rho}{\varepsilon} dx = \int \frac{-qN_A}{\varepsilon_{si}} dx = \frac{-qN_A}{\varepsilon_{si}} x + C \tag{2}$$

where C is the constant of integration. The constant, C, is determined by evaluating *E(x)* at the edges of the depletion region ($x = 0$ at the Si-SiO_2 interface; $x = x_d$ at the boundary of the depletion region in the bulk).

$$E(0) = E_0 = \frac{-qN_A}{\varepsilon_{si}} 0 + C = C \tag{3}$$

$$E(x_d) = 0 = \frac{-qN_A}{\varepsilon_{si}} x_d + C \tag{4}$$

$$C = \frac{qN_A}{\varepsilon_{si}} x_d \tag{5}$$

This gives an expression for *E(x)*

$$E(x) = \frac{qN_A}{\varepsilon_{si}} (x_d - x) \tag{6}$$

Applying the relationship between potential and electric field yields

$$\int d\phi = -\int E(x)\, dx = -\int \frac{qN_A}{\varepsilon_{si}} (x_d - x)\, dx \tag{7}$$

Integrating both sides of Eq. (7) with appropriate limits of integration gives

$$\int_{\phi_s}^{\phi_F} d\phi = -\int_0^{x_d} \frac{qN_A}{\varepsilon_{si}} (x_d - x)\, dx = -\frac{qN_A x_d^2}{2\varepsilon_{si}} = \phi_F - \phi_s \tag{8}$$

$$\frac{qN_A x_d^2}{2\varepsilon_{si}} = \phi_s - \phi_F \tag{9}$$

where ϕ_F is the equilibrium electrostatic potential (Fermi potential) in the semiconductor, ϕ_S is the surface potential of the semiconductor, and x_d is the thickness of the depletion region. For a p-type semiconductor, ϕ_F is given as

$$\phi_F = -V_t \ln(N_A/n_i) \tag{10}$$

and for an n-type semiconductor ϕ_F is given as

$$\phi_F = V_t \ln(N_D/n_i) \tag{11}$$

Eq. (9) can be solved for x_d assuming that $|\phi_s - \phi_F| \geq 0$ to get

$$x_d = \left[\frac{2\varepsilon_{Si}|\phi_S - \phi_F|}{qN_A}\right]^{1/2} \tag{12}$$

The immobile charge due to acceptor ions that have been stripped of their mobile holes is given by

$$Q = -qN_A x_d \tag{13}$$

Substituting Eq. (12) into Eq. (13) gives

$$Q \cong -qN_A\left[\frac{2\varepsilon_{Si}|\phi_S - \phi_F|}{qN_A}\right]^{1/2} = -\sqrt{2qN_A\varepsilon_{si}|\phi_s - \phi_F|} \tag{14}$$

When the gate voltage reaches a value called the *threshold voltage,* designated as V_T, the substrate underneath the gate becomes inverted, i.e., it changes from a p-type to an n-type semiconductor. Consequently, an n-type channel exists between the source and drain that allows carriers to flow. In order to achieve this inversion, the surface potential must increase from its original negative value ($\phi_s = \phi_F$), to zero ($\phi_s = 0$), and then to a positive value ($\phi_s = -\phi_F$). The value of gate-source voltage necessary to cause this change in surface potential is defined as the *threshold voltage*, V_T. This condition is known as *strong inversion.* The n-channel transistor in this condition is illustrated in Fig. 2.3-3. With the substrate at ground potential, the charge stored in the depletion region between the channel under the gate and the substrate is given by Eq. (14) where ϕ_s has been replaced by $-\phi_F$ to account for the fact that $v_{GS} = V_T$. This charge Q_{b0} is written as

$$Q_{b0} \cong -\sqrt{2qN_A\varepsilon_{si}|-2\phi_F|} \tag{15}$$

If a reverse bias voltage v_{BS} is applied across the pn junction, Eq. (15) becomes

$$Q_b \cong \sqrt{2qN_A\varepsilon_{si}|-2\phi_F + v_{SB}|} \tag{16}$$

An expression for the threshold voltage can be developed by breaking it down into several components. First, the term ϕ_{MS}[i] must be included to represent the difference in the work functions between the gate material and bulk silicon in the channel region. The term ϕ_{MS} is given by

$$\phi_{MS} = \phi_F(\text{substrate}) - \phi_F(\text{gate}) \tag{17}$$

where ϕ_F(metal) = 0.6 V. Second, a gate voltage of $[-2\phi_F - (Q_b/C_{ox})]$ is required to change the surface potential and offset the depletion layer charge Q_b. Lastly, there is always an undesired positive charge Q_{ss} present in the interface between the oxide and the bulk silicon. This charge is due to impurities and imperfections at the interface and must be compensated by a gate voltage of $-Q_{ss}/C_{ox}$. Thus, the threshold voltage for the MOS transistor can be expressed as

[i] Historically, this term has been referred to as the *metal-to-silicon* work function. We will continue the tradition even when the gate terminal is something other than metal (e.g., polysilicon).

$$V_T = \phi_{MS} + \left[-2\phi_F - \frac{Q_b}{C_{ox}}\right] + \left[\frac{-Q_{ss}}{C_{ox}}\right]$$

$$= \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_b - Q_{b0}}{C_{ox}} \tag{18}$$

The threshold voltage can be rewritten as

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|}) \tag{19}$$

where

$$V_{T0} = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} \tag{20}$$

and the body-factor, body-effect coefficient or bulk-threshold parameter γ is defined as

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{ox}} \tag{21}$$

The signs of the above analysis can become very confusing. Table 2.3-1 attempts to clarify any confusion that might arise [25].

Table 2.3-1 Signs for the Quantities in the Threshold Voltage Equation.

Parameter	N-CHANNEL (p-type substrate)	P-CHANNEL (n-type substrate)
ϕ_{MS}		
Metal	–	–
n^+ Si Gate	–	–
p^+ Si Gate	+	+
ϕ_F	–	+
Q_{b0}, Q_b	–	+
Q_{ss}	+	+
V_{SB}	+	–
γ	+	–

Example 2.3-1 Calculation of the Threshold Voltage

Find the threshold voltage and body factor γ for an n-channel transistor with an n^+ silicon gate if $t_{ox} = 200$ Å, $N_A = 3 \times 10^{16}$ cm^{-3}, gate doping, $N_D = 4 \times 10^{19}$ cm^{-3}, and if the positively-charged ions at the oxide-silicon interface per area is 10^{10} cm^{-2}.

From Eq. (10), ϕ_F(substrate) is given as

$$\phi_F(\text{substrate}) = -0.0259 \ln\left[\frac{3\times 10^{16}}{1.45 \times 10^{10}}\right] = -0.377 \text{ V}$$

The equilibrium electrostatic potential for the n^+ polysilicon gate is found from Eq. (11) as

$$\phi_F(\text{gate}) = 0.0259 \ln\left[\frac{4 \times 10^{19}}{1.45 \times 10^{10}}\right] = 0.563 \text{ V}$$

Eq. (17) gives ϕ_{MS} as

$$\phi_F(\text{substrate}) - \phi_F(\text{gate}) = -0.940 \text{ V}.$$

The oxide capacitance is given as

$$C_{ox} = \varepsilon_{ox}/t_{ox} = \frac{3.9 \times 8.854 \times 10^{-14}}{200 \times 10^{-8}} = 1.727 \times 10^{-7} \text{ F/cm}^2$$

The fixed charge in the depletion region, Q_{b0}, is given by Eq. (15) as

$$Q_{b0} = -[2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 2 \times 0.377 \times 3 \times 10^{16}]^{1/2}$$

$$= -8.66 \times 10^{-8} \text{ C/cm}^2.$$

Dividing Q_{b0} by C_{ox} gives –0.501 V. Finally, Q_{ss}/C_{ox} is given as

$$\frac{Q_{ss}}{C_{ox}} = \frac{10^{10} \times 1.60 \times 10^{-19}}{1.727 \times 10^{-7}} = 9.3 \times 10^{-3} \text{ V}$$

Substituting these values in Eq. (18) gives

$$V_{T0} = -0.940 + 0.754 + 0.501 - 9.3 \times 10^{-3} = 0.306 \text{ V}$$

The body factor is found from Eq. (21) as

$$\gamma = \frac{\left[2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 3 \times 10^{16}\right]^{1/2}}{1.727 \times 10^{-7}} = 0.577 \quad \text{V}^{1/2}$$

The above example shows how the value of impurity concentrations can influence the threshold voltage. In fact, the threshold voltage can be set to any value by proper choice of the variables in Eq. (18). Standard practice is to implant the proper type of ions into the substrate in the channel region to adjust the threshold voltage to the desired value. If the opposite impurities are implanted in the channel region of the substrate, the threshold for an n-channel transistor can be made negative. This type of transistor is

called a *depletion transistor* and can have current flow between the drain and source for zero values of the gate-source voltage.

When the channel is formed between the drain and source as illustrated in Fig. 2.3-3, a drain current i_D can flow if a voltage v_{DS} exists across the channel. The dependence of this drain current on the terminal voltages of the MOS transistor can be developed by considering the characteristics of an incremental length of the channel designated as *dy* in Fig. 2.3-3. It is assumed that the width of the MOS transistor (into the page) is *W* and that v_{DS} is small. The charge per unit area in the channel, $Q_I(y)$, can be expressed as

$$Q_I(y) = C_{ox}[v_{GS} - v(y) - V_T] \tag{22}$$

The resistance in the channel per unit of length *dy* can be written as

$$dR = \frac{dy}{\mu_n Q_I(y) W} \tag{23}$$

where μ_n is the average mobility of the electrons in the channel. The voltage drop, referenced to the source, along the channel in the *y* direction is

$$dv(y) = i_D\, dR = \frac{i_D\, dy}{\mu_n Q_I(y) W} \tag{24}$$

or

$$i_D\, dy = W\mu_n Q_I(y)\, dv(y) \tag{25}$$

Integrating along the channel from $y = 0$ to $y = L$ gives

$$\int_0^L i_D\, dy = \int_0^{v_{DS}} W\mu_n Q_I(y)\; dv(y) = \int_0^{v_{DS}} W\mu_n C_{ox}[v_{GS} - v(y) - V_T]\, dv(y) \tag{26}$$

Performing the integration results in the desired expression for i_D as

$$i_D = \frac{\mu_n C_{ox} W}{L}\left[(v_{GS} - V_T)v(y) - \frac{v(y)^2}{2}\right]_0^{v_{DS}} = \frac{\mu_n C_{ox} W}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right] \tag{27}$$

This equation is sometimes called the Sah equation [27] and has been used by Shichman and Hodges [28] as a model for computer simulation. Eq. (27) is only valid when

$$v_{GS} \geq V_T \;\text{ and }\; v_{DS} \leq (v_{GS} - V_T) \tag{28}$$

The factor $\mu_n C_{ox}$ is often defined as the device-transconductance parameter, given as

$$K' = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} \tag{29}$$

Eq. (28) will be examined in more detail in the next chapter, concerning the modeling of MOS transistors. The operation of the p-channel transistor is essentially the same as that of the n-channel transistor, except that all voltage and current polarities are reversed.

2.4 Passive Components

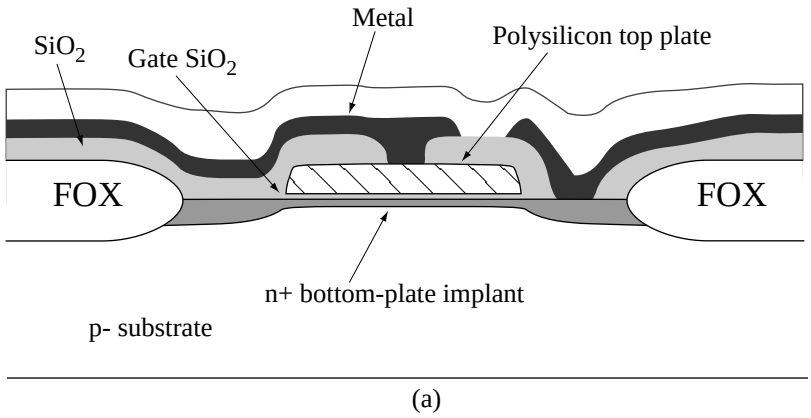
This section examines the passive components that are compatible with fabrication steps used to build the MOS device. These passive components include the capacitor and the resistor.

Capacitors

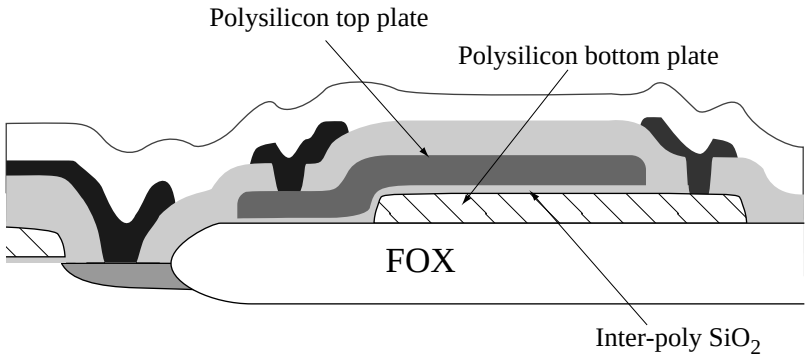
A good capacitor is often required when designing analog integrated circuits. They are used as compensation capacitors in amplifier designs, as bandwidth-determining components in gm/C filters, as charge storage devices in switched-capacitor filters and digital-to-analog converters, and other places as well. The desired characteristics for capacitors used in these applications are given below:

- Good matching accuracy
- Low voltage-coefficient
- High ratio of desired capacitance to parasitic capacitance
- High capacitance per unit area

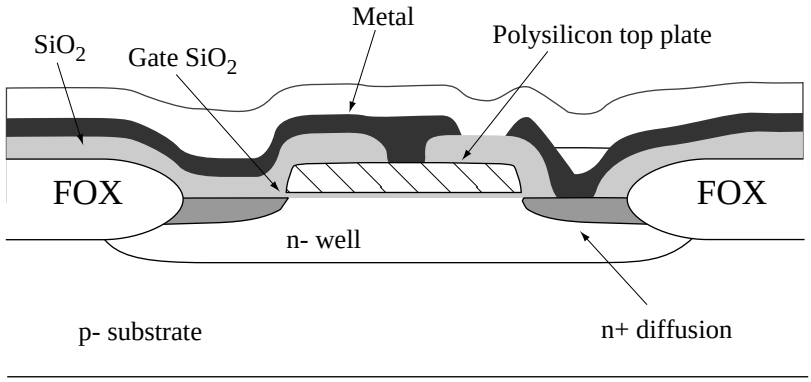
Analog CMOS processes differentiate themselves from purely digital ones by providing capacitors that meet the above criteria. For such analog processes, there are basically two types of capacitors made available. One type of capacitor is formed using one of the available interconnect layers (metal or polysilicon) on top of crystalline silicon separated by a dielectric (silicon dioxide layer). Figure 2.4-1(a) shows an example of this capacitor using polysilicon as the top conducting plate. In order to achieve a low voltage-coefficient capacitor, the bottom plate must be heavily-doped diffusion (similar to that of the source and drain). As the process was described in Sec. 2.3, such heavily-doped diffusion is normally not available underneath polysilicon because the source/drain implant step occurs after polysilicon is deposited and defined. To solve this problem, an extra implant step must be included prior to deposition of the polysilicon layer. The mask-defined implanted region becomes the bottom plate of the capacitor. The capacitance achieved using this technique is inversely proportional to gate oxide thickness. Typical values for a 0.8 μm process are given in Table 2.4-1. This capacitor achieves a high capacitance per unit area and good matching performance, but has a significant voltage dependent parasitic capacitance to the substrate.



(a)



(b)



(c)

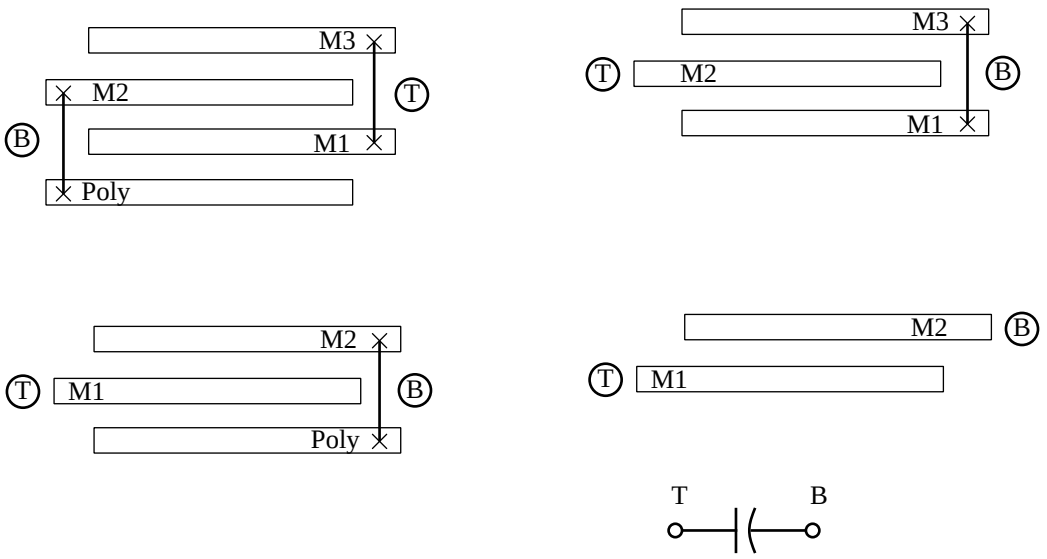
Figure 2.4-1 MOS capacitors. (a) Polysilicon-oxide-channel. (b) Polysilicon-oxide-polysilicon (c) Accumulation MOS capacitor.

The second type of capacitor available in analog-taylored processes is that formed by providing an additional polysilicon layer on top of gate polysilicon (separated by a dielectric). An example of a double polysilicon capacitor is illustrated in Fig. 2.4-1(b). The dielectric is formed by a thin silicon-dioxide layer which can only be produced by

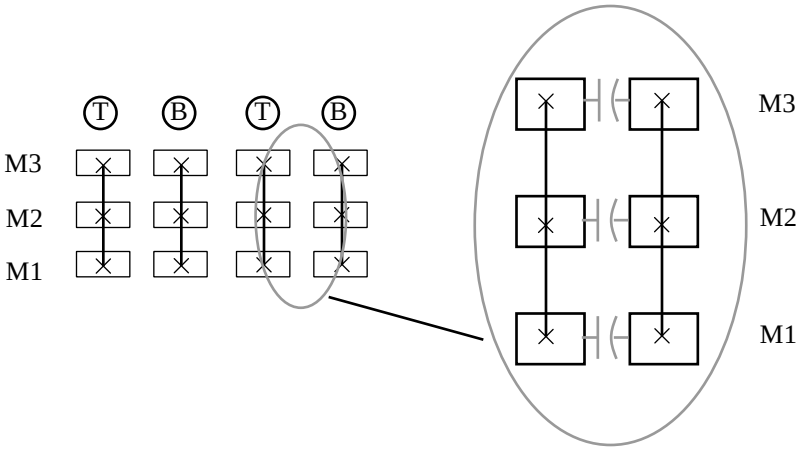
using several steps beyond the usual single polysilicon process. This capacitor does an excellent job of meeting the criteria set forth above. In fact, it is the best of all possible choices for high-performance capacitors. Typical values for a 0.8μm process are given in Table 2.4-1.

A third type of capacitor is illustrated in Fig. 2.4-1(c). This capacitor is constructed by putting an n-well underneath an n-channel transistor. It is similar to the capacitor in Fig2.4-1(a) except that its bottom plate (the n-well) has a much higher resistivity. Because of this fact, it is not used in circuits where a low voltage coefficient is important. It is, however, often used when one terminal of the capacitor is connected to ground (or VSS). It offers a very high capacitance per unit area, it can be matched well, and is available in all CMOS processes because no unique steps or masks are required.

Quite often, the processing performance required by the digital component of a mixed-signal integrated circuit, necessitates the use of a process targeted for digital applications. Such processes do not provide taylored capacitors for analog applications. Therefore, when a capacitor is needed, it must be derived from two or more of the interconnect layers. Figure 2.4-2 illustrates symbolically various schemes for making capacitors in one-, two-, and three-layer metal digital processes. In Fig. 2.4-2(a) capacitors are constructed vertically using the interlayer oxide as the capacitor dielectric. The four-layer example achieves the highest ratio of desired capacitance to parasitic capacitance whereas the two-layer capacitor achieves the lowest. As processes migrate toward finer line widths and higher speed performance, the oxide between metals increases while the allowed space between metals decreases. For such processes, same-layer, horizontal, capacitors can be more efficient than different-layer vertical capacitors. This is due to the fact that the allowed space between two M1 lines, for example, is less than the vertical space between M1 and M2 (see Fig. 2.1-6). An example of a same-layer horizontal capacitor is illustrated in Fig. 2.4-2(b). Compared to polysilicon-oxide-polysilcon capacitors, these capacitors typically suffer from lower per-unit-area capacitance and lower ratio of desired capacitance to parasitic capacitance. Matching accuracy of capacitors implemented like those in Fig 2.4-2 is on the order of 1-2% and voltage coefficient is low. Typical values for vertical capacitors in a 0.8μm process are given in Table 2.4-1.



(a)



(b)

Figure 2.4-2 Various ways to implement capacitors using available interconnect layers illustrated with a side view. M1, M2, and M3 represent the first, second, and third metal layers respectively. (a) Vertical parallel plate structures. (b) Horizontal parallel plate structures.

The voltage coefficient of integrated capacitors generally falls within the range of 0 to −200 ppm/V depending upon the structure of the capacitor and, if applicable, the doping concentration of the capacitor plates [32]. The temperature coefficient of integrated capacitors is found to be in the range of 20 to 50 ppm/°C. When considering the ratio of two capacitors on the same substrate, note that the variations on the absolute value of the capacitor due to temperature tend to cancel. Therefore temperature variations have little effect on the matching accuracy of capacitors. When capacitors are switched to different voltages, as in the case of sampled-data circuits, the voltage coefficient can have a deleterious effect if it is not kept to a minimum.

The parasitic capacitors associated with the capacitors of Fig's. 2.4-1 and 2.4-2 can give rise to a significant source of error in analog sampled-data circuits. The capacitor plate with the smallest parasitic associated with it is referred to as the *top plate*. It is not necessarily physically the top plate although quite often it is. In contrast, the *bottom plate* is that plate having the larger parasitic capacitance associated with it. Schematically, the top plate is represented by the flat plate in the capacitor symbol while the curved plate represents the bottom plate. For the capacitors illustrated in Fig. 2.4-1 the parasitic capacitor associated with the top plate of the capacitor itself is due primarily to interconnect lines leading to the capacitor and the bottom-plate parasitic capacitance is primarily due to the capacitance between the bottom plate and the substrate. The capacitors available in a digital process shown in Fig. 2.4-2 have parasitics that are not so easily generalized. The parasitics are very dependent upon the layout of the device (layout is discussed in Sec. 2.6).

Figure 2.4-3 shows a general capacitor with its top and bottom plate parasitics. These parasitic capacitances depend on the capacitor size, layout, and technology, and are unavoidable.

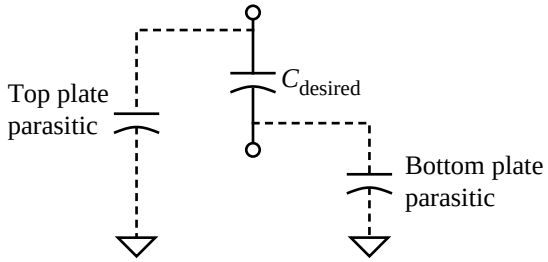


Figure 2.4-3 A model for the integrated capacitors showing top and bottom plate parasitics.

Resistors

The other passive component compatible with MOS technology is the resistor. Even though we shall use circuits consisting of primarily MOS active devices and capacitors, some applications, such as digital-to-analog conversion, use the resistor. Resistors compatible with the MOS technology of this section include diffused, polysilicon, and n-well (or p-well) resistors. Though not as common, metal can be used as a resistor as well.

A diffused resistor is formed using source/drain diffusion and is shown in Fig. 2.4-4(a). The sheet resistance of such resistors in a non-salicided process is usually in the range of 50 to 150 Ω/❑ (Ohms per square as explained in Sec 2.6). For a salicide process, these resistors are in the range of 5 to 15 Ω/❑. The fact that the source/drain diffusion is needed as a conductor in integrated circuits conflicts with its use as a resistor. Clearly the goal of a salicide process is to achieve "conductor-like" performance from source/drain diffusion. In these processes, a *salicide block* can be used to mask the silicide film thus allowing for a high-resistance source/drain diffusion where desired. The diffused resistor is found to have a voltage coefficient of resistance in the 100 to 500 ppm/V range. The parasitic capacitance to ground is also voltage dependent in this type of resistor.

A polysilicon resistor is shown in Fig. 2.4-4(b). This resistor is surrounded by thick oxide and has a sheet resistance in the range of 30 to 200 Ω/❑ depending upon doping levels. For a polysilicide process, the effective resistance of the polysilicon is about 10 Ω/❑.

An n-well resistor shown in Fig. 2.4-4(c) is made up of a strip of n-well contacted at both ends with n^+ source/drain diffusion. This type of resistor has a resistance of 1 to 10 kΩ/❑ and a high value for its voltage coefficient. In cases where accuracy is not required, such as pull-up resistors, or protection resistors, this structure is very useful.

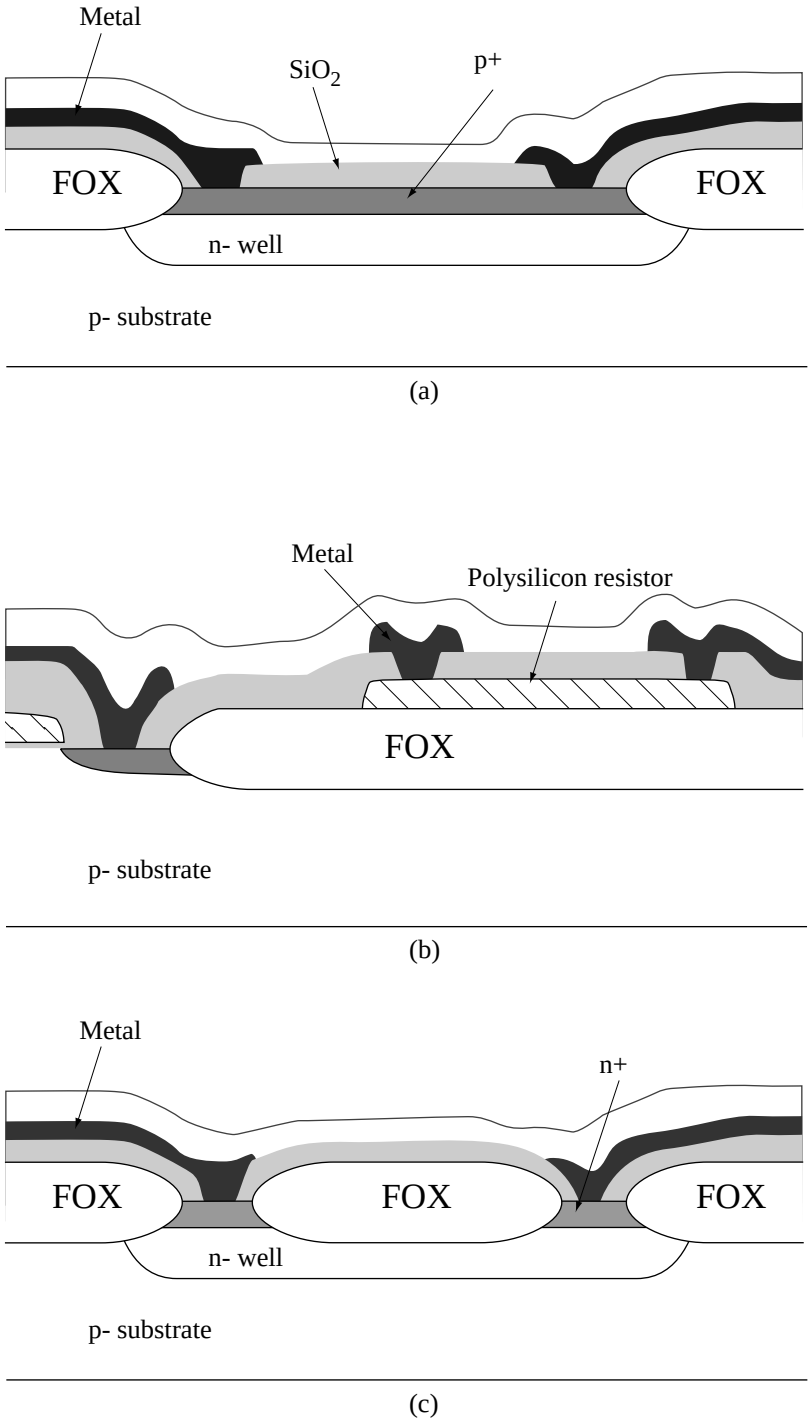


Figure 2.4-4 Resistors. (a) Diffused (b) Polysilicon (c) N-well

Other types of resistors are possible if the process is altered. The three categories above represent those most commonly applied with standard MOS technology. Table 2.4-1 summarizes the characteristics of the passive components hitherto discussed.

Table 2.4-1 Approximate Performance Summary of Passive Components in a 0.8μm CMOS Process

Component Type	Range of Values	Matching Accuracy	Temperature Coefficient	Voltage Coefficient
Poly/poly capacitor	0.8-1.0 fF/μm^2	0.05%	50 ppm/°C	50ppm/V
MOS capacitor	2.2-2.7 fF/μm^2	0.05%	50 ppm/°C	50ppm/V
M1-Poly capacitor	0.021-0.025 fF/μm^2	1.5%		
M2-M1 capacitor	0.021-0.025 fF/μm^2	1.5%		
M3-M2 capacitor	0.021-0.025 fF/μm^2	1.5%		
P+ Diffused resistor	80-150 Ω/❑	0.4%	1500 ppm/°C	200ppm/V
N+ Diffused resistor	50-80 Ω/❑	0.4%	1500 ppm/°C	200ppm/V
Poly resistor	20-40 Ω/❑	0.4%	1500 ppm/°C	100ppm/V
N-well resistor	1-2 kΩ/❑		8000 ppm/°C	10k ppm/V

2.5 Other Considerations of CMOS Technology

In the previous two sections, the active and passive components of the basic CMOS process have been presented. In this section we wish to consider some other components that are also available from the basic CMOS process but that are not used as extensively as the previous components. We will further consider some of the limitations of CMOS technology, including latch-up, temperature, and noise. This information will become useful later, when the performance of CMOS circuits is characterized.

So far we have seen that it is possible to make resistors, capacitors, and pn diodes that are compatible with the basic single-well CMOS fabrication process illustrated in Fig. 2.3-1. It is also possible to implement a bipolar junction transistor (BJT) that is compatible with this process, even though the collector terminal is constrained to V_{DD} (or V_{SS}). Figure 2.5-1 shows how the BJT is implemented for a n-well process. The emitter is the source or drain diffusion of an p-channel device, the base is the n-well (with a base width of W_B) and the p^- substrate is the collector. Because the pn junction between the n-well and the p^- substrate must be reverse biased, the collector must always be connected to the most negative power-supply voltage, V_{SS}. The BJT will still find many useful applications even though the collector is constrained. The BJT illustrated in Fig. 2.5-1 is often called a *substrate BJT*. The substrate BJT functions like the BJT fabricated in a process designed for BJTs. The only difference is that the collector is constrained and the base width is not well controlled, resulting in a wide variation of current gains.

Fig. 2.5-2 shows the minority-carrier concentrations in the BJT. Normally, the base-emitter (*BE*) pn junction is forward biased and the collector-base (*CB*) pn junction is reverse biased. The forward-biased *EB* junction causes free electrons to be injected into the base region. If the base width W_B is small, most of these electrons reach the *CB* junction and are swept into the collector by the reverse-bias voltage. If the minority-carrier concentrations are much less than the majority-carrier concentrations, then the

collector current can be found by solving for the current in the base region. In terms of current densities, the collector current density is

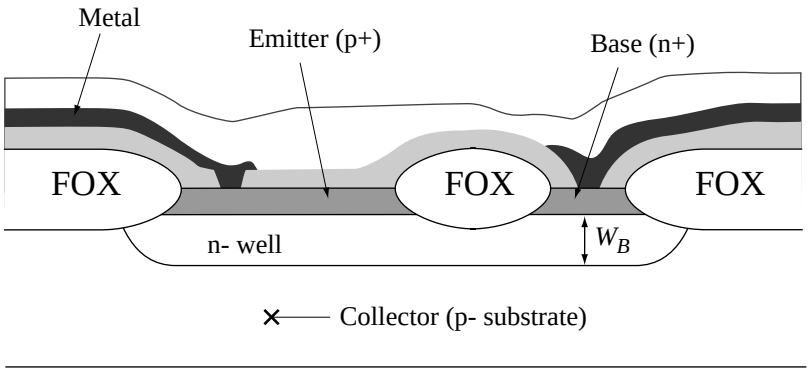


Figure 2.5-1 Substrate BJT available from a bulk CMOS process.

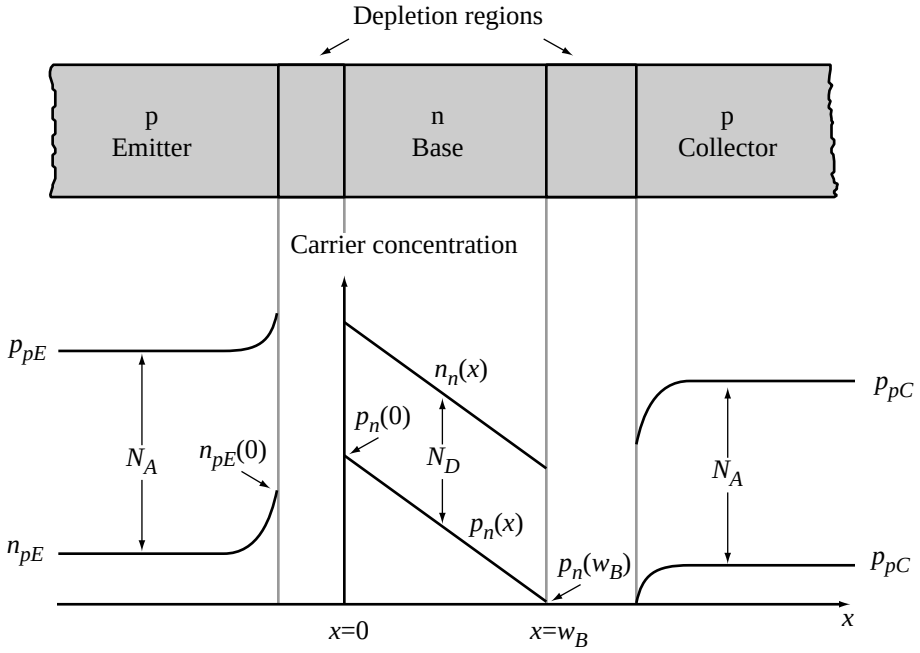


Figure 2.5-2 Minority carrier concentrations for a bipolar junction transistor.

$$J_C = -J_n\Big|_{\text{base}} = -qD_n\frac{dn_p(x)}{dx} = qD_n\frac{n_p(0)}{W_B} \tag{1}$$

From Eq. (16) of Sec. 2.2 we can write

$$n_p(0) = n_{po}\exp\left(\frac{v_{BE}}{V_t}\right) \tag{2}$$

Combining Eqs. (1) and (2) and multiplying by the area of the *BE* junction *A* gives the collector current as

$$i_C = AJ_C = \frac{qAD_n n_{po}}{W_B} \exp\left(\frac{v_{BE}}{V_t}\right) = I_s \exp\left(\frac{v_{BE}}{V_t}\right) \tag{3}$$

where I_s is defined as

$$I_s = \frac{qAD_n n_{po}}{W_B} \tag{4}$$

As the holes travel through the base, a small fraction will recombine with electrons which are the majority carriers in the base. As this occurs, an equal number of electrons must enter the base from the external base circuit in order to maintain electrical neutrality in the base region. Also, there will be injection of the electrons from the base to the emitter due to the forward-biased *BE* junction. This injection is much smaller than the hole injection from the emitter because the emitter is more heavily doped than the base. The injection of electrons into the emitter and the recombination of electrons with holes in the base both constitute the external base current i_B that flows into the base. The ratio of collector current to base current, i_C/i_B is defined as β_F or the common-emitter current gain. Thus, the base current is expressed as

$$i_B = \frac{i_C}{\beta_F} = \frac{I_S}{\beta_F} \exp\left(\frac{v_{BE}}{V_t}\right) \tag{5}$$

The emitter current can be found from the base current and the collector current because the sum of all three currents must equal zero. Although β_F has been assumed constant it varies with i_C, having a maximum for moderate currents and falling off from this value for large or small currents.

In addition to the substrate BJT, it is also possible to have a lateral BJT. Figure 2.3-1 can be used to show how the lateral BJT can be implemented. The emitter could be the n+ source of the n-channel device, the base the p^- substrate, and the collector the n^- well. Although the base is constrained to the substrate potential of the chip, the emitter and collector can have arbitrary voltages. Unfortunately the lateral BJT is not very useful because of the large base width. In fact the lateral BJT is considered more as a parasitic transistor. However, this lateral BJT becomes important in the problem of latch-up of CMOS circuits which is discussed next [33].

Latch-up in integrated circuits may be defined as a high current state accompanied by a collapsing or low-voltage condition. Upon application of a radiation transient or certain electrical excitations, the latched or high current state can be triggered. Latch-up can be initiated by at least three regenerative mechanisms. They are: (1) the four-layer, silicon-controlled-rectifier (SCR), regenerative switching action; (2) secondary breakdown; and (3) sustaining voltage breakdown. Because of the multiple p and n diffusions present in CMOS, they are susceptible to SCR latch-up.

Fig. 2.5-3(a) shows a cross-section of Fig. 2.3-1 and how the PNPN SCR is formed. The schematic equivalent of Fig. 2.5-3(a) is given in Fig. 2.5-3(b). Here the SCR action is clearly illustrated. The resistor R_{N-} is the n-well resistance from the base of the vertical *PNP* (Q2) to V_{DD}. The resistor R_{P-} is the substrate resistance from the base of the lateral *NPN* (Q2) to V_{SS}.

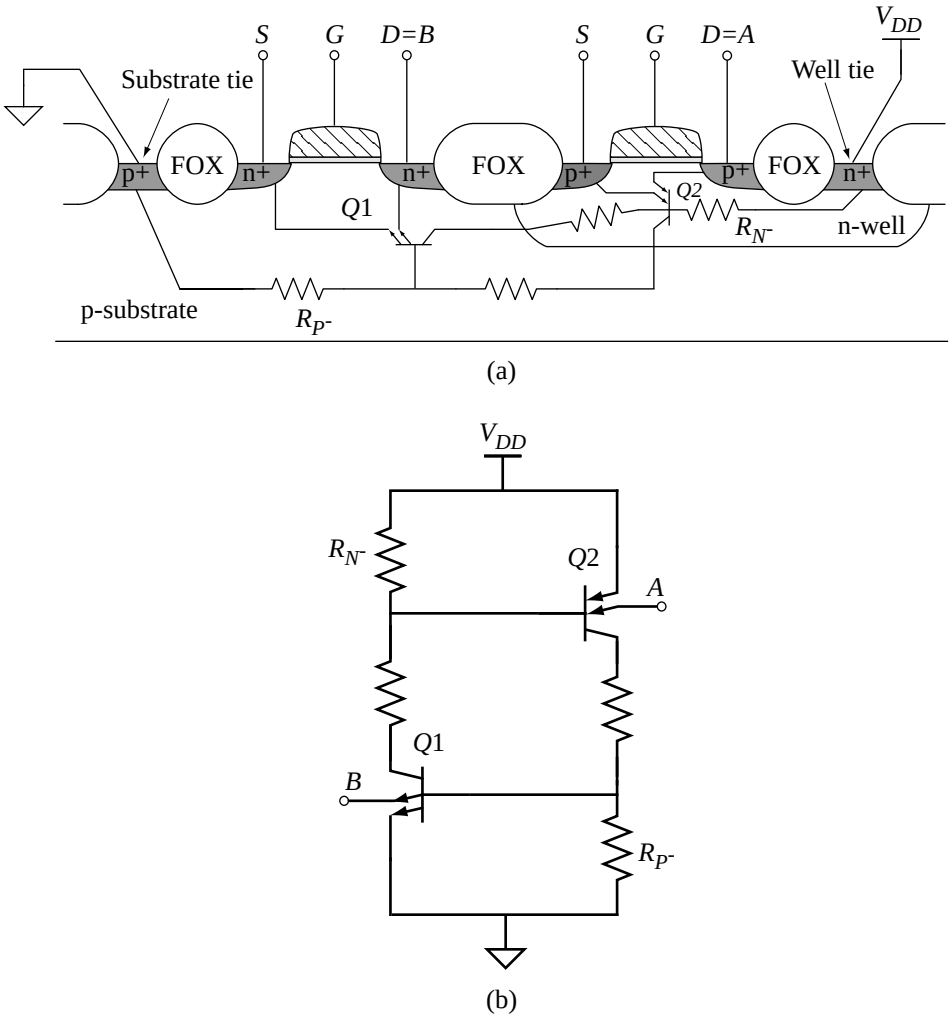


Figure 2.5-3 (a) Parasitic lateral NPN and vertical PNP bipolar transistor in CMOS integrated circuits. (b) Equivalent circuit of the SCR formed from the parasitic bipolar transistors.

Regeneration occurs when three conditions are satisfied. The first condition is that the loop gain must exceed unity. This condition is stated as

$$\beta_{NPN}\beta_{PNP} \geq 1 \tag{6}$$

where β_{NPN} and β_{PNP} are the common-emitter, current-gain ratios of Q2 and Q1, respectively. The second condition is that both of the base-emitter junctions must become forward biased. The third condition is that the circuits connected to the emitter must be capable of sinking and sourcing a current greater than the holding current of the *PNPN* device.

To prevent latch-up, several standard precautions are taken. One approach is to keep the source/drain of the n-channel device as far away from the n-well as possible. This reduces the value of β_{NPN} and helps to prevent latch-up. Unfortunately, this is very costly in terms of area. A second approach is to reduce the values of R_{N^-} and R_{P^-}. Smaller resistor values are helpful because more current must flow through them in order to forward bias the base-emitter regions of Q1 and Q2. These resistances can be reduced by

surrounding the p-channel devices with a n^+ guard ring connected to V_{DD} and by surrounding n-channel transistors with p^+ guard rings tied to V_{SS} as shown in Fig. 2.5-4.

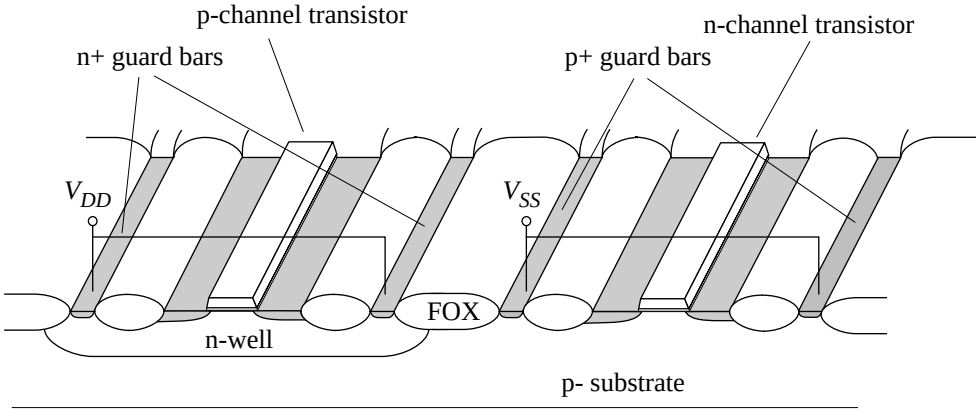


Figure 2.5-4 Preventing latch-up using guard bars in an n-well technology

Latch-up can also be prevented by keeping the potential of the source/drain of the p-channel device [A in Fig. 2.5-3 (b)] from being higher than V_{DD} or the potential of the source/drain of the n-channel device [B in Fig. 2.5-3 (b)] from going below V_{SS}. By careful design and layout, latch-up can be avoided in most cases. In the design of various circuits, particularly those that have high currents, one must use care to avoid circuit conditions that will initiate latch-up.

Another important consideration of CMOS technology is the electrostatic discharge protection of the gates of transistors which are externally accessible. To prevent accidental destruction of the gate oxide, a resistance and two reverse-biased pn junction diodes are employed to form an input protection circuit. One of the diodes is connected with the n side to the highest circuit potential (V_{DD}) and the p side to the gate to be protected. The other diode is connected with the n side to the gate to be protected and the p side to the lowest circuit potential (V_{SS}). This is illustrated in Fig. 2.5-5. For an n-well process, the first diode is usually made by a p^+ diffusion into the n^- well. The second diode is made by a n^+ diffusion into the substrate. The resistor is connected between the external contact and the junction between the diodes and the gate to be protected. If a large voltage is applied to the input, one of the diodes will breakdown depending upon the polarity of the voltage. If the resistor is large enough, it will limit the breakdown current so that the diode is not destroyed. This circuit should be used whenever the gates of a transistor (or transistors) are taken to external circuits.

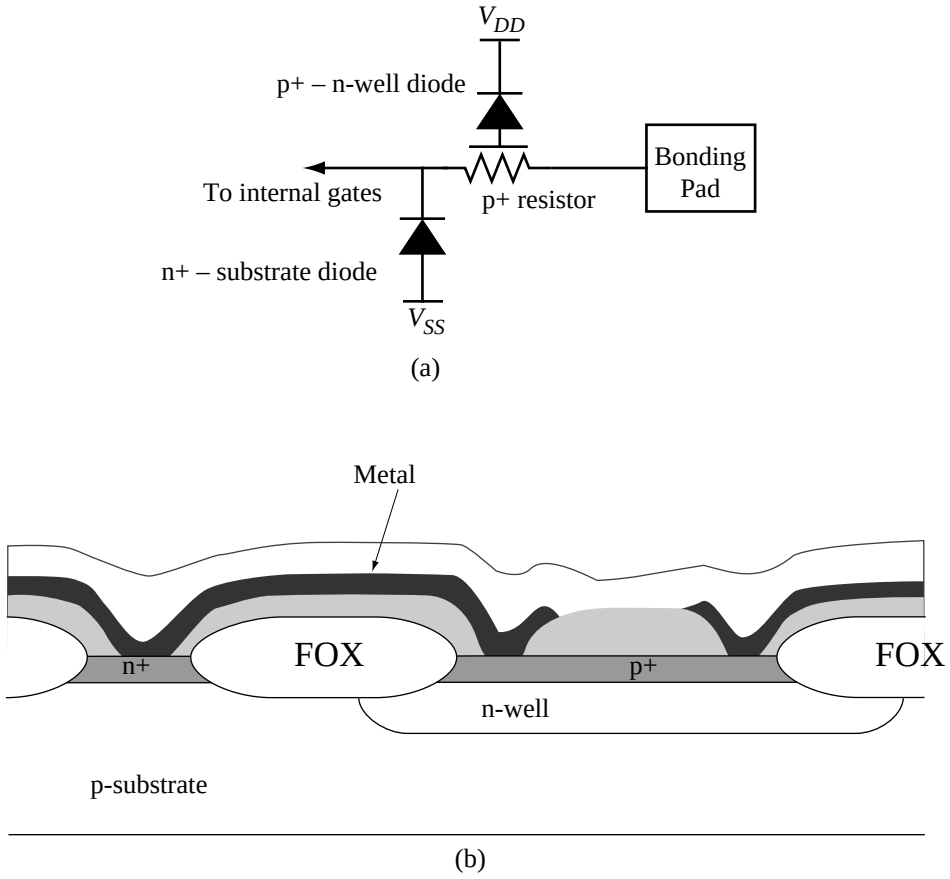


Figure 2.5-5 Electrostatic discharge protection circuitry. (a) Electrical equivalent circuit (b) Implementation in CMOS technology

The temperature dependence of MOS components is an important performance characteristic in analog circuit design. The temperature behavior of passive components is usually expressed in terms of a *fractional temperature coefficient* TC_F defined as

$$TC_F = \frac{1}{X} \cdot \frac{dX}{dT} \tag{7}$$

where X can be the resistance or capacitance of the passive component. Generally, the fractional temperature coefficient is multiplied by 10^6 and expressed in units of parts per million per °C or ppm/°C. The fractional temperature coefficient of various CMOS passive components has been given in Table 2.4-1.

The temperature dependence of the MOS device can be found from the expression for drain current given in Eq. (28) of Sec. 2.3. The primary temperature-dependent parameters are the mobility μ and the threshold voltage V_T. The temperature dependence of the carrier mobility μ is given as [34],

$$\mu = K_\mu T^{-1.5} \tag{8}$$

The temperature dependence of the threshold voltage can be approximated by the following expression [35]

$$V_T(\mathrm{T}) = V_T(\mathrm{T}_0) - \alpha(T - T_0) \tag{9}$$

where α is approximately 2.3 mV/°C. This expression is valid over the range of 200 to 400 K, with α depending on the substrate doping level and the dosages of the implants used during fabrication. These expressions for the temperature dependence of mobility and threshold voltage will be used later to determine the temperature performance of MOS circuits and are valid only for limited ranges of temperature variation about room temperature. Other modifications are necessary for extreme temperature ranges.

The temperature dependence of the pn junction is also important in this study. For example, the pn-junction diode can be used to create a reference voltage whose temperature stability will depend upon the temperature characteristics of the pn-junction diode. We shall consider the reverse-biased pn-junction diode first. Eq. (24) of Sec. 2.2 shows that when $v_D < 0$, that the diode current is given as

$$-i_D \cong I_s = qA\left[\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right] \cong \frac{qAD}{L}\frac{n_i^2}{N} = KT^3 \exp\left(\frac{-V_{Go}}{V_t}\right) \tag{10}$$

where it has been assumed that one of the terms in the brackets is dominant and that L and N correspond to the diffusion length and impurity concentration of the dominant term. Also T is the absolute temperature in Kelvin and V_{Go} is the bandgap voltage of silicon at 300 K (1.205 V). Differentiating Eq. (10) with respect to T results in

$$\frac{dI_S}{dT} = \frac{3KT^3}{T}\exp\left(\frac{-V_{Go}}{V_t}\right) + \frac{qKT^3 V_{Go}}{KT^2}\exp\left(\frac{-V_{Go}}{V_t}\right) = \frac{3I_S}{T} + \frac{I_S}{T}\frac{V_{Go}}{V_t} \tag{11}$$

The TC_F for the reverse diode current can be expressed as

$$\frac{1}{I_S}\frac{dI_S}{dT} = \frac{3}{T} + \frac{1}{T}\frac{V_{Go}}{V_t} \tag{12}$$

The reverse diode current is seen to double approximately every 5 °C increase as illustrated in the following example.

Example 2.5-1 Calculation of the Reverse Diode Current Temperature Dependence and TC_F

Assume that the temperature is 300 K (room temperature) and calculate the reverse diode current change and the TC_F for a 5 K increase.

The TC_F can be calculated from Eq. (12) as

$$TC_F = 0.01 + 0.155 = 0.165$$

Since the TC_F is change per degree, the reverse current will increase by a factor of 1.165 for every degree K (or °C) change in temperature. Multiplying by 1.165 five times gives an increase of approximately 2. This implies that the reverse saturation current will approximately double for every 5 °C temperature increase. Experimentally, the reverse current doubles for every 8 °C increase in temperature because the reverse current is in part leakage current.

The forward biased pn-junction diode current is given by

$$i_D \cong I_s \exp\left(\frac{v_D}{V_t}\right) \tag{13}$$

Differentiating this expression with respect to temperature and assuming that the diode voltage is a constant ($v_D = V_D$) gives

$$\frac{di_D}{dT} = \frac{i_D}{I_s} \cdot \frac{dI_s}{dT} - \frac{1}{T} \cdot \frac{V_D}{V_t} i_D \tag{14}$$

The fractional temperature coefficient for i_D results from Eq. (14) as

$$\frac{1}{i_D} \cdot \frac{di_D}{dT} = \frac{1}{I_s} \cdot \frac{dI_s}{dT} - \frac{V_D}{TV_t} = \frac{3}{T} + \left[\frac{V_{Go} - V_D}{TV_t}\right] \tag{15}$$

If V_D is assumed to be 0.6 volts, then the fractional temperature coefficient is equal to 0.01 + (0.155 – 0.077) = 0.0879. It can be seen that the forward diode current will double for approximately a 10°C increase in temperature.

The above analysis for the forward-bias pn-junction diode assumed that the diode voltage v_D was held constant. If the forward current is held constant ($i_D = I_D$), then the fractional temperature coefficient of the forward diode voltage can be found. From Eq. (13) we can solve for v_D to get

$$v_D = V_t \ln\left(\frac{I_D}{I_s}\right) \tag{16}$$

Differentiating Eq. (16) with respect to temperature gives

$$\frac{dv_D}{dT} = \frac{v_D}{T} - V_t\left(\frac{1}{I_s} \cdot \frac{dI_s}{dT}\right) = \frac{v_D}{T} - \frac{3V_t}{T} - \frac{V_{Go}}{T} = -\left[\frac{V_{Go} - v_D}{T}\right] - \frac{3V_t}{T} \tag{17}$$

Assuming that $v_D = V_D = 0.6$ V the temperature dependence of the forward diode voltage at room temperature is approximately –2.3 mV/°C.

Another limitation of CMOS components is noise. Noise is a phenomenon caused by small fluctuations of the analog signal within the components themselves. Noise results from the fact that electrical charge is not continuous but the result of quantized behavior and is associated with the fundamental processes in a semiconductor component. In essence, noise acts like a random variable and is often treated as one. Our objective is to introduce the basic concepts concerning noise in CMOS components. More detail can be found in several excellent references [24,36].

Several sources of noise are important in CMOS components. *Shot noise* is associated with the dc current flow across a pn junction. It typically has the form of

$$\overline{i}^2 = 2qI_D \Delta f \quad (Amperes^2) \tag{18}$$

where $\overline{i}^2$ is the mean-square value of the noise current, q is the charge of an electron, I_D is the average dc current of the pn junction, and Δf is the bandwidth in hertz. Noise-current spectral density can be found by dividing $\overline{i}^2$ by Δf. The noise-current spectral density is denoted as $\overline{i}^2/\Delta f$.

Another source of noise, called *thermal noise*, is due to random thermal motion of the electron and is independent of the dc current flowing in the component. It generally has the form of

$$\overline{v}^2 = 4kTR\,\Delta f \tag{19}$$

where k is Boltzmann's constant and R is the resistor or equivalent resistor in which the thermal noise is occurring.

An important source of noise for MOS components is the *flicker noise* or the 1/f *noise*. This noise is associated with carrier traps in semiconductors which capture and release carriers in a random manner. The time constants associated with this process give rise to a noise signal with energy concentrated at low frequency. The typical form of the $1/f$ noise is given as

$$\overline{i}^2 = K_f\left[\frac{I^a}{f^b}\right]\Delta f \tag{20}$$

where K_f is a constant, a is a constant (0.5 to 2), and b is a constant ($\cong$1). The current-noise spectral density for typical $1/f$ noise is shown in Fig. 2.5-6. Other sources of noise exist, such as burst noise and avalanche noise, but are not important in CMOS components and are not discussed here.

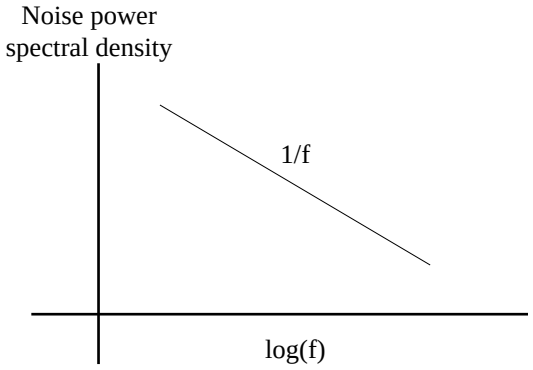


Figure 2.5-6 1/f noise spectrum.

2.6 Integrated Circuit Layout

The final subject in this chapter concerns the geometrical issues involved in the design of integrated circuits. A unique aspect of integrated-circuit design is that it requires understanding of the circuit beyond the schematic. A circuit defined and functioning properly at the schematic level can fail if it is not correctly designed physically. Physical design, in the context of integrated circuits, is referred to as *layout.*

As a designer works through the process of designing a circuit, he must consider all implications that the physical layout might have on a circuit's operation. Effects due to matching of components or parasitic components must be kept in mind. If, for example, two transistors are intended to exhibit identical performance, their layout must be identical. A wide-bandwidth amplifier design will not function properly if parasitic

capacitances at critical nodes are not minimized through careful layout. To appreciate these finer issues dealing with physical design, it is important to first develop a basic understanding of integrated-circuit layout and the rules that govern it.

As described in Sec. 2.1, an integrated circuit is made up of multiple layers, each defined by a photomask using a photolithographic process. Each photomask is built from a computer database which describes it geometrically. This database is derived from the physical layout drawn by a mask designer or by computer (at present, most analog layout is still performed manually). The layout consists of topological descriptions of all electrical components that will ultimately be fabricated on the integrated circuit. The most common components which have been discussed thus far are transistors, resistors, and capacitors.

Matching Concepts

As will be seen in later chapters, matching performance of two or more components is very important to overall circuit operation. Since matching is dependent upon layout topology, it is appropriate to discuss it here.

The rule for making two components electrically equivalent is simply to draw them as identical units. This is the *unit-matching* principle. To say that two components are identical means that both they and their surroundings must be identical. This concept can be explained in non-electrical terms.

Consider the two square components, A and B, illustrated in Fig. 2.6-1(a). In this example, these objects could be pieces of metal that are desired after deposition and etching. They have identical shape in area and perimeter as drawn. However, the surroundings seen by A and B are different due to the presence of object C. The presence of object C nearer to object B may cause that object to change in some way different than A. The solution to this is somehow force the surroundings of both geometries A and B to be the same. This can never be achieved perfectly! However, matching performance can normally be improved by at least making the immediate surroundings identical as illustrated in Fig. 2.6-1(b). This general principle will be applied repeatedly to components of various types. When it is desired to match components of different size, optimal matching is achieved when both geometries are made from integer numbers of units with all units being designed applying the unit-matching principle.

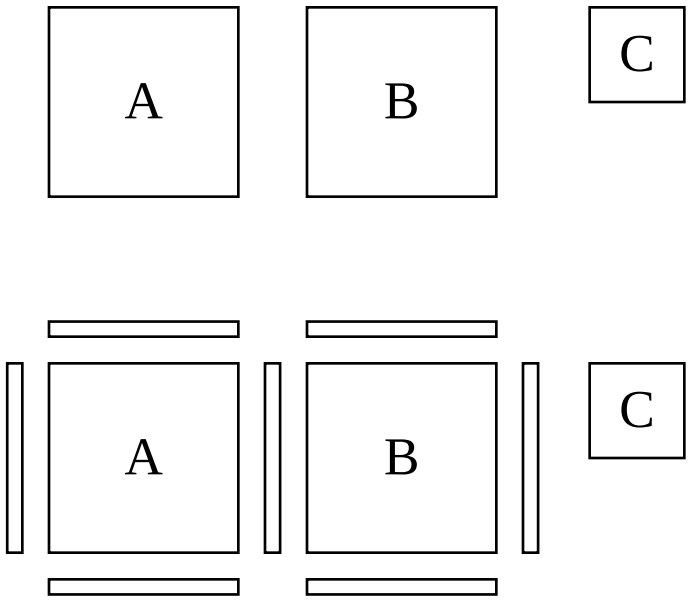


Figure 2.6-1 (a)Illustration of how matching of A and B is disturbed by the presence of C. (b) Improved matching achieved by matching surroundings of A and B

When multiple units are being matched using the unit-matching principle, another issue can arise. Suppose that there is some gradient that causes objects to grow smaller along some path as illustrated in Fig. 2.6-2(a). By design, component A composed of units A1 and A2 should be twice the size of unit component B. However, due to the gradient, component A is less than twice the size of component B. If the gradient is linear, this situation can be resolved by applying the principle of *common-centroid* layout. As illustrated in Fig. 2.6-2(b), component B is placed in the center (the centroid) between the units A_1 and A_2. Now, any linear gradient will cause A1 to change by an amount equal and opposite to A_2 such that their average value remains constant with respect to B. This is easily shown analytically in the following way.

If the linear gradient is described as

$$y = mx + b \tag{1}$$

then for Fig. 2.6-2(a) we have

$$A_1 = mx_1 + b \tag{2}$$

$$A_2 = mx_2 + b \tag{3}$$

$$B = mx_3 + b \tag{4}$$

$$\frac{A_1 + A_2}{B} = \frac{m(x_1 + x_2) + 2b}{mx_3 + b} \tag{5}$$

This ratio cannot be equal to two because

$$x_3 \neq \frac{x_1 + x_2}{2} \tag{6}$$

However, for the case illustrated in Fig. 2.6-2(b) it easy to show that

$$x_2 = \frac{x_1 + x_3}{2} \tag{7}$$

if $x_1 - x_2$, and $x_2 - x_3$ are equal.

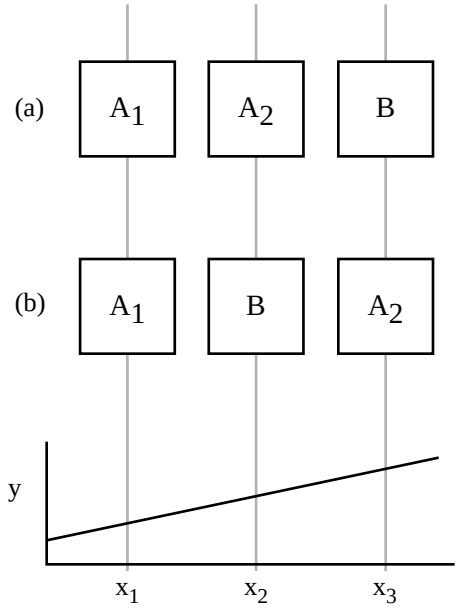


Figure 2.6-2 Components placed in the presence of a gradient,
(a) without common-centroid layout and (b) with common-centroid layout.

The matching principles described thus far should be applied to capacitors when it is desired to match them. In addition, there are other rules that should be applied when dealing with capacitors. When laying out a capacitor, the capacitor's value should be determined by only one plate to reduce its variability. Consider the dual-plate capacitors shown in Fig. 2.6-3. In this figure, the electric field lines are illustrated to indicate that the capacitance between the plates is due to both an area field and fringe field. In Fig. 2.6-3(a) the total capacitance between the two plates will vary if the edges of the top plate indicated by points A and A' move, or if the edges of the bottom plate indicated by points B and B' move. On the other hand, the value of the capacitor illustrated in Fig. 2.6-3(b) is sensitive only to the edge variations of the top plate. Even if the top plate shifts to the left or to the right by a small amount, the capacitance changes very little. The capacitor in Fig. 2.6-3(a) is sensitive to movement of both plates and thus will have greater variability due to process variations that the capacitor in Fig. 2.6-3(b).

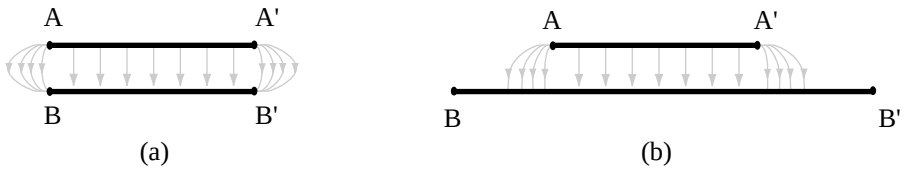


Figure 2.6-3 Side view of a capacitor made from two plates. The capacitor shown in (a) will vary in value do to edge variations at points A,A' and B,B'. The capacitor shown in (b) is not sensitive to edge variations at B,B'. It is only sensitive to edge variations at points A,A'.

The field lines illustrated in Fig. 2.6-3 are helpful to appreciate the fact that the total capacitance between two plates is due to an area component (the classic parallel plate capacitor) and a perimeter component (the fringe capacitance). With this in mind, consider a case where it is desired to ratio two capacitors, C_1 and C_2 by a precise amount (e.g., two to one ratio).

Let C_1 be defined as

$$C_1 = C_{1A} + C_{1P} \tag{8}$$

and C_2 be defined as

$$C_2 = C_{2A} + C_{2P} \tag{9}$$

where

C_{XA} is the area capacitance (parallel-plate capacitance)

C_{XP} is the peripheral capacitance (the fringe capacitance)

The ratio of C_2 to C_1 can be expressed as

$$\frac{C_2}{C_1} = \frac{C_{2A} + C_{2P}}{C_{1A} + C_{1P}} = \frac{C_{2A}}{C_{1A}}\left[\frac{1 + \dfrac{C_{2P}}{C_{2A}}}{1 + \dfrac{C_{1P}}{C_{1A}}}\right] \tag{10}$$

If C_{1P}/C_{1A} equals C_{2P}/C_{2A} then C_2/C_1 is determined by the ratios of capacitor areas only. Thus the equations show that maintaining a constant area-to-perimeter ratio eliminates matching sensitivity due to the perimeter. It should not be a surprise that a constant area-to-perimeter ratio is achieved when the unit-matching principle is applied! At this point it is worthwhile to ask what geometry is best at maintaining constant area-to-perimeter ratio—a square, rectangle, circle, or something else. Referring again to Eq. (10) it is clear that minimizing the perimeter-to-area ratio is a benefit. It is easy to show (see problem 29) that a circle achieves the least perimeter for a given area and thus it is the best choice for minimizing perimeter effects. Moreover, a circle has no corners and corners experience more etch variation than do sides. For a variety of reasons unrelated to the technology, circles may be undesirable. A reasonable compromise between a

square and a circle is a square with chamfered corners (an octagon) as illustrated in Fig. 2.6-4.

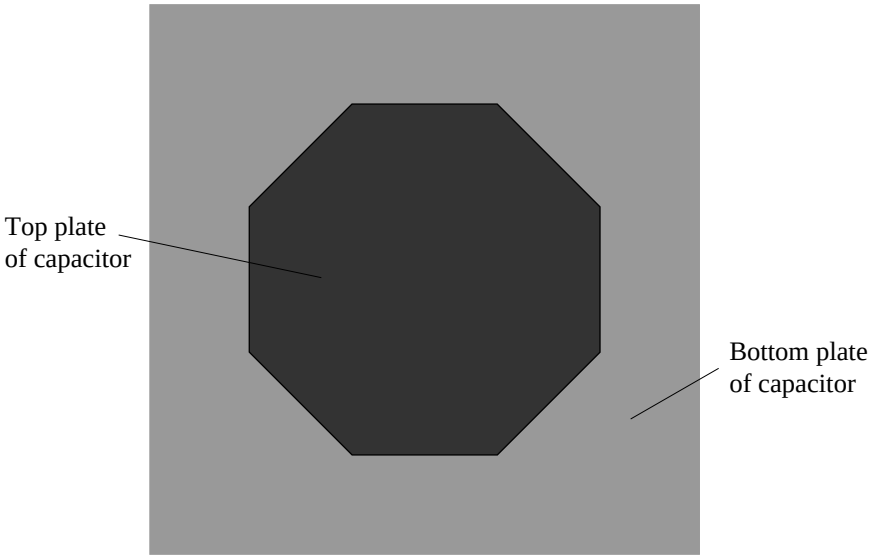


Figure 2.6-4 Illustration of a capacitor using an octagon to approximate a circle to minimize the ratio of perimeter to area.

Another useful capacitor layout technique uses the *Yiannoulos path*[i]. This method uses a serpentine structure that can maintain a constant area-to-perimeter ratio. The beauty of the technique is that you are not limited to integer ratios as is the case when using the unit-matching principle. An example of this layout technique is given in Fig. 2.6-5. It can be easily shown that this structure maintains a constant area-to-perimeter ratio (see problem 30)

[i] This idea was developed by Aristedes A. Yiannoulos.

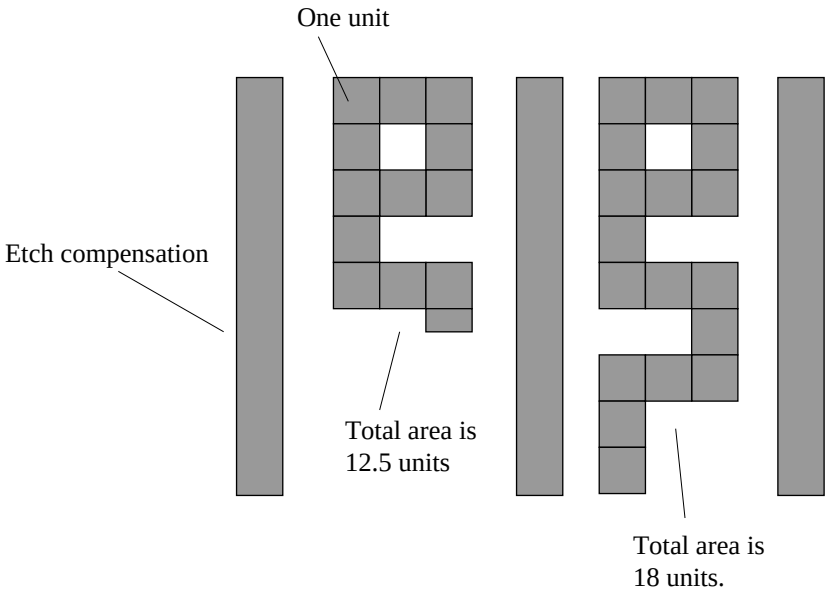


Figure 2.6-5 The Y-path technique for achieving non-integer capacitor ratios while maintaining constant area-to-perimeter ratio.

MOS Transistor Layout

Figure 2.6-6 illustrates the layout of a single MOS transistor and its associated side view. Transistors which are used for analog applications are drawn as linear *stripes* as opposed to a transistor drawn with a bend in the gate. The dimensions that will be important later on are the width and length of the transistor as well as the area and periphery of the drain and source. It is the *W/L* ratio that is the dominant dimensional component governing transistor conduction, and the area and periphery of the drain and source that determine drain and source capacitance on a per-device basis.

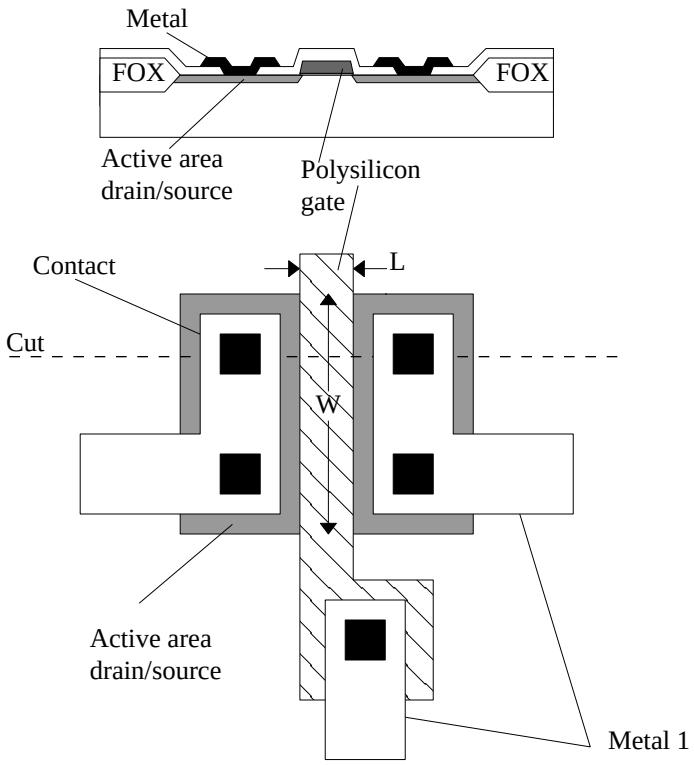
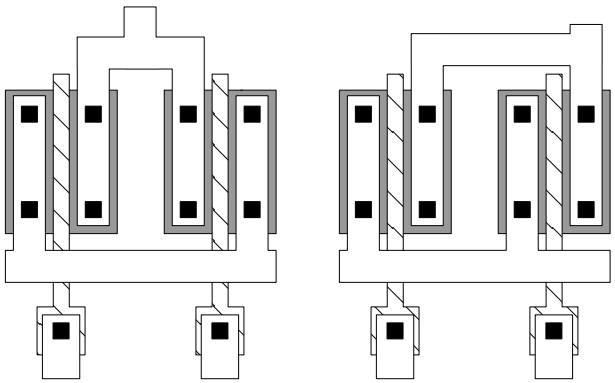


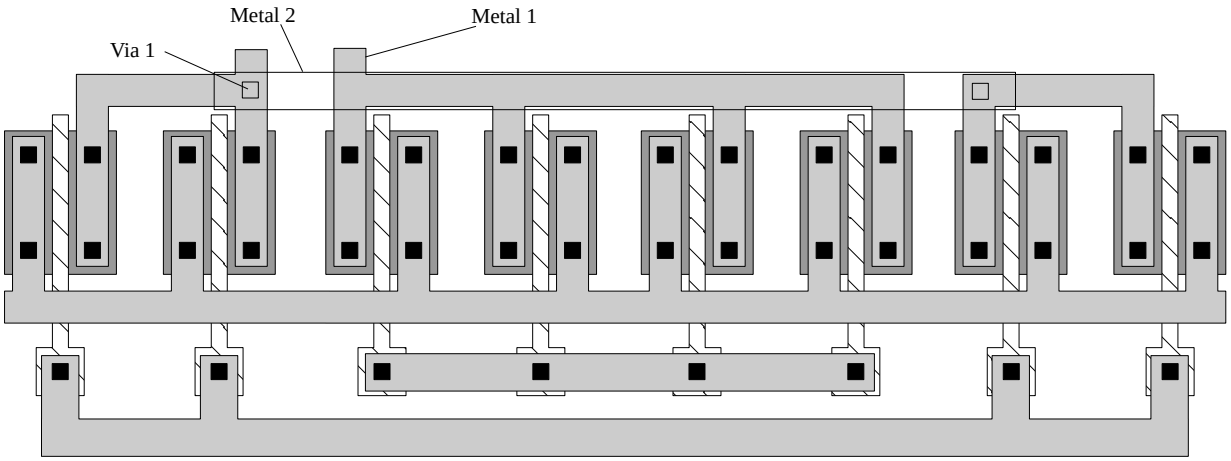
Figure 2.6-6 Example layout of an MOS transistor showing top view and side view at the cut line indicated.

When it is desired to match transistors, the unit-matching principle, and the common-centroid method should be applied. Once applied, the question arises as to whether, the drain/source orientation of the transistors should be mirror symmetric or have the same orientation. In Fig. 2.6-7(a) transistors exhibit mirror symmetry while in Fig. 2.6-7(b) transistors exhibit identical orientation, or *photolithographic invariance* (PLI)[i]. It is not uncommon for the drain/source implant to be applied at an angle. Because of its height (its thickness), polysilicon can shadow the implant on one side or the other causing the gate-source capacitance to differ from the gate-drain capacitance. By applying the PLI layout method, the effect of the implant angle is matched so that the two C_{GS} are matched and the two C_{GD} are matched. In order to achieve both common centroid and PLI layouts, matched transistors must be broken into four units each and laid out in accordance with Fig. 2.6-7(c).

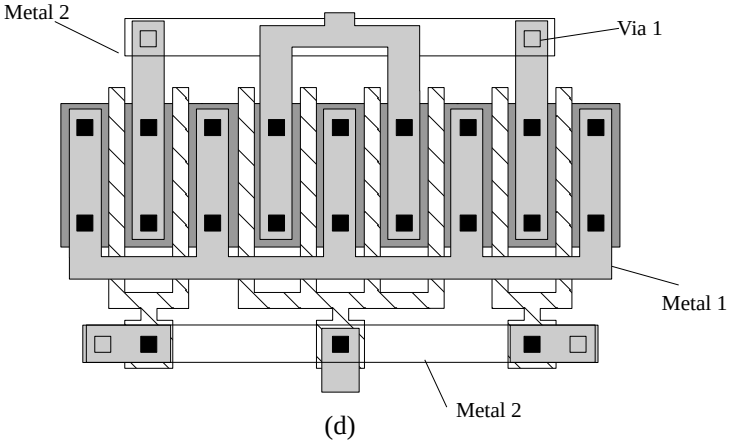
[i] The term "photolithographic invariance" was coined by Eric J. Swanson while at Crystal Semiconductor.



(a) (b)



(c)



(d)

Figure 2.6-7 Example layout of MOS transistors using (a) mirror symmetry, (b) photolithographic invariance, and (c) two transistors sharing a common source and laid out to achieve both photolithographic invariance and common centroid. (d) Compact layout of (c).

Resistor Layout

Figure 2.6-8(a) shows the layout of a resistor. The top view is general in that the resistive component can represent either diffusion (active area) or polysilicon. The side view is particular to the diffusion case. A well resistor is illustrated in Fig. 2.6-8(b). To understand the dimensions that are important in accessing the performance of a resistor, it is necessary to review the relationship for the resistance of a conductive bar.

For a conductive bar of material as shown in Fig. 2.6-9, the resistance R is given as

$$R = \frac{\rho L}{A} \quad (\Omega) \tag{11}$$

where ρ is resistivity in Ω-cm, and A is a plane perpendicular to the direction of current flow. In terms of the dimensions given in Fig. 2.6-9, Eq. (11) can be rewritten as

$$R = \frac{\rho L}{W\mathrm{T}} \quad (\Omega) \tag{12}$$

Since the nominal values for ρ and T are generally fixed for a given process and material type, they are grouped together to form a new term ρ_S called sheet resistivity. This is clarified by the following expression

$$R = \left(\frac{\rho}{\mathrm{T}}\right)\frac{L}{W} = \rho_S \frac{L}{W} \quad (\Omega) \tag{13}$$

It is conventional to give ρ_S the units of Ω/❑ (read *Ohms per square*). From the layout point of view, a resistor has the value determined by the *number of squares* of resistance multiplied by ρ_S.

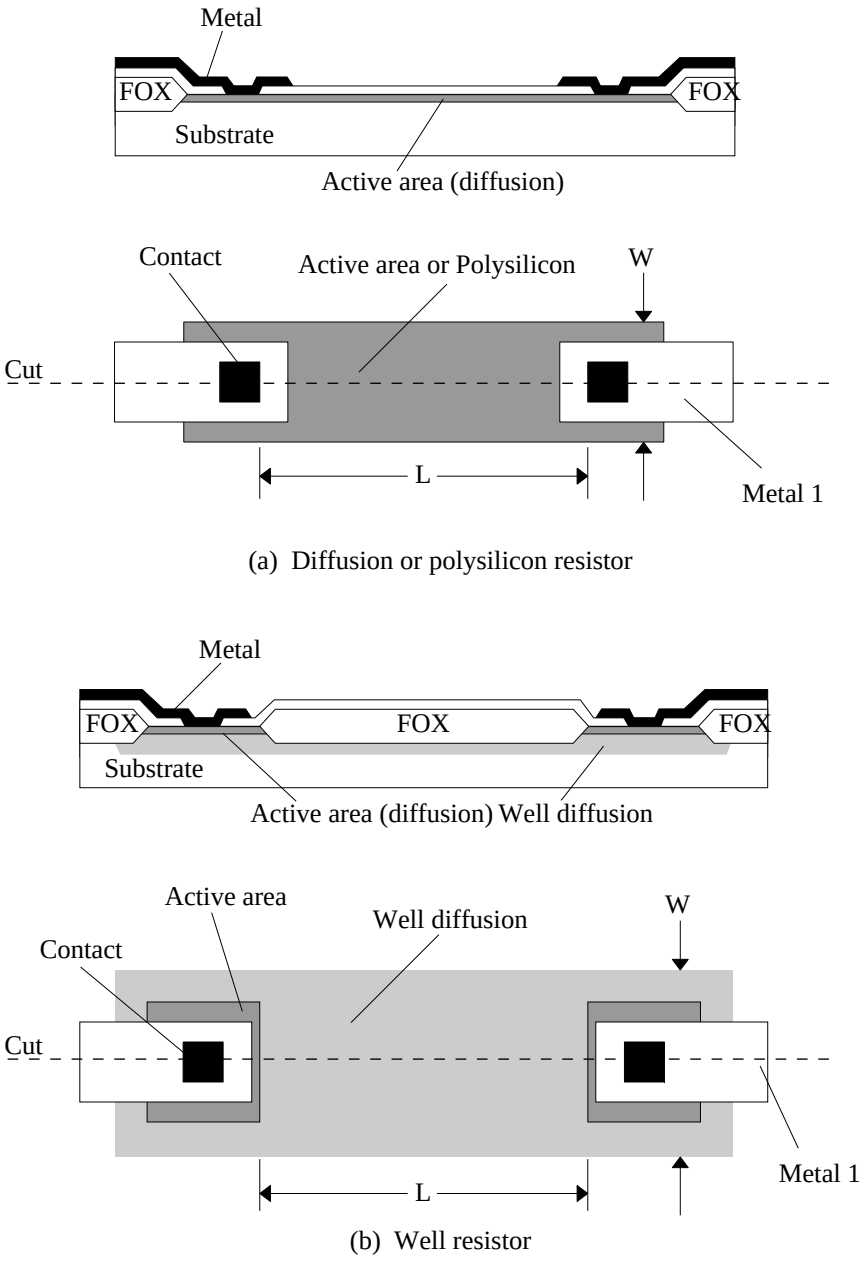


Figure 2.6-8 Example layout of (a) diffusion or polysilicon resistor and (b) Well resistor along with their respective side views at the cut line indicated.

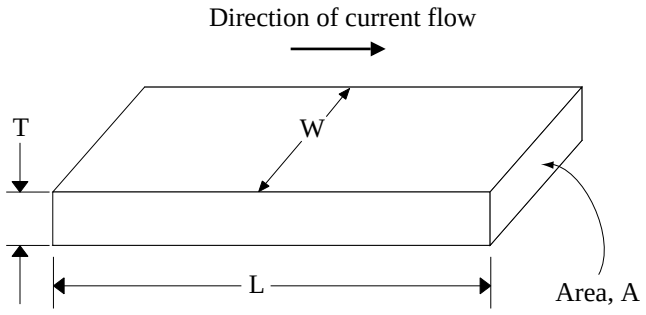


Figure 2.6-9 Current flow in a conductive bar.

Example 2.6-1 Resistance Calculation

Given a polysilicon resistor like that drawn in Fig. 2.6-8(a) with W=0.8μm and L=20μm, calculate ρ_S (in Ω/❑), the number of squares of resistance, and the resistance value. Assume that ρ for polysilicon is 9×10^{-4} Ω-cm and polysilicon is 3000 Å thick. Ignore any contact resistance.

First calculate ρ_S.

$$\rho_S = \frac{\rho}{T} = \frac{9 \times 10^{-4}\ \Omega\text{-cm}}{3000 \times 10^{-8}\ \text{cm}} = 30\ \Omega/\square$$

The number of squares of resistance, N, is

$$N = \frac{L}{W} = \frac{20\mu\text{m}}{0.8\mu\text{m}} = 25$$

giving the total resistance as

$$R = \rho_S \times N = 30 \times 25 = 750\ \Omega$$

Returning to Fig. 2.6-8, the resistance of each resistor shown is determined by the *L/W* ratio and its respective sheet resistance. One should wonder what the true values of *L* and *W* are since, in reality, the current flow is neither uniform nor unidirectional. It is convenient to measure *L* and *W* as shown and then characterize the total resistance in two components: the body component of the resistor (the portion along the length, *L*) and the contact component. One could choose a different approach as long as devices are characterized consistently with the measurement technique (this is covered in more detail in Appendix B on device characterization).

Capacitor Layout

Capacitors can be constructed in a variety of ways depending upon the process as well as the particular application. Only two detailed capacitor layouts will be shown here.

The double-polysilicon capacitor layout is illustrated in Fig. 2.6-10(a). Notice that the second polysilicon layer boundary falls completely within the boundaries of the first polysilicon layer (gate) and the top-plate contact is made at the center of the second polysilicon geometry. This technique minimizes top-plate parasitic capacitance that would have been worsened if the top polysilicon had, instead, followed a path outside the boundary of polysilicon gate and made contact to metal elsewhere.

Purely digital processes do not generally provide double-polysilicon capacitors. Therefore, precision capacitors are generally made using multiple layers of metal. If only one layer of metal exists, a metal-polysilicon capacitor can be constructed. For multi-layer metal processes, polysilicon can still be used as one of the capacitor layers. The problem with using polysilicon as a capacitor layer in this case is that the polysilicon-to-substrate capacitance can represent a substantial parasitic capacitance compared to the desired capacitor. If the additional parasitic capacitance resulting from the use of polysilicon is not a problem, greater per-unit-area capacitance can be achieved with this type of capacitor.

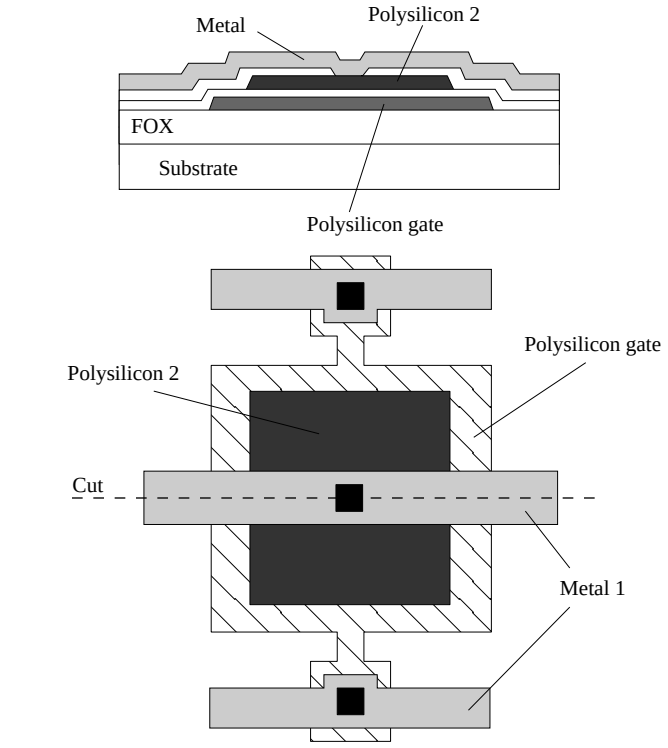
An example of a triple-metal capacitor is illustrated in Fig. 2.6-10(b). In this layout, the top plate of the capacitor is the metal two layer. The bottom plate is made from metals one and three.

The value of integrated circuit capacitors is approximately[i]

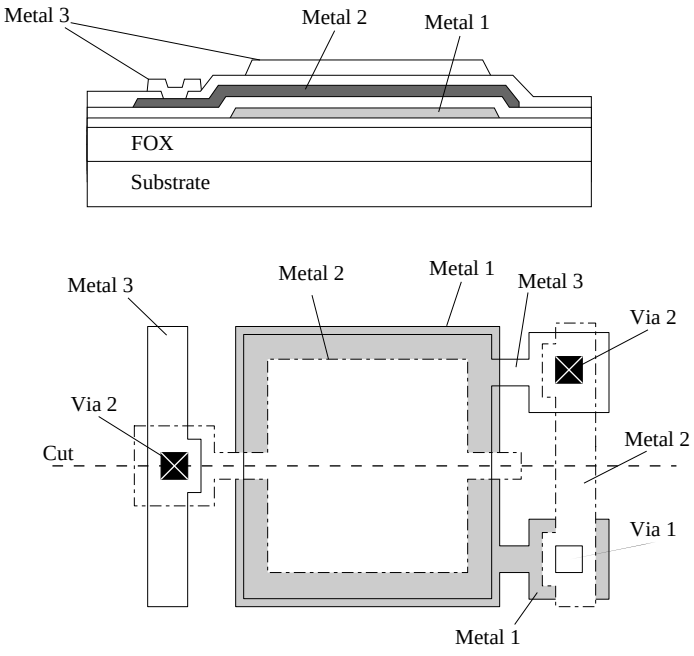
$$C = \frac{\varepsilon_{ox} A}{t_{ox}} = C_{ox} A \tag{14}$$

where ε_{ox} is the dielectric constant of the silicon dioxide (approximately 3.45×10^{-5} pF/μm), t_{ox} is the thickness of the oxide, and A is the area of the capacitor. The value of the capacitor is seen to depend upon the area A and the oxide thickness t_{ox}. There is, in addition, a fringe capacitance that is a function of the periphery of the capacitor. Therefore, errors in the ratio accuracy of two capacitors result from an error in either the ratio of the areas, or the oxide thickness. If the error is caused by a uniform linear variation in the oxide thickness, then a common centroid geometry can be used to eliminate its effects [**29**]. Area related errors result from the inability to precisely define the dimensions of the capacitor on the integrated circuit. This is due to the error tolerance associated with making the mask, the nonuniform etching of the material defining the capacitor plates, and other limitations [**30**].

[i] This is the infinite parallel-plate equation. This expression loses its accuracy as the plate dimensions approach the dimension separating the plates.



(a)



(b)

Figure 2.6-10 Example layout of (a) double-polysilicon capacitor, and (b) triple-level metal capacitor along with their respective side views at the cut line indicated.

The performance of analog sampled-data circuits can be directly related to the capacitors used in the implementation. From the standpoint of analog sampled-data applications, one of the most important characteristics of the capacitor is ratio accuracy [**31**].

Layout Rules

As the layout of an integrated circuit is being drawn, there are *layout rules* that must be observed in order to ensure that the integrated circuit is manufacturable. Layout rules governing manufacturability arise, in part, from the fact that at each mask step in the process, features of the next photomask must be aligned to features previously defined on the integrated circuit. Even when using precision automatic alignment tools, there is still some error in alignment. In some cases, alignment of two layers is critical to circuit operation. As a result, alignment tolerances impose a limitation of feature size and orientation with respect to other layers on the circuit.

Electrical performance requirements also dictate feature size and orientation with respect to other layers. A good example of this is the allowable distance between diffusions supporting a given voltage difference. Understanding the rules associated with electrical performance is most important to the designer if circuits are to be designed that challenge the limits of the technology. The limits for these rules are constrained by the process (doping concentration, junction depth, etc.) characterized under a specific set of conditions.

The following set of design rules are based upon the minimum dimension resolution λ (lambda, not to be confused with the channel length modulation parameter λ which will be introduced in Chapter 3). The minimum dimension resolution λ is typically one-half the minimum geometry allowed by the process technology.

The basic layout levels needed to define a double-metal, bulk, silicon gate CMOS circuit include well (p^- or n^-), active area (AA), polysilicon-gate (poly), second polysilicon (capacitor top plate), contact, metal-1, via, metal-2, and pad opening. The symbols for these levels are shown in Fig. 2.6-11(c). Table 2.6-1 gives the simplified design rules for a polysilicon-gate, bulk CMOS process. Figure 2.6-11 illustrates these rules.

In most cases design rules are unique to each wafer manufacturer. The design rules for the particular wafer manufacturer should be obtained before the design is begun and consulted during the design. This is especially important in the design of state-of-the-art analog CMOS. However, the principles developed here should remain unaltered while translated to specific processes.

Table 2.6-1 Design Rules for a Double-Metal, Double-Polysilicon, N-Well, Bulk CMOS Process.

Minimum Dimension Resolution (λ)

1.	N-Well	
	1A. width	6
	1B. spacing (same potential)	8
	1C. spacing (different potential)	22
2.	Active Area (AA)	
	2A. width	4
	Spacing to Well	
	2B. AA-n contained in n-Well	1

	2C. AA-n external to n-Well	10
	2D. AA-p contained in n-Well	3
	2E. AA-p external to n-Well	7
	Spacing to other AA (inside or outside well)	
	2F. AA to AA (p or n)	3
3.	Polysilicon Gate (Capacitor bottom plate)	
	3A. width	2
	3B. spacing	3
	3C. spacing of polysilicon to AA (over field)	1
	3D. extension of gate beyond AA (transistor width direction)	2
	3E. spacing of gate to edge of AA (transistor length direction)	4
4.	Polysilicon Capacitor top plate	
	4A. width	2
	4B. spacing	2
	4C. spacing to inside of polysilicon gate (bottom plate)	2
5.	Contacts	
	5A. size	2x2
	5B. spacing	4
	5C. spacing to polysilicon gate	2
	5D. spacing polysilicon contact to AA	2
	5E. metal overlap of contact	1
	5F. AA overlap of contact	2
	5G. polysilicon overlap of contact	2
	5H. capacitor top plate overlap of contact	2
6.	Metal-1	
	6A. width	3
	6B. spacing	3
7.	Via	
	7A. size	3x3
	7B. spacing	4
	7C. enclosure by Metal-1	2
	7D. enclosure by Metal-2	2
8.	Metal-2	
	8A. width	4
	8B. spacing	3
	Bonding Pad	
	8C. spacing to AA	24
	8D. spacing to metal circuitry	24
	8E. spacing to polysilicon gate	24
9.	Passivation Opening (Pad)	
	9A. bonding-pad opening	100μm x 100μm
	9B. bonding-pad opening enclosed by Metal-2	8
	9C. bonding-pad opening to pad opening space	40

Note: For a P-Well process, exchange p and n in all instances.

2.7 Summary

This chapter has introduced CMOS technology from the viewpoint of its use to implement analog circuits. The basic semiconductor fabrication processes were described in order to understand the fundamental elements of this technology. The basic fabrication steps include diffusion, implantation, deposition, etching, and oxide growth. These steps are implemented by the use of photolithographic methods which limit the processing steps to certain physical areas of the silicon wafer. The basic processing steps needed to implement a typical silicon-gate CMOS process were described next.

The pn junction was reviewed following the introduction to CMOS technology because it plays an important role in all semiconductor devices. This review examined a step pn junction and developed the physical dimensions, the depletion capacitance, and the voltage-current characteristics of the pn junction. Next, the MOS transistor was introduced and characterized with respect to its behavior. It was shown how the channel between the source and drain is formed and the influence of the gate voltage upon this channel was discussed. The MOS transistor is physically a very simple component. Finally, the steps necessary to fabricate the transistor were presented.

A discussion of possible passive components that can be achieved in CMOS technology followed. These components include only resistors and capacitors. The absolute accuracy of these components depends on their edge uncertainties and improves as the components are made physically larger. The relative accuracy of passive components depends upon type and layout.

The next section discussed further considerations of CMOS technology. These considerations included: the substrate and lateral BJTs compatible with the CMOS process; latch-up, which occurs under certain high-current conditions; the temperature dependence of CMOS components; and the noise sources in these components.

The last section covered the geometrical definition of CMOS devices. This focused on the physical constraints that insure that the devices will work correctly after fabrication. This material will lead naturally to the next chapter where circuit models are developed to be used in analyzing and designing circuits.

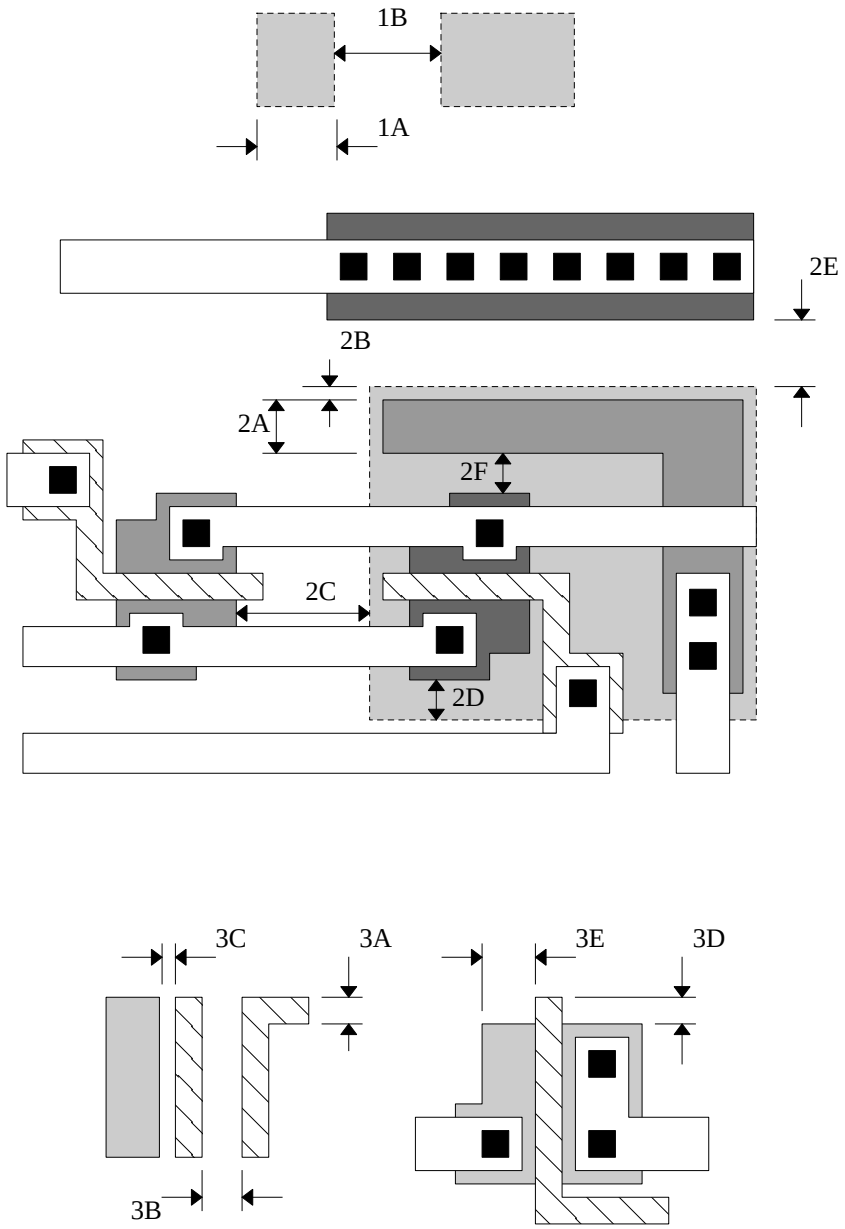


Figure 2.6-11(a) Illustration of the design rules 1-3 of Table 2.6-1.

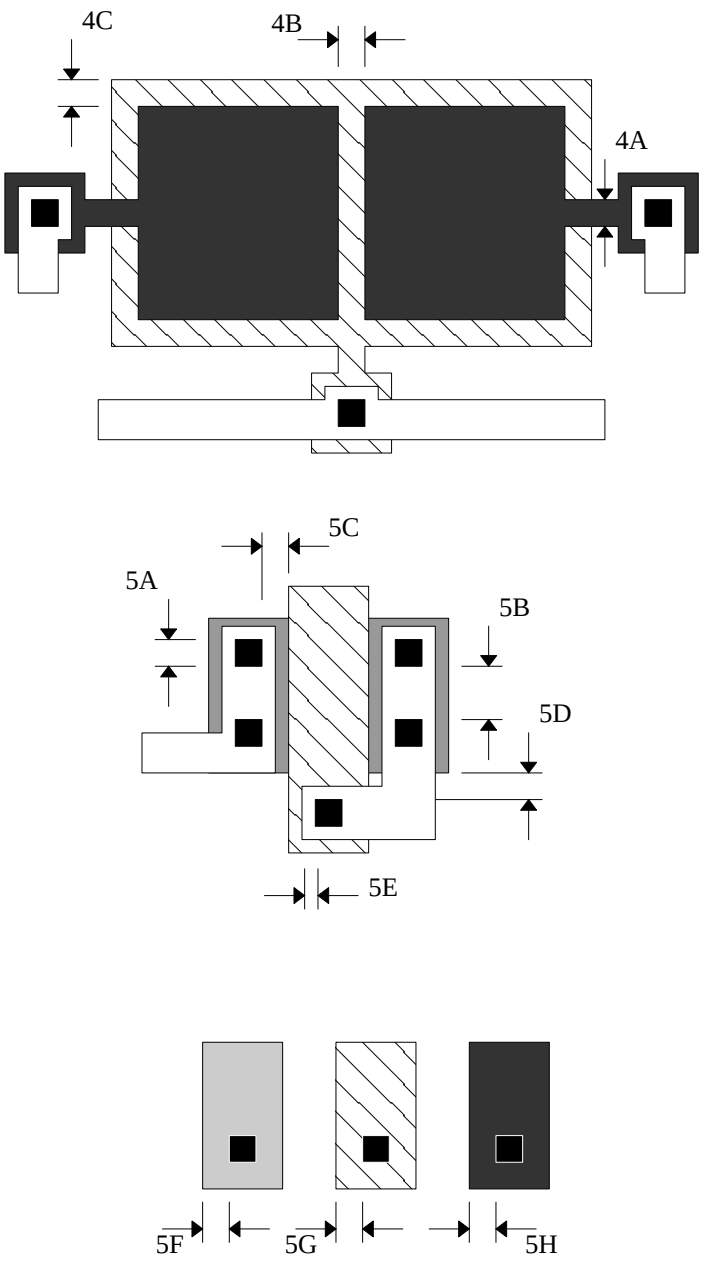


Figure 2.6-11(b) Illustration of the design rules 4-5 of Table 2.6-1.

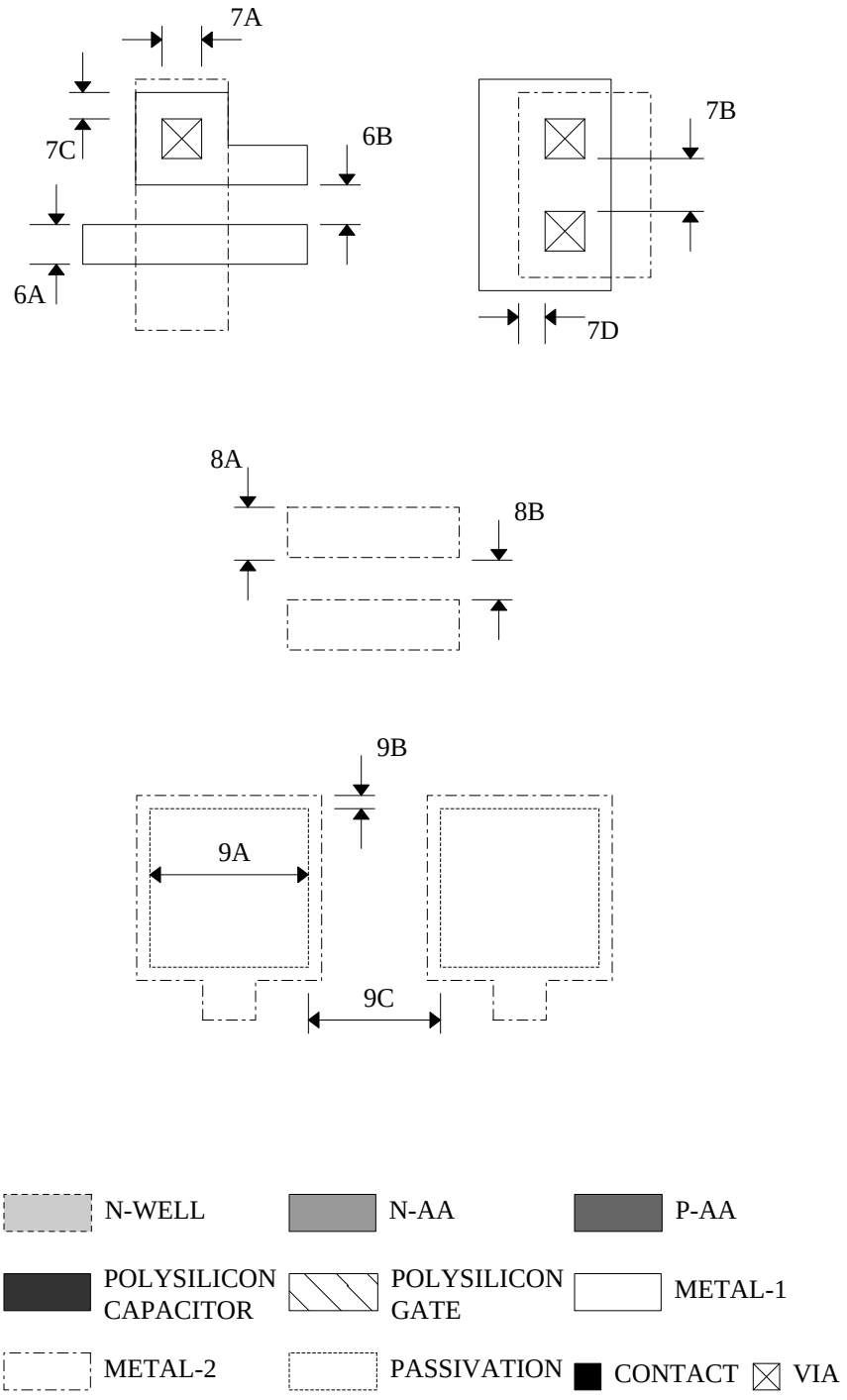


Figure 2.6-11(c) Illustration of the design rules 6-9 of Table 2.6-1.

PROBLEMS

1. List the five basic MOS fabrication processing steps and give the purpose or function of each step.
2. What is the difference between positive and negative photoresist and how is photoresist used?
3. Illustrate the impact on source and drain diffusions of a 7˚ angle off perpendicular ion implant. Assume that the thickness of polysilicon is 8000 Å and that out diffusion from point of ion impact is 0.07 μm.
4. Repeat Example 2.2-1 if the applied voltage is -2 V.
5. Develop Eq. (9) of Sec. 2.2 using Eqs. (1), (7), and (8) of the same section.
6. Redevelop Eqs. (7) and (8) pf Sec. 2.2 if the impurity concentration of a pn junction is given by Fig. 2.2-2 rather than the step junction of Fig. 2.2-1(b).
7. Plot the normalized reverse current, i_{RA}/i_R, versus the reverse voltage v_R of a silicon pn diode which has $BV = 12$ V and $n = 6$.
8. What is the breakdown voltage of a pn junction with $N_A = N_D = 10^{16}/\text{cm}^3$?
9. What change in v_D of a silicon pn diode will cause an increase of 10 (an order of magnitude) in the forward diode current?
10. Explain in your own words why the magnitude of the threshold voltage in Eq. (19) of Sec. 2.3 increases as the magnitude of the source-bulk voltage increases (The source-bulk pn diode remains reversed biased.)
11. If $V_{SB} = 2$ V, find the value of V_T for the n-channel transistor of Ex. 2.3-1.
12. Re-derive Eq. (27) given that V_T is not constant in Eq. (22) but rather varies linearly with $v(y)$ according to the following equation.

$$V_T = V_{T0} + \alpha \, | \, v_{SB} \, |$$

13. If the mobility of an electron is 500 $\text{cm}^2/(\text{V}\cdot\text{s})$ and the mobility of a hole is 200 $\text{cm}^2/(\text{V}\cdot\text{s})$, compare the performance of an n-channel with a p-channel transistor. In particular, consider the value of the transconductance parameter and speed of the MOS transistor.
14. What is the function of silicon nitride in the CMOS fabrication process described in Sec. 2.1?
15. Give typical thicknesses for the field oxide (FOX), thin oxide (TOX), n^+ or p^+, p-well, and metal 1 in units of μm.
16. Given the component tolerances in Table 2.4-1, design the simple lowpass filter illustrated in Fig P2.16 to minimize the variation in pole frequency over all process variations. Pole frequency should be designed to a nominal value of 1MHz. You must choose the appropriate capacitor and resistor type. Explain your reasoning. Calculate the variation of pole frequency over process using the design you have chosen.

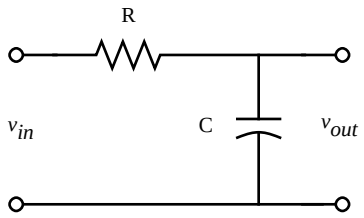


Figure P2.16

17. List two sources of error that can make the actual capacitor, fabricated using a CMOS process, differ from its designed value.
18. What is the purpose of the p^+ implantation in the capacitor of Fig. 2.4-1(a)?
19. Using Ex. 2.3-1 as a starting point, calculate the difference in threshold voltage between two devices whose gate-oxide is different by 5% (i.e., $t_{ox} = 210$ Å).
20. Repeat Ex. 2.3-1 using $N_A = 7 \times 10^{16}$ cm^{-3}, gate doping, $N_D = 1 \times 10^{19}$ cm^{-3}.
21. Consider the circuit in Fig. P2.21. Resistor R_1 is an n-well resistor with a nominal value of 10 kΩ when the voltage at both terminals is 3 V. The input voltage, v_{in}, is a sine wave with an amplitude of 2 VPP and a dc component of 3 V. Under these conditions, the value of R_1 is given as

$$R_1 = R_{nom}\left[1 + K\left(\frac{v_{in} + v_{out}}{2}\right)\right]$$

where R_{nom} is 10K and the coefficient K is the voltage coefficient of an n-well resistor and has a value of 10K ppm/V. Resistor R_2 is an ideal resistor with a value of 10 kΩ. Derive a time-domain expression for v_{out}. Assume that there are no frequency dependencies.

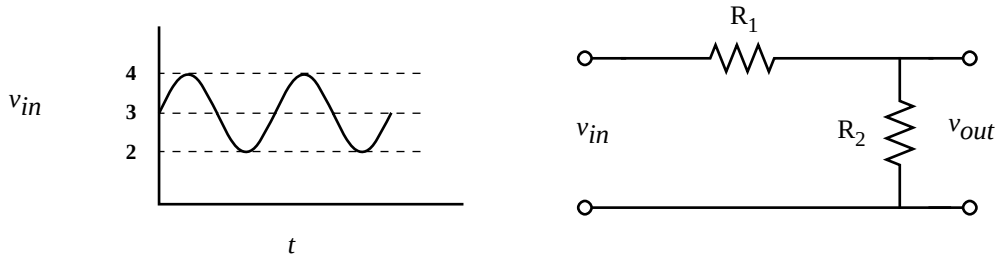


Figure P2.21

22. Repeat problem 21 using a P+ diffused resistor for R_1. Assume that a P+ resistor's voltage coefficient is 200 ppm/V. The n-well in which R1 lies, is tied to a 5 volt supply.
23. Consider problem 22 again but assume that the n-well in which R1 lies is not connected to a 5 volt supply, but rather is connected as shown in Fig. P2.23.

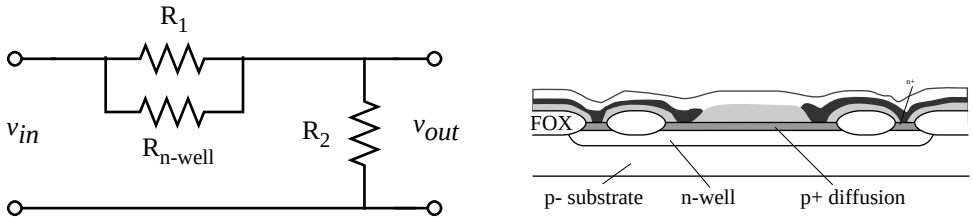
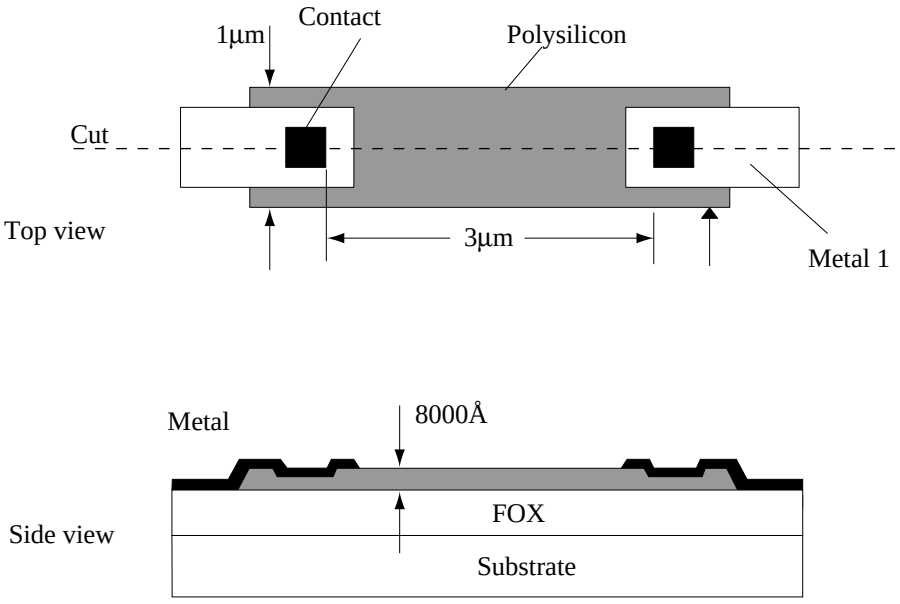


Figure P2.23

24. Assume $v_D = 0.7$ V and find the fractional temperature coefficient of I_S and v_D.
25. Plot the noise voltage as a function of the frequency if the thermal noise is 100 nV/$\sqrt{\text{Hz}}$ and the junction of the 1/f and thermal noise (the 1/f noise corner) is 10,000 Hz.
26. Given the polysilicon resistor in Fig. P2.26 with a resistivity of $\rho = 8\times10^{-4}$ Ω-cm, calculate the resistance of the structure. Consider only the resistance between contact edges. $\rho_S = 50$ Ω/ ❑



Diffusion or polysilicon resistor

Figure P2.26

27. Given that you wish to match two transistors having a W/L of 100μm/0.8μm each. Sketch the layout of these two transistors to achieve the best possible matching.
28. Assume that the edge variation of the top plate of a capacitor is 0.05μm and that capacitor top plates are to be laid out as squares. It is desired to match two equal capacitors to an accuracy of 0.1%. Assume that there is no variation in oxide thickness. How large would the capacitors have to be to achieve this matching accuracy?

29. Show that a circular geometry minimizes perimeter-to-area ratio for a given area requirement. In your proof, compare against rectangle and square.
30. Show analytically how the Yiannoulos-path technique illustrated in Fig. 2.6-5 maintains a constant area-to-perimeter ratio with non-integer ratios.
31. Design an optimal layout of a matched pair of transistors whose W/L are 8μm/1μm. The matching should be photolithographic invariant as well as common centroid.
32. Figure P.32 illustrates various ways to implement the layout of a resistor divider. Choose the layout that BEST achieves the goal of a 2:1 ratio. Explain why the other choices are not optimal.

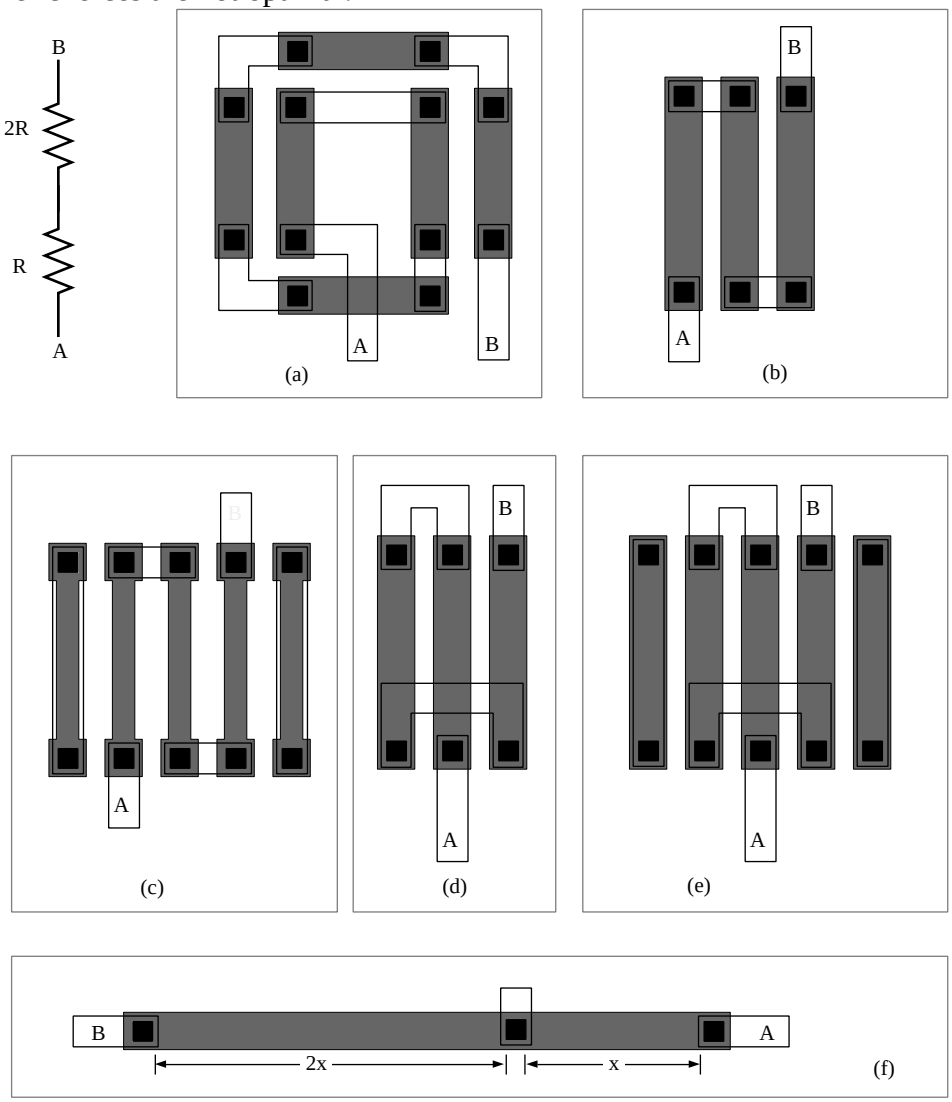


Figure P2.32

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Chapter 3 CMOS Device Modeling

Before one can design a circuit to be integrated in CMOS technology, one must first have a model describing the behavior of all the components available for use in the design. A model can take the form of mathematical equations, circuit representations, or tables. Most of the modeling used in this text will focus on the active and passive devices discussed in the previous chapter as opposed to higher-level modeling such as macromodeling, or behavioral modeling.

It should be stressed at the outset that a model is just that and no more—it is not the real thing! In an ideal world, we would have a model that accurately describes the behavior of a device under all possible conditions. Realistically, we are happy to have a model that predicts simulated performance to within a few percent of measured performance. There is no clear agreement as to which model comes closest to meeting this "ideal" model [1]. This lack of agreement is illustrated by the fact that, at this writing, HSPICE [25] offers the user 43 different MOS transistor models from which to choose!

This text will concentrate only three of these models. The simplest model which is appropriate for hand calculations was described in Sec 2.3 and will be further developed here to include capacitance, noise, and ohmic resistance. In SPICE terminology, this simple model is called the LEVEL 1 model. Next, a small-signal model is derived from the LEVEL 1 large-signal model and is presented in Sec. 3.3.

A far more complex model, the SPICE LEVEL 3 model is presented in Sec. 3.4. This model includes many effects that are more evident in modern short-channel technologies as well as subthreshold conduction. It is adequate for device geometries down to about 0.8μm. Finally, the BSIM3v3 model is presented. This model is the closest to becoming a standard for computer simulation.

Notation

SPICE was originally implemented in FORTRAN where all input was required to be uppercase ASCII characters. Lowercase, greek, and super/subscripting were not allowed. Modern SPICE implementations generally accept (but do not distinguish between) upper- and lowercase but the tradition of using uppercase ASCII still lives on. This is particularly evident in the device model parameters. Since greek characters are not available, these were simply spelled out, e.g., γ entered as GAMMA. Super and subscripts were simply not used.

It is inconvenient to adopt the SPICE naming convention throughout the book because equations would appear unruly and would not be familiar to what is commonly seen in the literature. On the other hand, it is necessary to provide the correct notation where application to SPICE is intended. To address this dilemma, we have decided to use SPICE uppercase (non italic) notation for all model parameters except those applied to the simple model (SPICE LEVEL 1).

3.1 Simple MOS Large-Signal

All large-signal models will be developed for the n-channel MOS device with the positive polarities of voltages and currents shown in Fig. 3.1-1(a). The same models can be used for the p-channel MOS device if all voltages and currents are multiplied by -1 and the absolute value of the p-channel threshold is used. This is equivalent to using the voltages and currents defined by Fig. 3.1-1(b) which are all positive quantities. As

mentioned in Chapter 1, lower-case variables with capital subscripts will be used for the variables of large-signal models and lower-case variables with lower-case subscripts will be used for the variables of small-signal models. When the voltage or current is a model parameter, such as threshold voltage, it will be designated by an upper-case variable and an upper-case subscript.

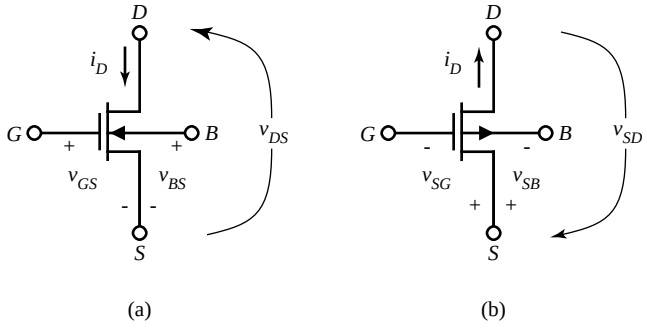


Figure 3.1-1 Positive sign convention for (a) n-channel, and (b) p-channel MOS transistor.

When the length and width of the MOS device is greater than about 10 μm, the substrate doping is low, and when a simple model is desired, the model suggested by Sah [2] and used in SPICE by Shichman and Hodges [3] is very appropriate. This model was developed in Eq. (28) of Sec. 2.3 and given below.

$$i_D = \frac{\mu_o C_{ox} W}{L}\left[(v_{GS} - V_T) - \left(\frac{v_{DS}}{2}\right)\right] v_{DS} \tag{1}$$

The terminal voltages and currents have been defined in the previous chapter. The various parameters of (1) are defined as

μ_o = surface mobility of the channel for the n-channel or p-channel device (cm^2/V-s)

$C_{ox} = \dfrac{\varepsilon_{ox}}{t_{ox}}$ = capacitance per unit area of the gate oxide (F/cm^2)

W = effective channel width

L = effective channel length

The threshold voltage V_T is given by Eq. (19) of Sec. 2.3 for an n-channel transistor

$$V_T = V_{T0} + \gamma\left[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\right] \tag{2}$$

$$V_{T0} = V_T\,(v_{SB} = 0) = V_{FB} + 2|\phi_F| + \frac{\sqrt{2q\varepsilon_{si}\, N_{SUB}\, 2|\phi_F|}}{C_{ox}} \tag{3}$$

$$\gamma = \text{bulk threshold parameter (V}^{1/2}) = \frac{\sqrt{2\varepsilon_{si}\, q\, N_{SUB}}}{C_{ox}} \tag{4}$$

$$\phi_F = \text{strong inversion surface potential (V)} = -\frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right) \tag{5}$$

$$V_{FB} = \text{flatband voltage (V)} = \phi_{MS} - \frac{Q_{ss}}{C_{ox}} \tag{6}$$

$$\phi_{MS} = \phi_F \text{ (substrate)} - \phi_F \text{ (gate)} \qquad \text{[Eq. (17) of Sec. 2.3]} \tag{7}$$

$$\phi_F(\text{substrate}) = -\frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right) \quad \text{[n-channel with p-substrate]} \tag{8}$$

$$\phi_F(\text{gate}) = \frac{kT}{q}\ln\left(\frac{N_{GATE}}{n_i}\right) \quad \text{[n-channel with } n^+ \text{ polysilicon gate]} \tag{9}$$

$$Q_{ss} = \text{oxide charge} = q\,N_{ss} \tag{10}$$

k = Boltzmann's constant

T = temperature (K)

n_i = intrinsic carrier concentration

Table 3.1-1 gives some of the pertinent constants for silicon.

Table 3.1-1 Constants for Silicon.

Constant Symbol	Constant Description	Value	Units
V_G	Silicon bandgap (27°C)	1.205	V
k	Boltzmann's constant	1.381×10^{-23}	J/K
n_i	Intrinsic carrier concentration (27°C)	1.45×10^{10}	cm^{-3}
ε_0	Permittivity of free space	8.854×10^{-14}	F/cm
ε_{si}	Permittivity of silicon	$11.7\ \varepsilon_0$	F/cm
ε_{ox}	Permittivity of SiO_2	$3.9\ \varepsilon_0$	F/cm

A unique aspect of the MOS device is its dependence upon the voltage from the source to bulk as shown by Eq. (2). This dependence means that the MOS device must be treated as a four-terminal element. It will be shown later how this behavior can influence both the large- and small-signal performance of MOS circuits.

In the realm of circuit design, it is more desirable to express the model equations in terms of electrical rather than physical parameters. For this reason, the drain current is often expressed as

$$i_D = \beta\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right]v_{DS} \tag{11}$$

or

$$i_D = K' \frac{W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right] v_{DS} \tag{12}$$

where the transconductance parameter β is given in terms of physical parameters as

$$\beta = (K') \frac{W}{L} \cong (\mu_o C_{ox}) \frac{W}{L} \quad (\text{A/V}^2) \tag{13}$$

When devices are characterized in the nonsaturation region with low gate and drain voltages the value for K' is approximately equal to $\mu_o C_{ox}$ in the simple model. This is not the case when devices are characterized with larger voltages introducing effects such as mobility degradation. For these latter cases, K' is usually smaller. Typical values for the model parameters of Eq. (12) are given in Table 3.1-2.

Table 3.1-2 Model Parameters for a Typical CMOS Bulk Process Suitable for Hand Calculations Using the Simple Model. These Values Are Based upon a 0.8 μm Silicon-Gate Bulk CMOS n-Well Process.

Parameter Symbol	Parameter Description	Typical Parameter Value N-Channel	P-Channel	Units
V_{T0}	Threshold Voltage ($V_{BS} = 0$)	0.7 ± 0.15	−0.7 ± 0.15	V
K'	Transconductance Parameter (in saturation)	110.0 ± 10%	50.0 ± 10%	μA/V^2
γ	Bulk threshold parameter	0.4	0.57	(V)$^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1 μm) 0.01 (L=2 μm)	0.05 (L = 1 μm) 0.01 (L = 2 μm)	(V)$^{-1}$
$2\lvert\phi_F\rvert$	Surface potential at strong inversion	0.7	0.8	V

There are various regions of operation of the MOS transistor based on the model of Eq. (1). These regions of operation depend upon the value of $v_{GS} - V_T$. If $v_{GS} - V_T$ is zero or negative, then the MOS device is in the cutoff[i] region and Eq. (1) becomes

$$i_D = 0, \qquad v_{GS} - V_T \le 0 \tag{14}$$

In this region, the channel acts like an open circuit.

A plot of Eq. (1) with $\lambda = 0$ as a function of v_{DS} is shown in Fig. 3.1-2 for various values of $v_{GS} - V_T$. At the maximum of these curves the MOS transistor is said to saturate. The value of v_{DS} at which this occurs is called the saturation voltage and is given as

$$v_{DS}(\text{sat}) = v_{GS} - V_T \tag{15}$$

[i] We will learn later that MOS transistors can operate in the subthreshold region where the gate-source voltage is less than the threshold voltage.

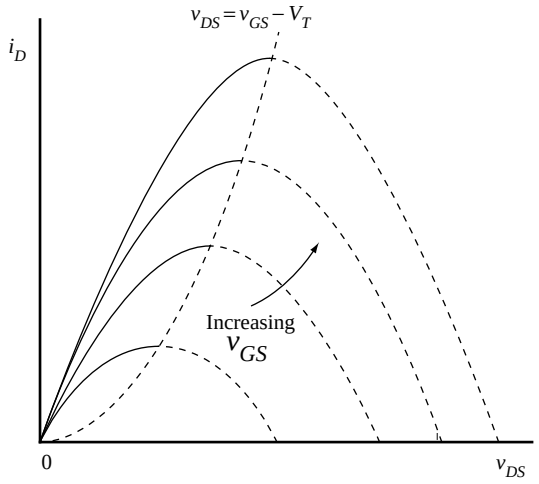


Figure 3.1-2 Graphical illustration of the modified Sah equation.

Thus, v_{DS}(sat) defines the boundary between the remaining two regions of operation. If v_{DS} is less than v_{DS}(sat), then the MOS transistor is in the nonsaturated region and Eq. (1) becomes

$$i_D = (K')\frac{W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right]v_{DS} \quad ; \quad 0 < v_{DS} \leq (v_{GS} - V_T) \tag{16}$$

In Fig. 3.1-2, the nonsaturated region lies between the vertical axis ($v_{DS} = 0$) and $v_{DS} = v_{GS} - V_T$ curve.

The third region occurs when v_{DS} is greater than v_{DS}(sat) or $v_{GS} - V_T$. At this point the current i_D becomes independent of v_{DS}. Therefore, v_{DS} in Eq. (1) is replaced by v_{DS}(sat) of Eq. (11) to get

$$i_D = K'\frac{W}{2L}(v_{GS} - V_T)^2, \quad 0 < (v_{GS} - V_T) \leq v_{DS} \tag{17}$$

Equation (17) indicates that drain current remains constant once v_{DS} is greater than $v_{GS} - V_T$. In reality, this is not true. As drain voltage increases, the channel length is reduced resulting in increased current. This phenomenon is called *channel length modulation* and is accounted for in the saturation model with the addition of the factor, $(1 + \lambda v_{DS})$ where v_{DS} is the actual drain-source voltage and not v_{DS}(sat). The saturation region model modified to include channel-length modulation is given in Eq. (18)

$$i_D = K'\frac{W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS}), \quad 0 < (v_{GS} - V_T) \leq v_{DS} \tag{18}$$

The output characteristics of the MOS transistor can be developed from Eqs. (14), (16), and (18). Figure 3.1-3 shows these characteristics plotted on a normalized basis. These curves have been normalized to the upper curve where V_{GS0} is defined as the value of v_{GS} which causes a drain current of I_{D0} in the saturation region. The entire characteristic is developed by extending the solid curves of Fig. 3.1-2 horizontally to the

right from the maximum points. The solid curves of Fig. 3.1-3 correspond to $\lambda = 0$. If $\lambda \neq 0$, then the curves are the dashed lines.

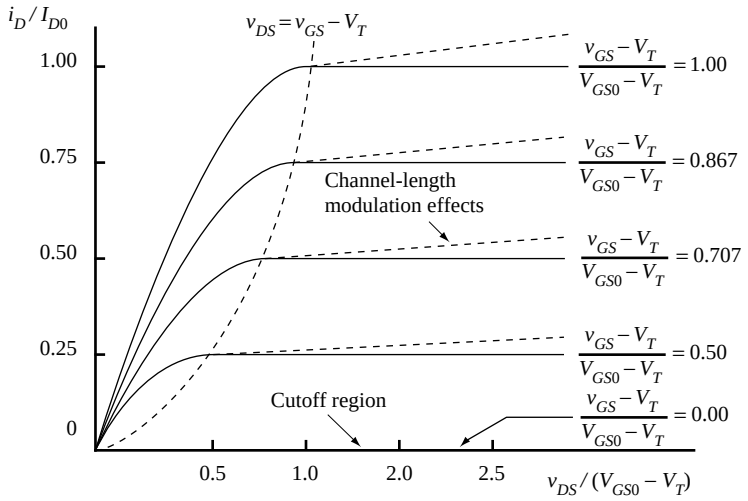


Figure 3.1-3 Output characteristics of the MOS device.

Another important characteristic of the MOS transistor can be obtained by plotting i_D versus v_{GS} using Eq. (18). Fig. 3.1-4 shows this result. This characteristic of the MOS transistor is called the transconductance characteristic. We note that the transconductance characteristic in the saturation region can be obtained from Fig. 3.1-3 by drawing a vertical line to the right of the parabolic dashed line and plotting values of i_D versus v_{GS}. Fig. 3.1-4 is also useful for illustrating the effect of the source-bulk voltage, v_{SB}. As the value of v_{SB} increases, the value of V_T increases for the enhancement, n-channel devices (for a p-channel device, $|V_T|$ increases as v_{BS} increases). V_T also increases positively for the n-channel depletion device, but since V_T is negative, the value of V_T approaches zero from the negative side. If v_{SB} is large enough, V_T will actually become positive and the depletion device becomes an enhancement device.

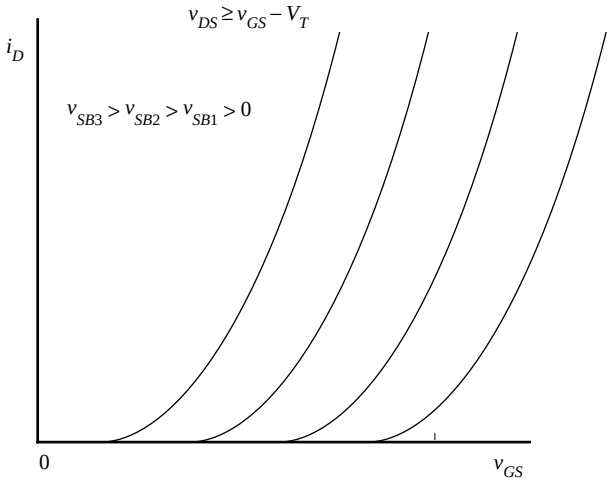


Figure 3.1-4 Transconductance characteristic of the MOS transistor as a function of the bulk-source voltage, v_{SB}.

Since the MOS transistor is a bidirectional device, determining which physical node is the drain and which the source may seem arbitrary. This is not really the case. For an n-channel transistor, the source is always at the lower potential of the two nodes. For the p-channel transistor, the source is always at the higher potential. It is obvious that the drain and source designations are not constrained to a given node of a transistor but can switch back and forth depending upon the terminal voltages applied to the transistor.

A circuit version of the large-signal model of the MOS transistor consists of a current source connected between the drain and source terminals, that depends on the drain, source, gate, and bulk terminal voltages defined by the simple model described in this section. This simple model has five electrical and process parameters that completely define it. These parameters are K', V_T, γ, λ, and $2\phi_F$. The subscript n or p will be used when the parameter refers to an n-channel or p-channel device, respectively. They constitute the Level I model parameters of SPICE [23]. Typical values for these model parameters are given in Table 3.1-2.

The function of the large-signal model is to solve for the drain current given the terminal voltages of the MOS device. An example will help to illustrate this as well as show how the model is applied to the p-channel device.

Example 3.1-1 Application of the Simple MOS Large Signal Model

Assume that the transistors in Fig. 3.1-1 have a W/L ratio of 5 μm/1 μm and that the large signal model parameters are those given in Table 3.1-2. If the drain, gate, source, and bulk voltages of the n-channel transistor is 3 V, 2 V, 0 V, and 0 V, respectively, find the drain current. Repeat for the p-channel transistor if the drain, gate, source, and bulk voltages are −3 V, −2 V, 0 V, and 0 V, respectively.

We must first determine in which region the transistor is operating. Eq. (15) gives v_{DS}(sat) as 2 V − 0.7 V = 1.3 V. Since v_{DS} is 3 V, the n-channel transistor is in the saturation region. Using Eq. (18) and the values from Table 3.1-2 we have

$$i_D = \frac{K'_N W}{2L}(v_{GS} - V_{TN})^2(1 + \lambda_N v_{DS})$$

$$= \frac{110 \times 10^{-6}(5\ \mu\text{m})}{2(1\ \mu\text{m})}(2 - 0.7)^2(1 + 0.04 \times 3) = 520\ \mu\text{A}$$

Evaluation of Eq. (15) for the p-channel transistor is given as

$$v_{SD}(\text{sat}) = v_{SG} - |V_{TP}| = 2\text{ V} - 0.7\text{ V} = 1.3\text{ V}$$

Since v_{SD} is 3 V, the p-channel transistor is also in the saturation region, Eq. (17) is applicable. The drain current of Fig. 3.1-1(b) can be found using the values from Table 3.1-2 as

$$i_D = \frac{K'_P W}{2L}(v_{SG} - |V_{TP}|)^2(1 + \lambda_P v_{SD})$$

$$= \frac{50 \times 10^{-6}(5\ \mu\text{m})}{2(1\ \mu\text{m})}(2 - 0.7)^2(1 + 0.05 \times 3) = 243\ \mu\text{A}$$

It is often useful to describe v_{GS} in terms of i_D in saturation as shown below.

$$v_{GS} = V_T + \sqrt{\frac{2i_D}{\beta}} \tag{19}$$

This expressions illustrates that there are two components to v_{GS} —an amount to invert the channel plus an additional amount to support the desired drain current. This second component is often referred to in the literature as V_{ON}. Thus V_{ON} can be defined as

$$V_{ON} = \sqrt{\frac{2i_D}{\beta}} \tag{20}$$

The term V_{ON} should be recognized as the term for saturation voltage V_{DS} (sat). They can be used interchangeably.

3.2 Other MOS Large-Signal Model Parameters

The large-signal model also includes several other characteristics such as the source/drain bulk junctions, source/drain ohmic resistances, various capacitors, and noise. The complete version of the large-signal model is given in Fig. 3.2-1.

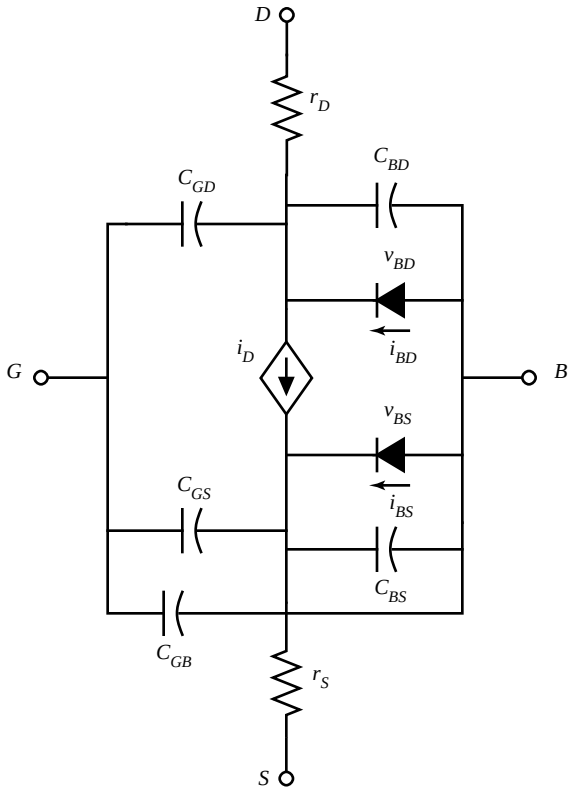


Figure 3.2-1 Complete large-signal model for the MOS transistor.

The diodes of Fig. 3.2-1 represent the pn junctions between the source and substrate and the drain and substrate. For proper transistor operation, these diodes must always be reverse biased. Their purpose in the dc model is primarily to model leakage currents. These currents are expressed as

$$i_{BD} = I_S\left[\exp\left(\frac{qv_{BD}}{kT}\right)-1\right] \tag{1}$$

and

$$i_{BS} = I_S\left[\exp\left(\frac{qv_{BS}}{kT}\right)-1\right] \tag{2}$$

where I_s is the reverse saturation current of a pn junction, q is the charge of an electron, k is Boltzmann's constant, and T is temperature in Kelvin units.

The resistors r_D and r_S represent the ohmic resistance of the drain and source, respectively. Typically, these resistors may be 50 to 100 ohms[i] and can often be ignored at low drain currents.

The capacitance of Fig. 3.2-1 can be separated into three types. The first type includes capacitors C_{BD} and C_{BS} which are associated with the back-biased depletion region between the drain and substrate and the source and substrate. The second type includes capacitors C_{GD}, C_{GS}, and C_{GB} which are all common to the gate and are

[i] For a silicide process, these resistances will be much less—on the order of 5 to 10 ohms.

dependent upon the operating condition of the transistor. The third type includes parasitic capacitors which are independent of the operating conditions.

The depletion capacitors are a function of the voltage across the pn junction. The expression of this junction-depletion capacitance is divided into two regions to account for the high injection effects. The first is given as

$$C_{BX} = (\text{CJ})\,(\text{AX})\left[1 - \frac{v_{BX}}{\text{PB}}\right]^{-\text{MJ}}, \qquad v_{BX} \le (\text{FC})(\text{PB}) \tag{3}$$

where

$X = D$ for C_{BD} or $X = S$ for C_{BS}

AX = area of the source (X = S) or drain (X = D)

CJ = zero-bias ($v_{BX} = 0$) junction capacitance (per unit area)

$$\text{CJ} \cong \sqrt{\frac{q\varepsilon_{si}N_{SUB}}{2\text{PB}}}$$

PB = bulk junction potential (same as ϕ_o given in Eq. (6), sec. 2.2)

FC = forward-bias nonideal junction-capacitance coefficient ($\cong 0.5$)

MJ = bulk-junction grading coefficient (1/2 for step junctions and 1/3 for graded junctions)

The second region is given as

$$C_{BX} = \frac{(\text{CJ})(\text{AX})}{(1 - \text{FC})^{1+\text{MJ}}}\left[1 - (1 + \text{MJ})\text{FC} + \text{MJ}\,\frac{v_{BX}}{\text{PB}}\right], \qquad v_{BX} > (\text{FC})(\text{PB}) \tag{4}$$

Fig. 3.2-2 illustrates how the junction-depletion capacitances of Eqs. (3) and (4) are combined to model the large signal capacitances C_{BD} and C_{BS}. It is seen that Eq. (4) prevents C_{BX} from approaching infinity as v_{BX} approaches PB.

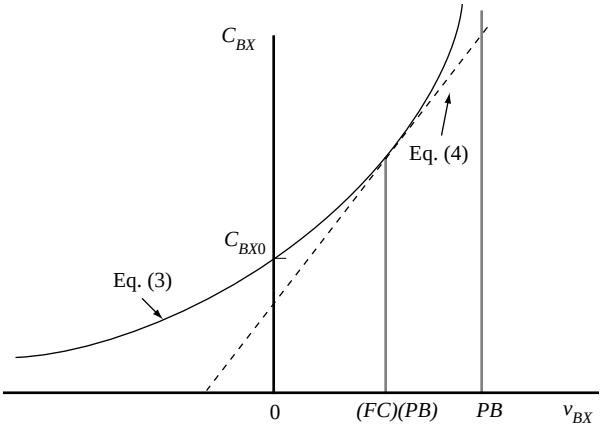


Figure 3.2-2 Example of the method of modeling the voltage dependence of the bulk junction capacitances.

A closer examination of the depletion capacitors in Fig. 3.2-3 shows that this capacitor is like a tub. It has a bottom with an area equal to the area of the drain or source. However, there are the sides that are also part of the depletion region. This area is called the sidewall. A_{BX} in Eqs. (3) and (4) should include both the bottom and sidewall assuming the zero-bias capacitances of the two regions are similar. To more closely model the depletion capacitance, break it into the bottom and sidewall components, given as follows.

$$C_{BX} = \frac{(\text{CJ})(\text{AX})}{\left[1 - \left(\frac{v_{BX}}{\text{PB}}\right)\right]^{\text{MJ}}} + \frac{(\text{CJSW})(\text{PX})}{\left[1 - \left(\frac{v_{BX}}{\text{PB}}\right)\right]^{\text{MJSW}}}, \quad v_{BX} \leq (\text{FC})(\text{PB}) \tag{5}$$

and

$$C_{BX} = \frac{(\text{CJ})(\text{AX})}{(1 - \text{FC})^{1+\text{MJ}}}\left[1 - (1 + \text{MJ})\text{FC} + \text{MJ}\,\frac{v_{BX}}{\text{PB}}\right]$$

$$+ \frac{(\text{CJSW})(\text{PX})}{(1 - \text{FC})^{1+\text{MJSW}}}\left[1 - (1 + \text{MJSW})\text{FC} + \frac{v_{BX}}{\text{PB}}(\text{MJSW})\right],$$

$$v_{BX} \geq (\text{FC})(\text{PB}) \tag{6}$$

where

AX = area of the source ($X = S$) or drain ($X = D$)

PX = perimeter of the source ($X = S$) or drain ($X = D$)

CJSW = zero-bias, bulk-source/drain sidewall capacitance

MJSW = bulk-source/drain sidewall grading coefficient

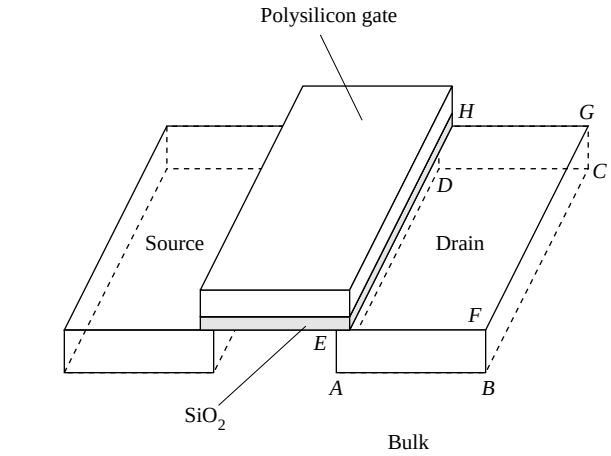


Figure 3.2-3 Illustration showing the bottom and sidewall components of the bulk junction capacitors.

Table 3.2-1 gives the values for CJ, CJSW, MJ, and MJSW for an MOS device which has an oxide thickness of 140 Å resulting in a $C_{ox} = 24.7 \times 10^{-4}$ F/m^2. It can be seen that the depletion capacitors cannot be accurately modeled until the geometry of the device is known, e.g., the area and perimeter of the source and drain. However, values can be assumed for the purpose of design. For example, one could consider a typical source or drain to be 1.8 μm by 5 μm. Thus a value for C_{BX} of 2.9 fF and 6.9 fF results, for n-channel and p-channel devices respectively, for $V_{BX} = 0$.

The large-signal, charge-storage capacitors of the MOS device consist of the gate-to-source (C_{GS}), gate-to-drain (C_{GD}), and gate-to-bulk (C_{GB}) capacitances. Figure 3.2-4 shows a cross section of the various capacitances that constitute the charge-storage capacitors of the MOS device. C_{BS} and C_{BD} are the source-to-bulk and drain-to-bulk capacitors discussed above. The following discussion represents a heuristic development of a model for the large-signal charge-storage capacitors.

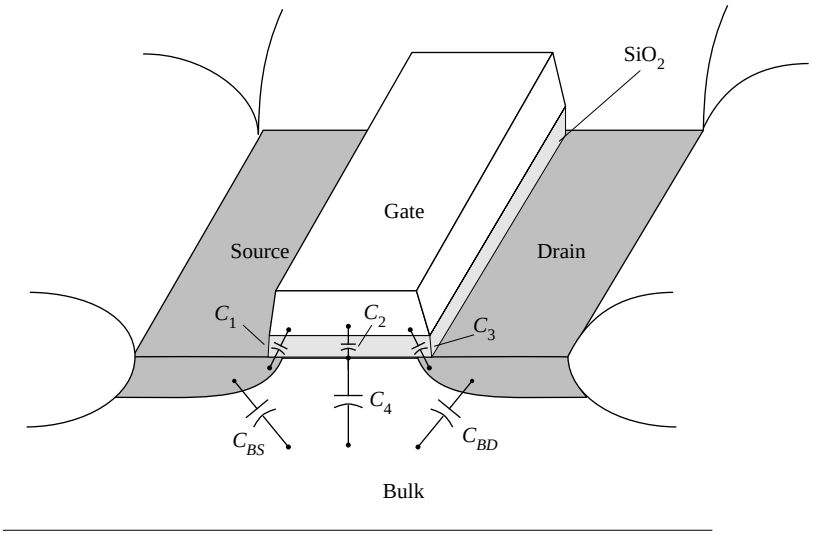


Figure 3.2-4 Large-signal, charge-storage capacitors of the MOS device.

Table 3.2-1 Capacitance Values and Coefficients for the MOS Model.

Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

Based on an oxide thickness of 140 Å or Cox=24.7×10^{-4} F/m^2.

C_1 and C_3 are overlap capacitances and are due to an overlap of two conducting surfaces separated by a dielectric. The overlapping capacitors are shown in more detail in Fig. 3.2-5. The amount of overlap is designated as LD. This overlap is due to the lateral diffusion of the source and drain underneath the polysilicon gate. For example, a 0.8 μm CMOS process might have a lateral diffusion component, LD, of approximately 16 nm. The overlap capacitances can be approximated as

$$C_1 = C_3 \cong (\text{LD})(W_{\text{eff}})C_{ox} = (\text{CGXO})W_{\text{eff}} \tag{7}$$

where W_{eff} is the effective channel width and CGXO ($X = S$ or D) is the overlap capacitance in F/m for the gate-source or gate-drain overlap. The difference between the mask W and actual W is due to the encroachment of the field oxide under the silicon nitride. Table 3.2-1 gives a value for CGSO and CGDO based on a device with an oxide thickness of 140 Å. A third overlap capacitance that can be significant is the overlap between the gate and the bulk. Fig. 3.2-6 shows this overlap capacitor (C_5) in more detail. This is the capacitance that occurs between the gate and bulk at the edges of the channel and is a function of the effective length of the channel, L_{eff}. Table 3.2-1 gives a typical value for CGBO for a device based on an oxide thickness of 140 Å.

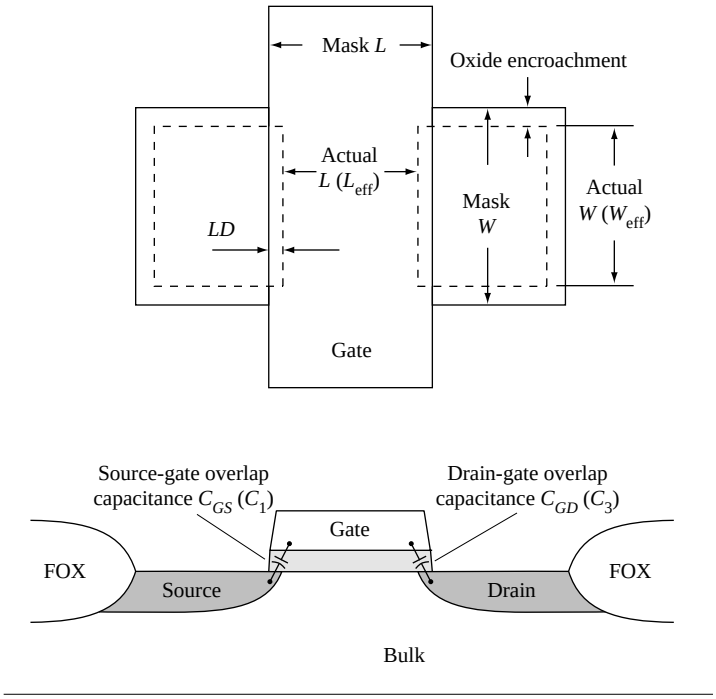


Figure 3.2-5 Overlap capacitances of an MOS transistor. (a) Top view showing the overlap between the source or drain and the gate. (b) Side view.

The channel of Fig. 3.2-4 is shown for the saturated state and would extend completely to the drain if the MOS device were in the nonsaturated state. C_2 is the gate-to-channel capacitance and is given as

$$C_2 = W_{\text{eff}}(L - 2\text{LD})C_{ox} = W_{\text{eff}}(L_{\text{eff}})C_{ox} \tag{8}$$

The term L_{eff} is the effective channel length resulting from the mask-defined length being reduced by the amount of lateral diffusion (note that up until now, the symbols L and W were used to refer to "effective" dimensions whereas now these have been changed for added clarification). C_4 is the channel-to-bulk capacitance which is a depletion capacitance that will vary with voltage like C_{BS} or C_{BD}.

It is of interest to examine C_{GB}, C_{GS}, and C_{GD} as v_{DS} is held constant and v_{GS} is increased from zero. To understand the results, one can imagine following a vertical line on Fig. 3.1-3 at say, $v_{DS} = 0.5(V_{GS0} - V_T)$, as v_{GS} increases from zero. The MOS device will first be off until v_{GS} reaches V_T. Next, it will be in the saturated region until v_{GS} becomes equal to $v_{DS}(\text{sat}) + V_T$. Finally, the MOS device will be in the nonsaturated region. The approximate variation of C_{GB}, C_{GS}, and C_{GD} under these conditions is shown in Fig. 3.2-7. In cutoff, there is no channel and C_{GB} is approximately equal to $C_2 + 2C_5$. As v_{GS} approaches V_T from the off region, a thin depletion layer is formed, creating a large value of C_4. Since C_4 is in series with C_2, little effect is observed. As v_{GS} increases, this depletion region widens, causing C_4 to decrease and reducing C_{GB}. When $v_{GS} = V_T$, an inversion layer is formed which prevents further decreases of C_4 (and thus C_{GB}).

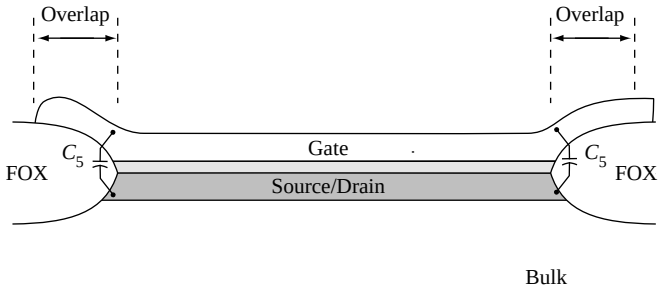


Figure 3.2-6 Gate-bulk overlap capacitances.

C_1, C_2, and C_3 constitute C_{GS} and C_{GD}. The problem is how to allocate C_2 to C_{GS} and C_{GD}. The approach used is to assume in saturation that approximately 2/3 of C_2 belongs to C_{GS} and none to C_{GD}. This is, of course, an approximation. However, it has been found to give reasonably good results. Fig. 3.2-7 shows how C_{GS} and C_{GD} change values in going from the off to the saturation region. Finally, when v_{GS} is greater than $v_{DS} + V_T$, the MOS device enters the nonsaturated region. In this case, the channel extends from the drain to the source and C_2 is simply divided evenly between C_{GD} and C_{GS} as shown in Fig. 3.2-7.

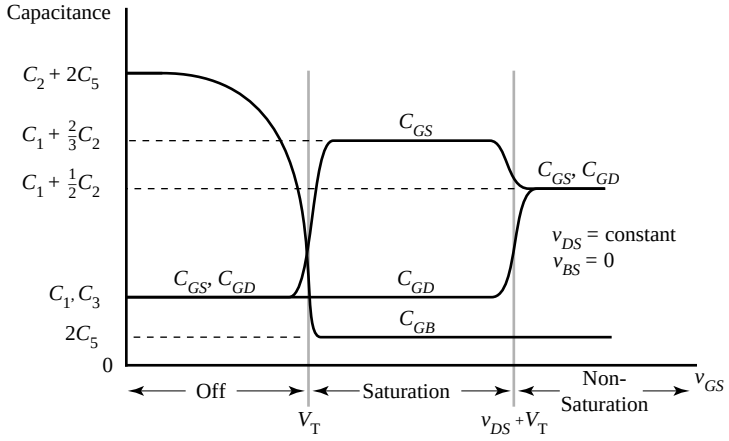


Figure 3.2-7 Voltage dependence of C_{GS}, C_{GD}, and C_{GB} as a function of V_{GS} with V_{DS} constang and $V_{BS} = 0$.

As a consequence of the above considerations, we shall use the following formulas for the charge-storage capacitances of the MOS device in the indicated regions.

Off

$$C_{GB} = C_2 + 2C_5 = C_{ox}(W_{\text{eff}})(L_{\text{eff}}) + 2\text{CGBO}(L_{\text{eff}}) \tag{9a}$$

$$C_{GS} = C_1 \cong C_{ox}(\text{LD})(W_{\text{eff}}) = \text{CGSO}(W_{\text{eff}}) \tag{9b}$$

$$C_{GD} = C_3 \cong C_{ox}(\text{LD})(W_{\text{eff}}) = \text{CGDO}(W_{\text{eff}}) \tag{9c}$$

Saturation

$$C_{GB} = 2C_5 = \text{CGBO}\,(L_{\text{eff}}) \tag{10a}$$

$$C_{GS} = C_1 + (2/3)C_2 = C_{ox}(\text{LD} + 0.67L_{\text{eff}})(W_{\text{eff}})$$

$$= \text{CGSO}(W_{\text{eff}}) + 0.67C_{ox}(W_{\text{eff}})(L_{\text{eff}}) \tag{10b}$$

$$C_{GD} = C_3 \cong C_{ox}(\text{LD})(W_{\text{eff}}) = \text{CGDO}(W_{\text{eff}}) \tag{10c}$$

Nonsaturated

$$C_{GB} = 2C_5 = \text{CGBO}\,(L_{\text{eff}}) \tag{11a}$$

$$C_{GS} = C_1 + 0.5C_2 = C_{ox}(\text{LD} + 0.5L_{\text{eff}})(W_{\text{eff}})$$

$$= (\text{CGSO} + 0.5C_{ox}L_{\text{eff}})W_{\text{eff}} \tag{11b}$$

$$C_{GD} = C_3 + 0.5C_2 = C_{ox}(\text{LD} + 0.5L_{\text{eff}})(W_{\text{eff}})$$

$$= (\text{CGDO} + 0.5C_{ox}L_{\text{eff}})W_{\text{eff}} \tag{11c}$$

Equations which provide a smooth transition between the three regions can be found in the literature [5].

Other capacitor parasitics associated with transistors are due to interconnect to the transistor, e.g., polysilicon over field (substrate). This type of capacitance typically constitutes the major portion of C_{GB} in the nonsaturated and saturated regions, thus are very important and should be considered in the design of CMOS circuits.

Another important aspect of modeling the CMOS device is noise. The existence of noise is due to the fact that electrical charge is not continuous but is carried in discrete amounts equal to the charge of an electron. In electronic circuits, noise manifests itself by representing a lower limit below which electrical signals cannot be amplified without significant deterioration in the quality of the signal. Noise can be modeled by a current source connected in parallel with i_D of Fig. 3.2-1. This current source represents two sources of noise, called thermal noise and flicker noise [6,7]. These sources of noise were discussed in Sec. 2.5. The mean-square current-noise source is defined as

$$\overline{i}_N^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{(KF)I_D}{f\,C_{ox}\,L^2}\right]\Delta f \tag{12}$$

where

Δf = a small bandwidth (typically 1 Hz) at a frequency f

$\eta = g_{mbs}/g_m$ (see Eq. (8) of Section 3.3)

k = Boltzmann's constant

T = temperature (K)

g_m = small-signal transconductance from gate to channel (see Eq. (6)

of Section 3.3)

KF = flicker-noise coefficient (F·A)

f = frequency (Hz)

KF has a typical value of 10^{-28} (F·A). Both sources of noise are process dependent and the values are usually different for enhancement and depletion mode FETs.

The mean-square current noise can be reflected to the gate of the MOS device by dividing Eq. (12) by g_m^2, giving

$$\overline{v}_N^2 = \frac{\overline{i}_N^2}{g_m^2} = \left[\frac{8kT(1+\eta)}{3\,g_m} + \frac{\text{KF}}{2f\,C_{ox}\,WLK'}\right]\Delta f \tag{13}$$

The equivalent input-mean-square voltage-noise form of Eq. (13) will be useful for analyzing the noise performance of CMOS circuits in later chapters.

The experimental noise characteristics of n-channel and p-channel devices are shown in Figures 3.2-8(a) and 3.2-8(b). These devices were fabricated using a sub-micron, silicon-gate, n-well, CMOS process. The data in Figs. 3.2-8(a) and 3.2-8(b) are typical for MOS devices and show that the $1/f$ noise is the dominant source of noise for frequencies below 100 kHz (at the given bias conditions)[i]. Consequently, in many practical cases, the equivalent input-mean-square voltage noise of Eq. (13) is simplified to

$$\overline{v}_{eq}^2 = \left[\frac{\text{KF}}{2f\,C_{ox}\,WLK'}\right]\Delta f \tag{14}$$

or in terms of the input-voltage-noise spectral density we can rewrite Eq. (14) as

$$\overline{e}_{eq}^2 = \frac{\overline{v}_{eq}^2}{\Delta f} = \frac{\text{KF}}{2f\,C_{ox}\,WLK'} = \frac{B}{f\,WL} \tag{15}$$

where B is a constant for a n-channel or p-channel device of a given process. The right-hand expression of Eq. (15) will be important in optimizing the design with respect to noise performance.

[i] If the bias current is reduced, the thermal noise floor increases, thus moving the 1/f noise corner to a lower frequecy. Therefore, the 1/f noise corner is a function of the thermal noise floor.

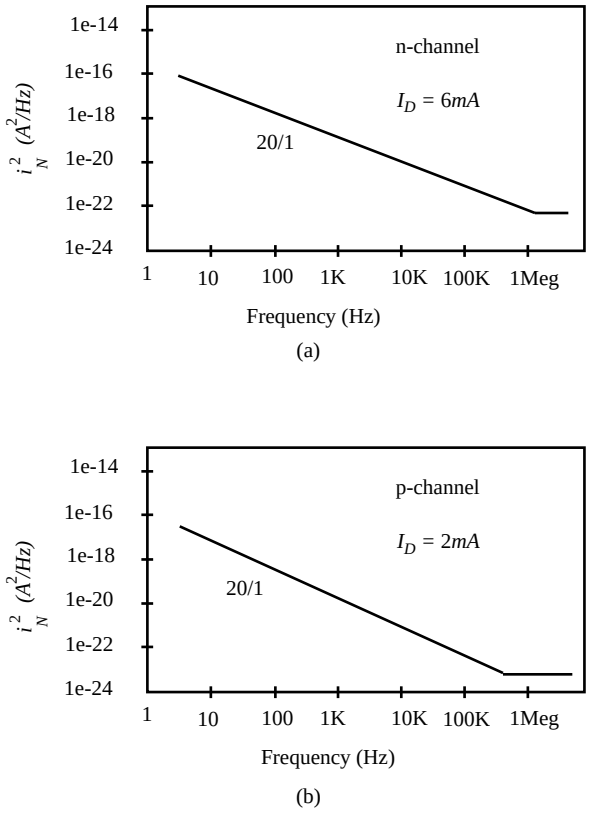


Figure 3.2-8 Drain-current noise for a (a) n-channel and (b) p-channel MOSFET measured on a silicon-gate submicron process.

3.3 Small-Signal Model for the MOS Transistor

Up to this point, we have been considering the large-signal model of the MOS transistor shown in Fig. 3.2-1. However, after the large-signal model has been used to find the dc conditions, the small-signal model becomes important. The small-signal model is a linear model which helps to simplify calculations. It is only valid over voltage or current regions where the large-signal voltage and currents can be adequately represented by a straight line.

Fig. 3.3-1 shows a linearized small-signal model for the MOS transistor. The parameters of the small-signal model will be designated by lower case subscripts. The various parameters of this small-signal model are all related to the large-signal model parameters and dc variables. The normal relationship between these two models assumes that the small-signal parameters are defined in terms of the ratio of small perturbations of the large-signal variables or as the partial differentiation of one large-signal variable with respect to another.

The conductances g_{bd} and g_{bs} are the equivalent conductances of the bulk-to-drain and bulk-to-source junctions. Since these junctions are normally reverse biased, the conductances are very small. They are defined as

$$g_{bd} = \frac{\partial I_{BD}}{\partial V_{BD}} \text{(at the quiescent point)} \cong 0 \qquad (1)$$

and

$$g_{bs} = \frac{\partial I_{BS}}{\partial V_{BS}} \text{(at the quiescent point)} \cong 0 \tag{2}$$

The channel conductances, g_m, g_{mbs}, and g_{ds} are defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{(at the quiescent point)} \tag{3}$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} \text{(at the quiescent point)} \tag{4}$$

and

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \text{(at the quiescent point)} \tag{5}$$

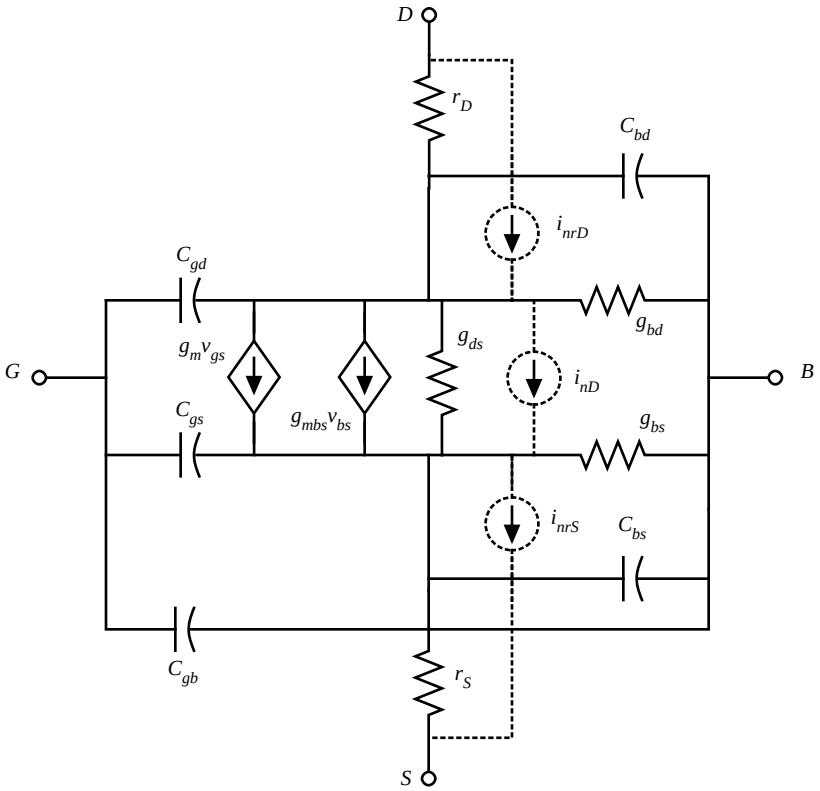


Figure 3.3-1 Small-signal model of the MOS transistor.

The values of these small signal parameters depend on which region the quiescent point occurs in. For example, in the saturated region g_m can be found from Eq. (13) of Section 3.1 as

$$g_m = \sqrt{(2K'W/L)|I_D|(1 + \lambda V_{DS})} \cong \sqrt{(2K'W/L)|I_D|} \tag{6}$$

which emphasizes the dependence of the small-signal parameters upon the large-signal operating conditions. The small-signal channel transconductance due to v_{SB} is found by rewriting Eq. (4) as

$$g_{mbs} = \frac{-\partial I_D}{\partial V_{SB}} = -\left(\frac{\partial I_D}{\partial V_T}\right)\left(\frac{\partial V_T}{\partial V_{SB}}\right) \tag{7}$$

Using Eq. (2) of Section 3.1 and noting that $\frac{\partial I_D}{\partial V_T} = \frac{-\partial I_D}{\partial V_{GS}}$, we get

$$g_{mbs} = g_m \frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}} = \eta\, g_m \tag{8}$$

This transconductance will become important in our small-signal analysis of the MOS transistor when the ac value of the source-bulk potential v_{sb} is not zero.

The small-signal channel conductance, g_{ds} (g_o), is given as

$$g_{ds} = g_o = \frac{I_D\,\lambda}{1 + \lambda\, V_{DS}} \cong I_D\,\lambda \tag{9}$$

The channel conductance will be dependent upon L through λ which is inversely proportional to L. We have assumed the MOS transistor is in saturation for the results given by Eqs. (6), (8), and (9).

The important dependence of the small-signal parameters upon the large-signal model parameters and dc voltages and currents is illustrated in Table 3.3-1. In this Table we see that the three small-signal model parameters of g_m, g_{mbs}, and g_{ds} have several alternate forms. An example of the typical values of the small-signal model parameters follows.

Example 3.3-1 Typical Values of Small Signal Model Parameters

Find the values of g_m, g_{mbs}, and g_{ds} using the large signal model parameters in Table 3.1-2 for both an n-channel and p-channel device if the dc value of the magnitude of the drain current is 50 μA and the magnitude of the dc value of the source-bulk voltage is 2 V. Assume that the W/L ratio is 1 μm/1 μm.

Using the values of Table 3.1-2 and Eqs. (6), (8), and (9) gives g_m = 105 μA/V, g_{mbs} = 12.8 μA/V, and $g_{ds} \cong$ 2.0 μA/V for the n-channel device and g_m = 70.7 μA/V, g_{mbs} = 12.0 μA/V, and $g_{ds} \cong$ 2.5 μA/V for the p-channel device.

Table 3.3-1 Relationships of the Small Signal Model Parameters upon the DC Values of Voltage and Current in the Saturation Region.

Small Signal Model Parameters	DC Current	DC Current and Voltage	DC Voltage
g_m	$\cong (2K' I_D W/L)^{1/2}$	—	$\cong \frac{K' W}{L}(V_{GS} - V_T)$
g_{mbs}	—	$\frac{\gamma (2I_D\beta)^{1/2}}{2(2\lvert\phi_F\rvert + V_{SB})^{1/2}}$	$\frac{\gamma [\ \beta (V_{GS} - V_T)\ ]^{1/2}}{2(2\lvert\phi_F\rvert + V_{SB})^{1/2}}$
g_{ds}	$\cong \lambda I_D$	—	—

Although the MOS devices are not often used in the nonsaturation region in analog circuit design, the relationships of the small-signal model parameters in the nonsaturation region are given as

$$g_m = \frac{\partial I_d}{\partial V_{GS}} = \beta V_{DS}(1 + \lambda V_{DS}) \cong \beta V_{DS} \tag{10}$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\beta\gamma V_{DS}}{2(2|\phi_F| + V_{SB})^{1/2}} \tag{11}$$

and

$$g_{ds} = \beta(V_{GS} - V_T - V_{DS})(1 + \lambda V_{DS}) + \frac{I_D\lambda}{1 + \lambda V_{DS}}$$

$$\cong \beta(V_{GS} - V_T - V_{DS}) \tag{12}$$

Table 3.3-2 summarizes the dependence of the small-signal model parameters on the large-signal model parameters and dc voltages and currents for the nonsaturated region. The typical values of the small-signal model parameters for the nonsaturated region are illustrated in the following example.

Table 3.3-2 Relationships of the Small-Signal Model Parameters upon the DC Values of Voltage and Current in the Nonsaturation Region.

Small Signal Model Parameters	DC Voltage and/or Current Dependence
g_m	$\cong \beta V_{DS}$
g_{mbs}	$\frac{\beta\gamma V_{DS}}{2(2\lvert\phi_F\rvert + V_{SB})^{1/2}}$
g_{ds}	$\cong \beta(V_{GS} - V_T - V_{DS})$

Example 3.3-2 Typical Values of the Small-Signal Model Parameters in the Nonsaturated Region

Find the values of the small-signal model parameters in the nonsaturation region for an n-channel and p-channel transistor if $V_{GS} = 5$ V, $V_{DS} = 1$ V, and $|V_{BS}| = 2$ V. Assume that the W/L ratios of both transistors is 1 μm/1 μm. Also assume that the value for K' in

the nonsaturation region is that same as that for the saturation (generally a poor assumption).

First it is necessary to calculate the threshold voltage of each transistor using Eq. (2) of Sec. 3.1. The results are a V_T of 1.02 V for the n-channel and −1.14 V for the p-channel. This gives a dc current of 383 μA and 168 μA, respectively. Using Eqs. (10), (11), and (12), we get g_m = 110 μA/V, g_{mbs} = 46.6 μA/V, and r_{ds} = 3.05 KΩ for the n-channel transistor and g_m = 50 μA/V, g_{mbs} = 28.6 μA/V, and r_{ds} = 6.99 KΩ for the p-channel transistor.

The values of r_d and r_s are assumed to be the same as r_D and r_S of Fig. 3.2-1. Likewise, for small-signal conditions C_{gs}, C_{gd}, C_{gb}, C_{bd}, and C_{bs} are assumed to be the same as C_{GS}, C_{GD}, C_{GB}, C_{BD}, and C_{BS}, respectively.

If the noise of the MOS transistor is to be modeled, then three additional current sources are added to Fig. 3.3-1 as indicated by the dashed lines. The values of the mean-square noise-current sources are given as

$$\overline{i}^2_{nrD} = \left(\frac{4kT}{r_D}\right)\Delta f \quad (\text{A}^2) \tag{13}$$

$$\overline{i}^2_{nrS} = \left(\frac{4kT}{r_S}\right)\Delta f \quad (\text{A}^2) \tag{14}$$

and

$$\overline{i}^2_{nD} = \left[\frac{8kT\,g_m(1+\eta)}{3} + \frac{(\text{KF})I_D}{f\,C_{ox}\,L^2}\right]\Delta f \quad (\text{A}^2) \tag{15}$$

The various parameters for these equations have been previously defined. With the noise modeling capability, the small-signal model of Fig. 3.3-1 is a very general model.

It will be important to be familiar with the small-signal model for the saturation region developed in this section. This model, along with the circuit simplification techniques given in Appendix A, will be the key element in analyzing the circuits in the following chapters.

3.4 Computer Simulation Models

The large-signal model of the MOS device previously discussed is simple to use for hand calculations but neglects many important second-order effects. While a simple model for hand calcualtion and design intuition is critical, a more accurate model is required for computer simulation. There are many model choices available for the designer when choosing a device model to use for computer simulation. At one time, HSPICE[i] supported 43 different mosfet models [25] (many of which were company proprietary) while SmartSpice publishes support for 14 [24]. Which model is the right one to use? In the fabless semiconductor environment, the user must use the model provided by the wafer foundry. In companies where the foundry is captive (i.e., the company owns their own wafer fabrication facility) a modeling group provides the model

[i] HSPICE is now owned by Avant! Inc. and has been renamed to Star-Hspice

to circuit designers. It is seldom that the designer takes it upon himself to choose a model and perform parameter extraction to get the terms for the model chosen.

The SPICE Level 3 dc model will be covered in some detail because it is a relatively straightforward extension of the Level 2 model. The BSIM3v3 model will be introduced but the detailed equations will not be presented because of the volume of equations required to describe it—there are other good texts that deal with the subject of modeling exclusively [28,29], and there is little additional design intuition derived from covering the details.

Models developed for computer simulation have improved over the years but no model has yet been developed that, with a single set of parameters, covers device operation for all possible geometries. Therefore, many SPICE simulators offer a feature called "model binning." Parameters are derived for transistors of different geometry (Ws and Ls) and the simulator determines which set of parameters to use based upon the particular W and L called out in the device instantiation line in the circuit description. The circuit designer need only be aware of this since the binning is done by the model provider.

SPICE Level 3 Model

The large-signal model of the MOS device previously discussed is simple to use for hand calculations but neglects many important second-order effects. Most of these second-order effects are due to narrow or short channel dimensions (less than about 3μm). In this section, we will consider a more complex model that is suitable for computer-based analysis (circuit simulation, i.e., SPICE simulation). In particular, the SPICE Level 3 model will be covered. This model is typically good for MOS technologies down to about 0.8 μm. We will also consider the effects of temperature upon the parameters of the MOS large signal model.

We first consider second-order effects due to small geometries. When v_{GS} is greater than V_T, the drain current for a small device can be given as [25]

Drain Current

$$i_{DS} = \text{BETA}\left[v_{GS} - V_T - \left(\frac{1+f_b}{2}\right)v_{DE}\right]\cdot v_{DE} \tag{1}$$

$$\text{BETA} = \text{KP}\,\frac{W_{\text{eff}}}{L_{\text{eff}}} = \mu_{\text{eff}}\text{COX}\,\frac{W_{\text{eff}}}{L_{\text{eff}}} \tag{2}$$

$$L_{\text{eff}} = L - 2(\text{LD}) \tag{3}$$

$$W_{\text{eff}} = W - 2(\text{WD}) \tag{4}$$

$$v_{DE} = \min(v_{DS}\,,\, v_{DS}\,(\text{sat})) \tag{5}$$

$$f_b = f_n + \frac{\text{GAMMA} \cdot f_s}{4(\text{PHI} + v_{SB})^{1/2}} \tag{6}$$

Note that PHI is the SPICE model term for the quantity $2\phi_f$. Also be aware that PHI is always positive in SPICE regardless of the transistor type (p- or n-channel). In this text, the term, PHI, will always be positive while the term, $2\phi_f$, will have a polarity determined by the transistor type as shown in Table 2.3-1.

$$f_n = \frac{\text{DELTA}}{W_{\text{eff}}} \frac{\pi \varepsilon_{\text{si}}}{2 \cdot \text{COX}} \tag{7}$$

$$f_s = 1 - \frac{x_j}{L_{\text{eff}}} \left\{ \frac{\text{LD} + wc}{x_j} \left[1 - \left(\frac{wp}{x_j + wp} \right)^2 \right]^{1/2} - \frac{\text{LD}}{x_j} \right\} \tag{8}$$

$$wp = xd\,(\text{PHI} + v_{SB})^{1/2} \tag{9}$$

$$xd = \left(\frac{2 \cdot \varepsilon_{si}}{q \cdot \text{NSUB}} \right)^{1/2} \tag{10}$$

$$wc = x_j \left[k_1 + k_2 \left(\frac{wp}{x_j} \right) - k_3 \left(\frac{wp}{x_j} \right)^2 \right] \tag{11}$$

$k_1 = 0.0631353$, $k_2 = 0.08013292$, $k_3 = 0.01110777$

Threshold Voltage

$$V_T = V_{bi} - \left(\frac{\text{ETA} \cdot 8.15^{-22}}{C_{\text{ox}} L_{\text{eff}}^3} \right) v_{DS} + \text{GAMMA} \cdot f_s (\text{PHI} + v_{SB})^{1/2} + f_n (\text{PHI} + v_{SB}) \tag{12}$$

$$v_{bi} = \text{v}_{fb} + \text{PHI} \tag{13}$$

or

$$v_{bi} = \text{VTO} - \text{GAMMA} \cdot \sqrt{\text{PHI}} \tag{14}$$

Saturation Voltage

$$v_{sat} = \frac{v_{gs} - V_T}{1 + f_b} \tag{15}$$

$$v_{DS}(\text{sat}) = v_{sat} + v_C - \left(v_{\text{sat}}^2 + v_C^2\right)^{1/2} \tag{16}$$

$$v_C = \frac{\text{VMAX} \cdot L_{\text{eff}}}{\mu_{\text{s}}} \tag{17}$$

If VMAX is not given, then $v_{DS}(\text{sat}) = v_{sat}$

Effective Mobility

$$\mu_s = \frac{\text{U0}}{1 + \text{THETA}\,(v_{GS} - V_T)} \text{ when VMAX} = 0 \tag{18}$$

$$\mu_{\text{eff}} = \frac{\mu_s}{1 + \dfrac{v_{DE}}{v_C}} \text{ when VMAX} > 0\text{; otherwise } \mu_{\text{eff}} = \mu_S \tag{19}$$

Channel-Length Modulation

When VMAX = 0

$$\Delta L = xd\left[\text{KAPPA}\ \ (v_{DS} - v_{DS}(\text{sat}))\right]^{1/2} \tag{20}$$

when VMAX > 0

$$\Delta L = -\frac{ep \cdot xd^{\,2}}{2} + \left[\left(\frac{ep \cdot xd^{\,2}}{2}\right)^2 + \text{KAPPA} \cdot xd^{\,2} \cdot (v_{DS} - v_{DS}(\text{sat}))\right]^{1/2} \tag{21}$$

where

$$ep = \frac{v_C\,(v_C + v_{DS}(\text{sat}))}{L_{\text{eff}}\, v_{DS}\,(\text{sat})} \tag{22}$$

$$i_{DS} = \frac{i_{DS}}{1 - \Delta L} \tag{21}$$

Table 3.4-1 Typical Model Parameters Suitable for SPICE Simulations Using Level-3 Model (Extended Model). These Values Are Based upon a 0.8μm Si-Gate Bulk CMOS n-Well Process and Include Capacitance Parameters from Table 3.2-1.

Parameter Symbol	Parameter Description	Typical Parameter Value N-Channel	P-Channel	Units
VTO	Threshold	0.7 ± 0.15	-0.7 ± 0.15	V
UO	mobility	660	210	$cm^2/V\text{-}s$
DELTA	Narrow-width threshold adjust factor	2.4	1.25	—
ETA	Static-feedback threshold adjust factor	0.1	0.1	—
KAPPA	Saturation field factor in channel-length modulation	0.15	2.5	1/V
THETA	Mobility degradation factor	0.1	0.1	1/V
NSUB	Substrate doping	3×10^{16}	6×10^{16}	cm^{-3}
TOX	Oxide thickness	140	140	Å
XJ	Mettallurgical junction depth	0.2	0.2	μm
WD	Delta width			μm
LD	Lateral diffusion	0.016	0.015	μm
NFS	Parameter for weak inversion modeling	7×10^{11}	6×10^{11}	cm^{-2}
CGSO		220×10^{-12}	220×10^{-12}	F/m
CGDO		220×10^{-12}	220×10^{-12}	F/m
CGBO		700×10^{-12}	700×10^{-12}	F/m
CJ		770×10^{-6}	560×10^{-6}	F/m^2
CJSW		380×10^{-12}	350×10^{-12}	F/m
MJ		0.5	0.5	
MJSW		0.38	0.35	

The temperature-dependent variables in the models developed so far include the: Fermi potential, PHI, EG, bulk junction potential of the source-bulk and drain-bulk junctions, PB, the reverse currents of the pn junctions, I_S, and the dependence of mobility upon temperature. The temperature dependence of most of these variables is found in the equations given previously or from well-known expressions. The dependence of mobility upon temperature is given as

$$\text{UO}(T) = \text{UO}(T_0)\left(\frac{T}{T_0}\right)^{\text{BEX}} \tag{15}$$

where BEX is the temperature exponent for mobility and is typically -1.5.

$$v_{therm}(T) = \frac{KT}{q} \tag{16}$$

$$\mathrm{EG}(T) = 1.16 - 7.02 \cdot 10^{-4} \cdot \left[\frac{T^2}{T + 1108.0}\right] \tag{17}$$

$$\mathrm{PHI}(T) = \mathrm{PHI}(T_0) \cdot \left(\frac{T}{T_0}\right) - v_{therm}(T)\left[3 \cdot \ln\left(\frac{T}{T_0}\right) + \frac{\mathrm{EG}(T_0)}{v_{therm}(T_0)} - \frac{\mathrm{EG}(T)}{v_{therm}(T)}\right] \tag{18}$$

$$v_{bi}(T) = v_{bi}(T_0) + \frac{\mathrm{PHI}(T) - \mathrm{PHI}(T_0)}{2} + \frac{\mathrm{EG}(T_0) - \mathrm{EG}(T)}{2} \tag{19}$$

$$\mathrm{VT0}(T) = v_{bi}(T) + \mathrm{GAMMA}\left[\sqrt{\mathrm{PHI}(T)}\right] \tag{20}$$

$$\mathrm{PHI}(T) = 2 \cdot v_{therm} \ln\left(\frac{\mathrm{NSUB}}{n_i(T)}\right) \tag{21}$$

$$n_{i(T)} = 1.45 \cdot 10^{16} \cdot \left(\frac{T}{T_0}\right)^{3/2} \cdot \exp\left[\mathrm{EG} \cdot \left(\frac{T}{T_0} - 1\right) \cdot \left(\frac{1}{2 \cdot v_{therm}(T_0)}\right)\right] \tag{22}$$

For drain and source junction diodes, the following relationships apply.

$$\mathrm{PB}(T) = \mathrm{PB} \cdot \left(\frac{T}{T_0}\right) - v_{therm}(T)\left[3 \cdot \ln\left(\frac{T}{T_0}\right) + \frac{\mathrm{EG}(T_0)}{v_{therm}(T_0)} - \frac{\mathrm{EG}(T)}{v_{therm}(T)}\right] \tag{23}$$

and

$$I_S(T) = \frac{I_S(T_0)}{\mathrm{N}} \cdot exp\left[\frac{\mathrm{EG}(T_0)}{v_{therm}(T_0)} - \frac{\mathrm{EG}(T)}{v_{therm}(T)} + 3 \cdot \ln\left(\frac{T}{T_0}\right)\right] \tag{24}$$

where N is diode emission coefficient.

The nominal temperature, T_0, is 300 K.

An alternate form of the temperature dependence of the MOS model can be found elsewhere [12].

BSIM 3v3 Model

MOS transistor models introduced thus far in this chapter have been used successfully when applied to 0.8 μm technologies and above. As geometries shrink below 0.8 μm, better models are required. Researchers in the Electrical Engineering and Computer Sciences department at The University of California at Berkeley have been leaders in the developement of SPICE and the models used in it. In 1984 they introduced the BSIM1 model [27] to address the need for a better submicron MOS transistor model. The BSIM1 model model approached the modeling problem as a multi-parameter curve-fitting exercise. The model contained 60 parameters covering the dc performance of the

MOS transistor. There was some relationship to device physics, but in a large part, it was a non-phycal model. Later, in 1991, UC Berkeley released the BSIM2 model that improved performance related to the modeling of output resistance changes due to hot-electron effects, source/drain parasitic resistance, and inversion-layer capacitance. This model contained 99 dc parameters, making it more unwieldy than the 60-parameter (dc parameters) BSIM1 model. In 1994, U.C. Berkeley introduced the BSIM3 model (version 2) which, unlike the earlier BSIM models, returned to a more device-physic based modeling approach. The model is simpler to use and only has 40 dc parameters. Moreover, the BSIM3 provides good performance when applied to analog as well as digital circuit simulation. In its third version, BSIM3v3 [26], it has become the industry standard MOS transistor model.

The BSIM3 model addresses the following important effects seen in deep-submicron MOSFET operation:

- Threshold voltage reduction
- Mobility degradation do to a vertical field
- Velocity saturation effects
- Drain-induced barrier lowering (DIBL)
- Channel length modulation
- Subthreshold (weak inversion) conduction
- Parasitic resistance in the source and drain
- Hot-electron effects on output resistance

The plot shown in Fig. 3.4-2 shows a comparison of a 20/0.8 device using the Level 1, Level 3, and the BSIM3v3 models. The model parameters were adjusted to provide similar characterists (given the limitations of each model). Assuming that the BSIM3v3 model closely approximates actual transistor performance, this figure indicates that the Level 1 model is grossly in error, the Level 3 model shows a significant difference in modeling the transition from non-saturation to linear region.

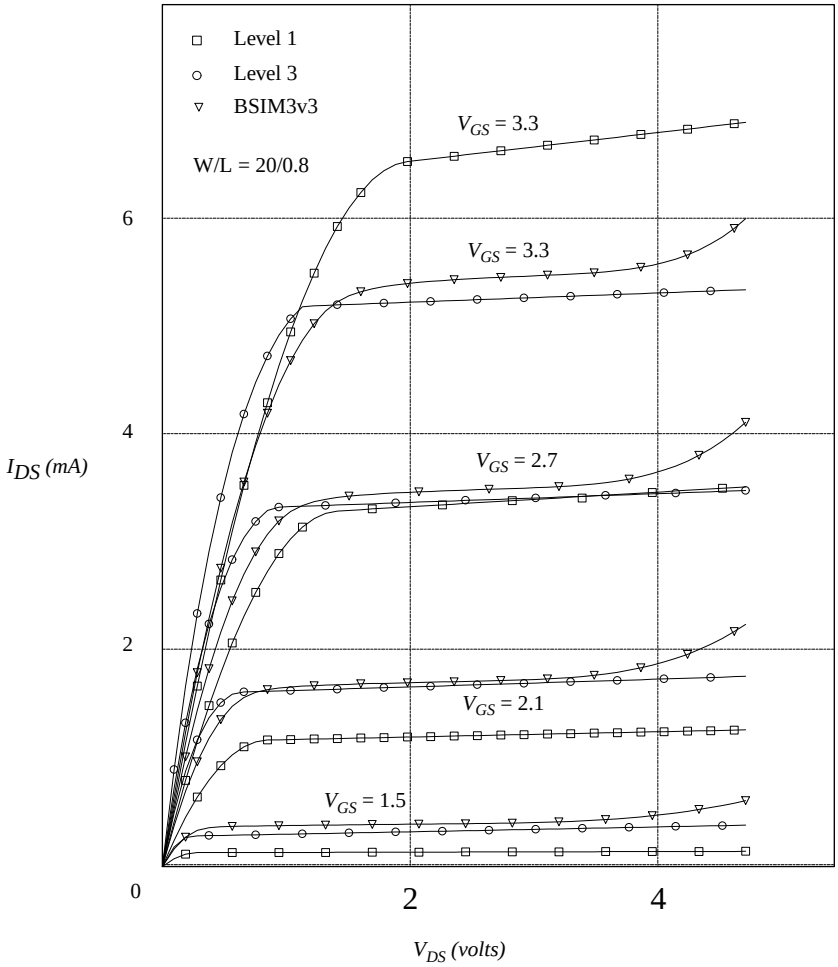


Figure 3.4-2 Simulation of MOSFET transconductance characteristic using Level=1, Level=3, and the BSIM3v3 models.

3.5 Subthreshold MOS Model

The models discussed in previous sections predict that no current will flow in a device when the gate-source voltage is at or below the threshold voltage. In reality, this is not the case. As v_{GS} approaches V_T, the $i_D - v_{GS}$ characteristics change from square-law to exponential. Whereas the region where v_{GS} is above the threshold is called the *strong inversion* region, the region below (actually, the transition between the two regions is not well defined as will be explained later) is called the *subthreshold,* or *weak inversion* region. This is illustrated in Fig. 3.5-1 where the transconductance characteristic a MOSFET in saturation is shown with the square root of current plotted as a function of the gate-source voltage. When the gate-source voltage reaches the value designated as v_{on} (this relates to the SPICE model formulation), the current changes from square-law to an exponential-law behavior. It is the objective of this section to present two models suitable for the subthreshold region. The first is the SPICE LEVEL 3 [25] model for computer simulation while the second is useful for hand calculations.

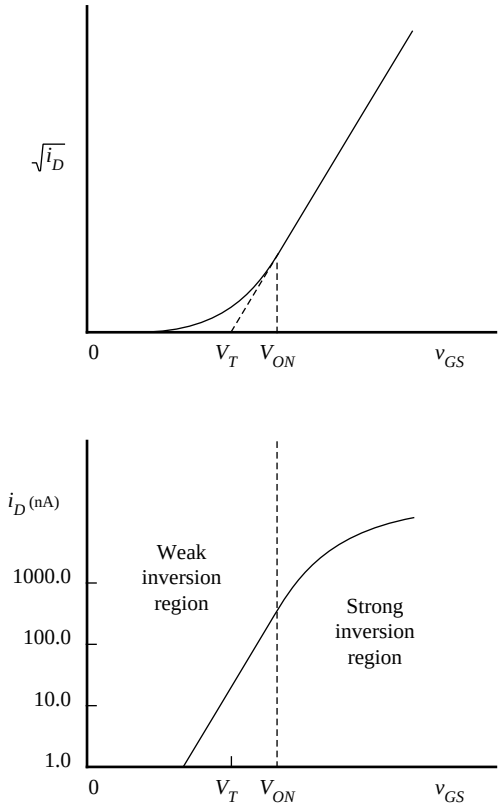


Figure 3.5-1 Weak-inversion characteristics of the MOS transistor as modeled by Eq. (4).

In the SPICE Level 3 model, the transition point from the region of strong inversion to the weak inversion characteristic of the MOS device is designated as v_{on} and is greater than V_T. v_{on} is given by

$$v_{on} = V_T + fast \tag{1}$$

where

$$fast = \frac{kT}{q}\left[1 + \frac{q \cdot NFS}{\text{COX}} + \frac{\text{GAMMA} \cdot f_s\,(\text{PHI} + v_{SB})^{1/2} + f_n\,(\text{PHI} + v_{SB})}{2(\text{PHI} + v_{SB})}\right] \tag{2}$$

NFS is a parameter used in the evaluation of v_{on} and can be extracted from measurements. The drain current in the weak inversion region, v_{GS} less than v_{on}, is given as

$$i_{DS} = i_{DS}\,(v_{on}, v_{DE}, v_{SB})\, e^{\left(\frac{v_{GS} - v_{on}}{fast}\right)} \tag{3}$$

where i_{DS} is given as (from Eq. (1), Sec. 3.4 with v_{GS} replaced with v_{on})

$$i_{DS} = \text{BETA}\left[v_{on} - V_T - \left(\frac{1+f_b}{2}\right)v_{DE}\right] \cdot v_{DE} \tag{4}$$

For hand calculations, a simple model describing weak-inversion operation is given as

$$i_D \cong \frac{W}{L} I_{DO} \exp\left(\frac{v_{GS}}{n(kT/q)}\right) \tag{5}$$

where term n is the subthreshold slope factor, and I_{DO} is a process-dependent parameter which is dependent also on v_{SB} and V_T. These two terms are best extracted from experimental data. Typically n is greater than 1 and less than 3 ($1 < n < 3$). The point at which a transistor enters the weak-inversion region can be approximated as

$$v_{gs} < V_T + n\frac{kT}{q} \tag{6}$$

Unfortunately, the model equations given here do not properly model the transistor as it makes the transition from strong to weak inversion. In reality, there is a transition region of operation between strong and weak inversion called the “moderate inversion” region [15]. This is illustrated in Fig. 3.5-2. A complete treatment of the operation of the transistor through this region is given in the literature [15,16].

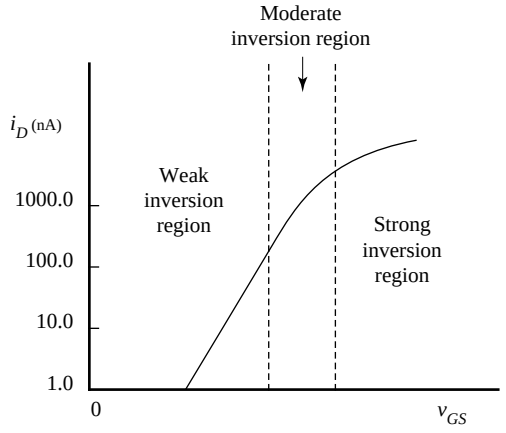


Figure 3.5-2 The three regions of operation of an MOS transistor.

It is important to consider the temperature behavior of the MOS device operating in the subthreshold region. As is the case for strong inversion, the temperature coefficient of the threshold voltage is negative in the subthreshold region. The variation of current due to temperature of a device operating in weak inversion is dominated by the negative temperature coefficient of the threshold voltage. Therefore, for a given gate-source voltage, subthreshold current increases as the temperature increases. This is illustrated in Fig. 3.5-3 [21].

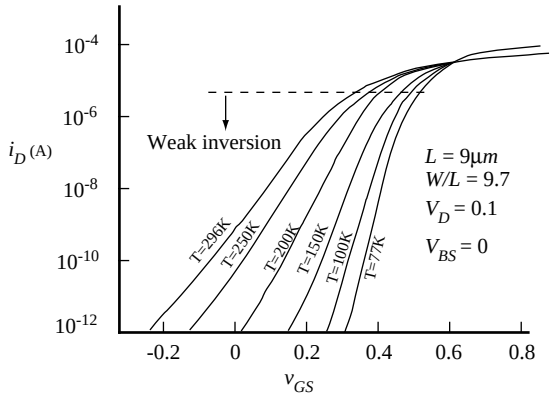


Figure 3.5-3 Transfer characteristics of a long-channel device as a function of temperature. (© IEEE)

Operation of the MOS device in the subthreshold region is very important when low-power circuits are desired. A whole class of CMOS circuits have been developed based on the weak-inversion operation characterized by the above model [17,18,19,20]. We will consider some of these circuits in later chapters.

3.6 SPICE Simulation of MOS Circuits

The objective of this section is to show how to use SPICE to verify the performance of an MOS circuit. It is assumed that the reader already has experience using SPICE to simulate circuits containing resistors, capacitors, sources, etc. This section will extend the readers knowledge to include the application of MOS transistors into SPICE simulations. The models used in this section are the Level 1 and Level 3 models.

In order to simulate MOS circuits in SPICE, two components of the SPICE simulation file are needed. They are *instance* declarations and model descriptions. Instance declarations are simply descriptions of MOS devices appearing in the circuit along with characteristics unique to each instance. A simple example which shows the minimum required terms for a transistor instance follows:

```
M1 3 6 7 0 NCH W=100U L=1U
```

Here, the first letter in the instance declaration, “M,” tells SPICE that the instance is an MOS transistor (just like “R” tells SPICE that an instance is a resistor). The “1” makes this instance unique (different from M2, M99, etc.) The four numbers following”M1” specify the nets (or nodes) to which the drain, gate, source, and substrate (bulk) are connected. These nets have a specific order as indicated below:

```
M<number>  <DRAIN>  <GATE>  <SOURCE>  <BULK> ...
```

Following the net numbers, is the model name governing the character of the particular instance. In the example given above, the model name is “NCH.” There must be a model description somewhere in the simulation file that describes the model “NCH.” The transistor width and length are specified for the instance by the “W=100U” and “L=1U” expressions. The default units for width and length are meters so the “U”

following the number 100 is a multiplier of 10^{-6}. [Recall that the following multipliers can be used in SPICE: M, U, N, P, F, for 10^{-3}, 10^{-6}, 10^{-9}, 10^{-12} , 10^{-15} , respectively.]

Additional information can be specified for each instance. Some of these are

Drain area and periphery (AD and PD)
Source area and periphery (AS and PS)
Drain and source resistance in squares (NRD and NRS)
Multiplier designating how many devices are in parallel (M)
Initial conditions (for initial transient analysis)

Drain and source area and periphery terms are used in calculating depletion capacitance and diode currents (remember, the drain and source are pn diodes to the bulk or well). The number of squares of resistance in the drain and source (NRD and NRS) are used to calculate the drain and source resistance for the transistor. The multiplier designator is very important and thus deserves extended discussion here.

In Sec 2.6 layout matching techniques were developed. One of the fundamental principles described was the "unit-matching" principle. This principle prescribes that when one device needs to be "M" times larger than another device, then the larger device should be made from "M" units of the smaller device. In the layout, the larger device would be drawn using "M" copies of the smaller device—all of them in parallel (i.e., all of the gates tied together, all of the drains tied together, and all of the sources tied together). In SPICE, one must account for the multiple components tied in parallel. One way to do this would be to instantiate the larger device by instantiating "M" of the smaller devices. A more convenient way to handle this is to use the multiplier parameter when the larger device is instantiated. Figure 3.6-1 illustrates two methods for implementing a 2X device (unit device implied). In Fig. 3.6-1(a) the correct way to instantiate the device in SPICE is

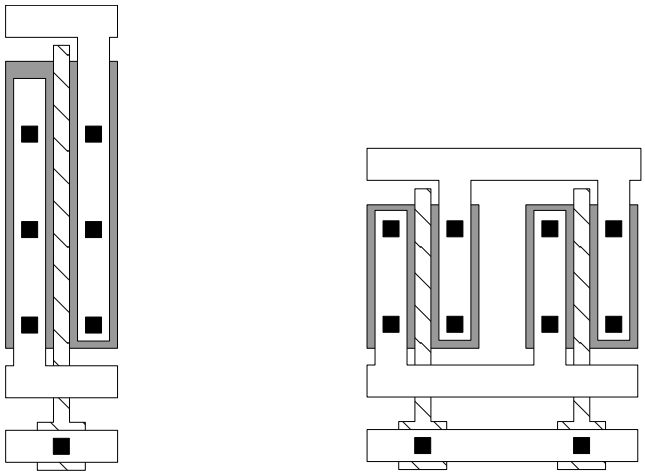
```
M1 3 2 1 0 NCH W=20U L=1U
```

whereas in Fig3.6-1(b) the correct SPICE instantiation is

```
M1 3 2 1 0 NCH W=10U L=1U M=2
```

Clearly, from the point of view of matching (again, it is implied that an attempt is made to achieve a 2 to 1 ratio), case (b) is the better choice and thus the instantiation with the multiplier is required. For the sake of completeness, it should be noted that the following pair of instantiations are equivalent to the use of the multiplier:

```
M1A 3 2 1 0 NCH W=10U L=1U
M1B 3 2 1 0 NCH W=10U L=1U
```



(a) (b)

Figure 3.6-1 (a)M1 3 2 1 0 NCH W=20U L=1U. (b) M1 3 2 1 0 NCH W=10U L=1U M=2.

Some SPICE simulators offer additional terms further describing an instance of a MOS transistor.

A SPICE simulation file for an MOS circuit is incomplete without a description of the model to be used to characterize the MOS transistors used in the circuit. A model is described by placing a line in the simulation file using the following format.

```
.MODEL <MODEL NAME> <MODEL TYPE> <MODEL PARAMETERS>
```

The model line must always begin with ".MODEL" and be followed by a model name such as "NCH" in our example. Following the model name is the model type. The appropriate choices for model type in MOS circuits is either "PMOS" or "NMOS." The final group of entries is model parameters. If no entries are provided, SPICE uses a default set of model parameters. Except for the crudest of simulations, you will always want to avoid the default parameters. Most of the time you should expect to get a model from the foundry where the wafers will be fabricated, or from the modeling group within your company. For times where it is desired to check hand calculations that were performed using the simple model (Level 1 model) it is useful to know the details of entering model information. An example model description line follows.

```
.MODEL NCH NMOS LEVEL=1 VTO=1 KP=50U GAMMA=0.5
+LAMBDA=0.01
```

In this example, the model name is "NCH" and the model type is "NMOS." The model parameters dictate that the LEVEL 1 model is used with VTO, KP, GAMMA, and LAMBDA specified. Note that the "+" is SPICE syntax for a continuation line.

The information on the model line is much more extensive and will be covered in this and the following paragraphs. The model line is preceded by a period to flag the program that this line is not a component. The model line identifies the model LEVEL (e.g., LEVEL=1) and provides the electrical and process parameters. If the user does not input the various parameters, default values are used. These default values are indicated in the user's guide for the version of SPICE being used (e.g., SmartSpice). The LEVEL 1 model parameters were covered in Sec. 3.1 and are: the zero-bias threshold voltage, VTO

(V_{T0}), in volts extrapolated to $i_D = 0$ for large devices, the intrinsic transconductance parameter, KP (K'), in amps/volt^2, the bulk threshold parameter, GAMMA (γ) in volt$^{1/2}$, the surface potential at strong inversion, PHI ($2\phi_f$), in volts, and the channel-length modulation parameter, LAMBDA (λ), in volt^{-1}. Values for these parameters can be found in Table 3.1-2.

Sometimes, one would rather let SPICE calculate the above parameters from the appropriate process parameters. This can be done by entering the surface state density in cm^{-2} (NSS), the oxide thickness in meters (TOX), the surface mobility, UO (μ_0), in cm^2/V-s, and the substrate doping in cm^{-3} (NSUB). The equations used to calculate the electrical parameters are

$$\text{VTO} = \phi_{MS} - \frac{q(\text{NSS})}{(\varepsilon_{ox}/\text{TOX})} + \frac{(2q \cdot \varepsilon_{si} \cdot \text{NSUB} \cdot \text{PHI})^{1/2}}{(\varepsilon_{ox}/\text{TOX})} + \text{PHI} \tag{1}$$

$$\text{KP} = \text{UO}\,\frac{\varepsilon_{ox}}{\text{TOX}} \tag{2}$$

$$\text{GAMMA} = \frac{(2q \cdot \varepsilon_{si} \cdot \text{NSUB})^{1/2}}{(\varepsilon_{ox}/\text{TOX})} \tag{3}$$

and

$$\text{PHI} = \left| 2\phi_F \right| = \frac{2kT}{q} \ln\left(\frac{\text{NSUB}}{n_i}\right) \tag{4}$$

LAMBDA is not calculated from the process parameters for the LEVEL 1 model. The constants for silicon, given in Table 3.1-1, are contained within the SPICE program and do not have to be entered.

The next model parameters considered are those that were considered in Sec. 3.2. The first parameters considered were associated with the bulk-drain and bulk-source pn junctions. These parameters include the reverse current of the drain-bulk or source-bulk junctions in A (IS) or the reverse-current density of the drain-bulk or source-bulk junctions in A/m^2 (JS). JS requires the specification of AS and AD on the model line. If IS is specified, it overrides JS. The default value of IS is usually 10^{-14} A. The next parameters considered in Sec. 3.2 were the drain ohmic resistance in ohms (RD), the source ohmic resistance in ohms (RS), and the sheet resistance of the source and drain in ohms/square (RSH). RSH is overridden if RD or RS are entered. To use RSH, the values of NRD and NRS must be entered on the model line.

The drain-bulk and source-bulk depletion capacitors can be specified by the zero-bias bulk junction bottom capacitance in farads per m^2 of junction area (CJ). CJ requires NSUB and assumes a step junction using a formula similar to Eq. (12) of Sec. 2.2. Alternately, the drain-bulk and source-bulk depletion capacitances can be specified using Eqs. (5) and (6) of Sec. 3.2. The necessary parameters include the zero-bias bulk-drain junction capacitance in farads (CBD), the zero-bias bulk-source junction capacitance in farads (CBS), the bulk junction potential in volts (PB), the coefficient for forward-bias depletion capacitance (FC), the zero-bias bulk junction sidewall capacitance in farads per meter of junction perimeter (CJSW), and the bulk junction sidewall capacitance grading coefficient (MJSW). If CBD or CBS is specified, then CJ is overridden. The values of

AS, AD, PS, and PD must be given on the device line to use the above parameters. Typical values of these parameters are given in Table 3.2-1.

The next parameters discussed in Sec. 3.2 were the gate overlap capacitances. These capacitors are specified by the gate-source overlap capacitance in farads/meter (CGSO), the gate-drain overlap capacitance in farads/meter (CGDO), and the gate-bulk overlap capacitance in farads/meter (CGBO). Typical values of these overlap capacitances can be found in Table 3.2-1. Finally, the noise parameters include the flicker noise coefficient (KF) and the flicker noise exponent (AF). Typical values of these parameters are 10^{-28} and 1, respectively.

Additional parameters not discussed in Sec. 3.4 include the type of gate material (TPG), the thin oxide capacitance model flag and the coefficient of channel charge allocated to the drain (XQC). The choices for TPG are +1 if the gate material is opposite to the substrate, –1 if the gate material is the same as the substrate, and 0 if the gate material is aluminum. A charge controlled model is used in the SPICE simulator if the value of the parameter *XQC* has a value smaller than or equal to 0.5. This model attempts to keep the sum of charge associated with each node equal to zero. If XQC is larger than 0.5, charge conservation is not guaranteed.

In order to illustrate its use and to provide examples for the novice user to follow, several examples will be given showing how to use SPICE to perform various simulations.

Example 3.6-1 Use of SPICE to Simulate MOS Output Characteristics

Use SPICE to obtain the output characteristics of the n-channel transistor shown in Fig. 3.6-2 using the LEVEL 1 model and the parameter values of Table 3.1-2. The output curves are to be plotted for drain-source voltages from 0 to 5 V and for gate-source voltages of 1, 2, 3, 4, and 5 V. Assume that the bulk voltage is zero. Table 3.6-1 shows the input file for SPICE to solve this problem. The first line is a title for the simulation file and must be present. The lines not preceded by "`.`" define the interconnection of the circuit. The second line describes how the transistor is connected, defines the model to be used, and gives the `W` and `L` values. Note that because the units are meters, the suffix "`U`" is used to convert to μm. The third and forth lines describe the independent voltages. `VDS` and `VGS` are used to bias the MOSFET. The fifth line is the model description for M1. The remaining lines instruct SPICE to perform a dc sweep and print desired results. "`.DC`" asks for a dc sweep. In this particular case, a nested dc sweep is specified in order to avoid seven consecutive analyses. The "`.DC...`" line will set `VGS` to a value of 1 V and then sweep `VDS` from 0 to 5 V in increments of 0.2 V. Next, it will increment `VGS` to 2 V and repeat the `VDS` sweep. This is continued until five VDS sweeps have been made with the desired values of `VGS`. The "`.PRINT...`" line directs the program to print the values of the dc sweeps. The last line of every SPICE input file must be .END which is line eleven. Fig. 3.6-3 shows the output plot of this analysis.

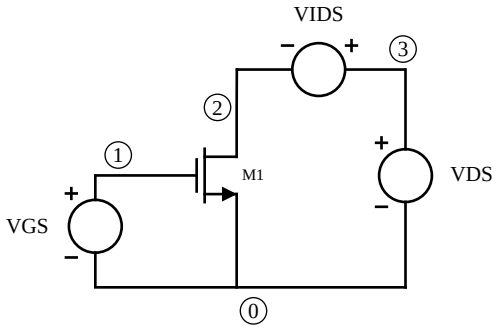


Figure 3.6-2 Circuit for Example 3.6-1

Table 3.6-1 SPICE Input File for Example 3.6-1.

```
Ex. 3.6-1 Use of SPICE to Simulate MOS Output
M1 2 1 0 0 MOS1 W=5U L=1.0U
VDS 2 0 5
VGS 1 0 1
.MODEL MOS1 NMOS VTO=0.7 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
.DC VDS 0 5 0.2 VGS 1 5 1
.PRINT DC V(2) I(VDS)
.END
```

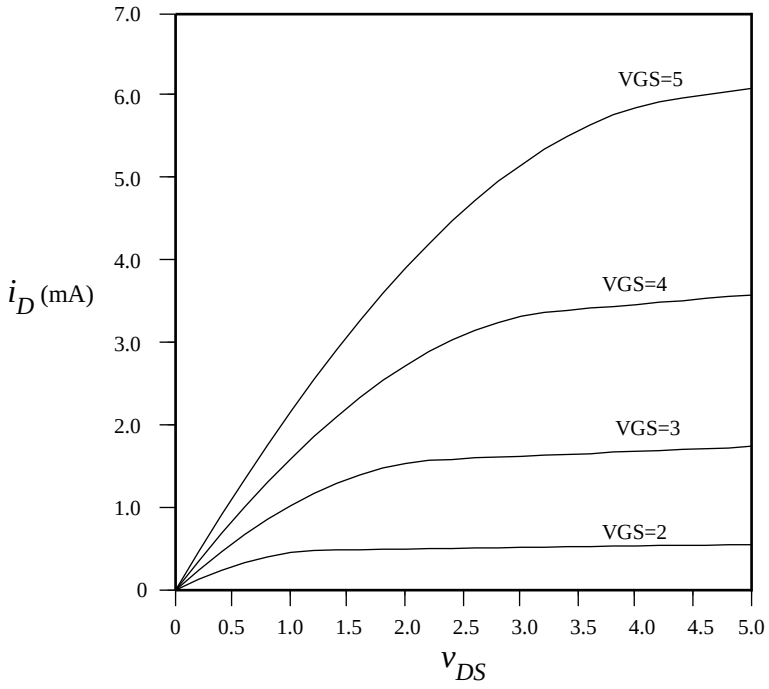


Figure 3.6-3 Output from Example 3.6-1

Example 3.6-2 dc Analysis of Fig. 3.6-4.

Use the SPICE simulator to obtain a plot of the value of v_{OUT} as a function of v_{IN} of Fig. 3.6-3. Identify the dc value of v_{IN} which gives $v_{OUT} = 0$ V.

The input file for SPICE is shown in Table 3.6-2. It follows the same format as the previous example except that two types of transistors are used. These models are designated by MOSN and MOSP. A dc sweep is requested starting from $v_{IN} = 0$ V and going to +5 V. Figure 3.6-5 shows the resulting output of the dc sweep.

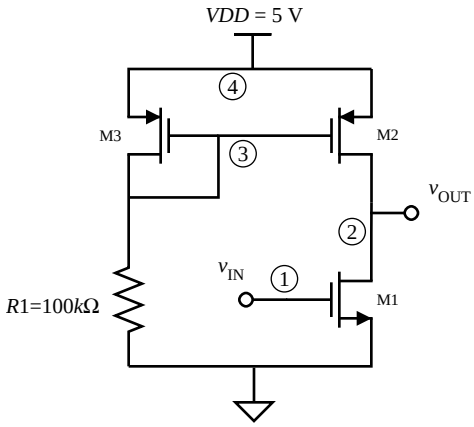


Figure 3.6-4 A simple MOS amplifier for Example 3.6-2

Table 3.6-2 SPICE Input File for Example 3.6-2.

```
Ex. 3.6-2 DC Analysis of Fig. 3.6-3.
M1 2 1 0 0 MOSN W=20U L=10U
M2 2 3 4 4 MOSP W=10U L=20U
M3 3 3 4 4 MOSP W=10U L=20U
R1 3 0 100K
VDD 4 0 DC 5.0
VIN 1 0 DC 5.0
.MODEL MOSN NMOS VTO=0.7 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
.MODEL MOSP PMOS VTO=-0.7 KP=50U GAMMA=0.57 LAMBDA=0.05 PHI=0.8
.DC VIN 0 5 0.1
.PRINT DC V(2)
.END
```

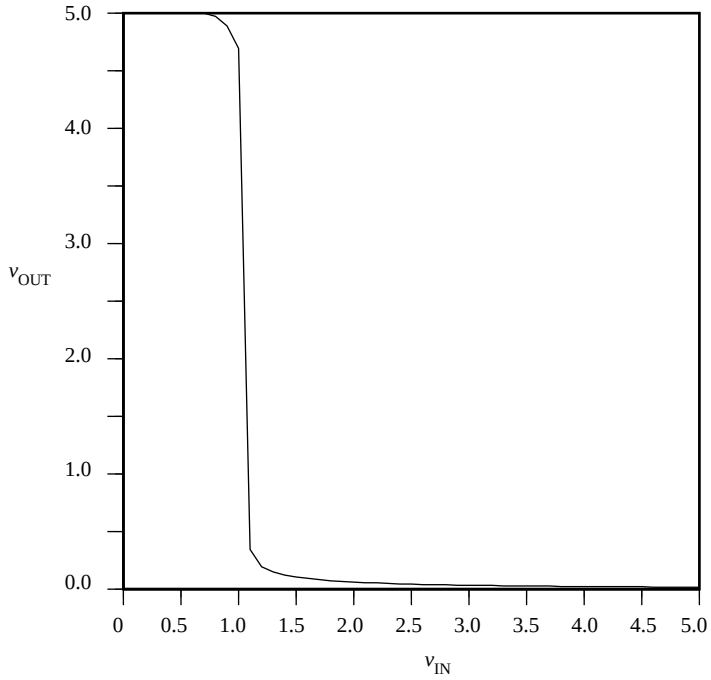


Figure 3.6-5 Output of Example 3.6-2

Example 3.6-3 ac Analysis of Fig. 3.6-4

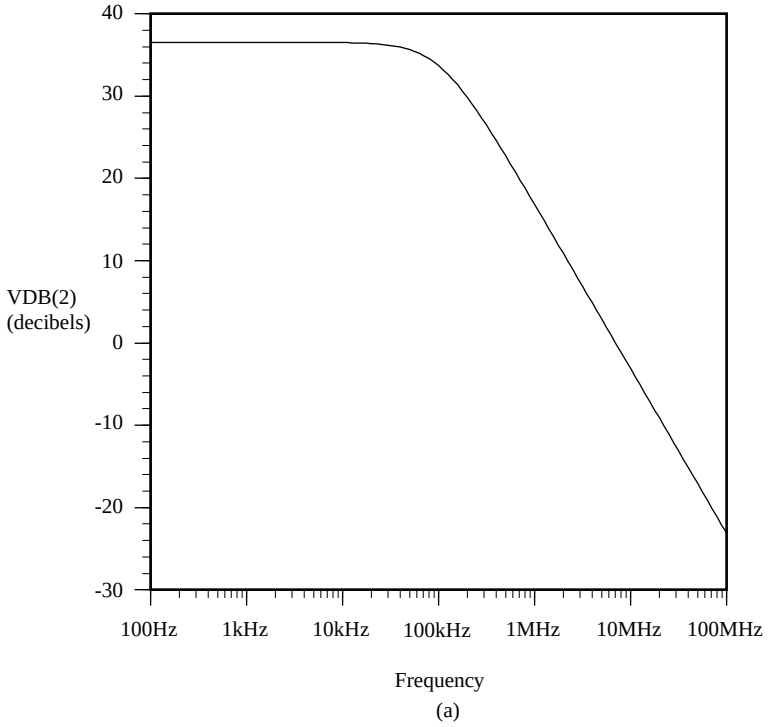
Use SPICE to obtain a small signal frequency response of $V_{OUT}(\omega)/V_{IN}(\omega)$ when the amplifier is biased in the transition region. Assume that a 5 pF capacitor is attached to the output of Fig. 3.6-4 and find the magnitude and phase response over the frequency range of 100 Hz to 100 MHz.

The SPICE input file for this example is shown in Table 3.6-3. It is important to note that v_{IN} has been defined as both an ac and dc voltage source with a dc value of 1.07 V. If the dc voltage were not included, SPICE would find the dc solution for $v_{IN} = 0$ V which is not in the transition region. Therefore, the small signal solution would not be evaluated in the transition region. Once the dc solution has been evaluated, the amplitude of the signal applied as the ac input has no influence on the simulation. Thus, it is convenient to use ac inputs of unity in order to treat the output as a gain quantity. Here, we have assumed an ac input of 1.0 volt peak.

The simulation desired is defined by the "`.AC DEC 20 100 100MEG`" line. This line directs SPICE to make an ac analysis over a log frequency with 20 points per decade from 100 Hz to 100 MHz. The `.OP` option has been added to print out the dc voltages of all circuit nodes in order to verify that the ac solution is in the desired region. The program will calculate the linear magnitude, dB magnitude, and phase of the output voltage. Figures 3.6-6(a) and (b) show the magnitude (dB) and the phase of this simulation.

Table 3.6-3 SPICE Input File for Example 3.6-3.

```
Ex. 3.6-3 AC Analysis of Fig. 3.6-3.
M1 2 1 0 0 MOSN W=20U L=10U
M2 2 3 4 4 MOSP W=10U L=20U
M3 3 3 4 4 MOSP W=10U L=20U
CL 2 0 5P
R1 3 0 100K
VDD 4 0 DC 5.0
VIN 1 0 DC -2.42 AC 1.0
.MODEL MOSN NMOS VTO=0.7 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
.MODEL MOSP PMOS VTO=-0.7 KP=50U GAMMA=0.57 LAMBDA=0.05 PHI=0.8
.AC DEC 20 100 100MEG
.OP
.PRINT AC VM(2) VDB(2) VP(2)
.END
```



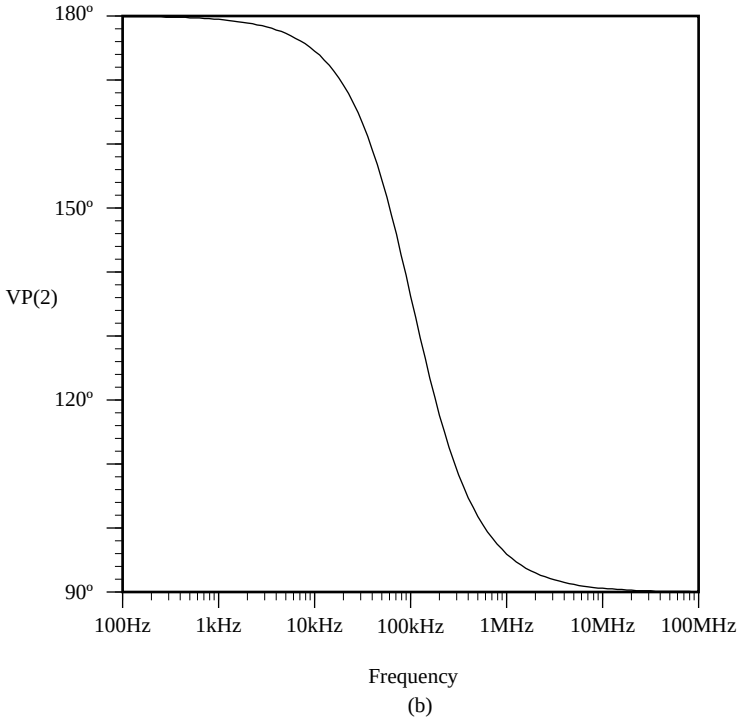


Figure 3.6-6 (a) Magnitude response of Example 3.6-3, (b) Phase response of Example 3.6-3

Example 3.6-4 Transient Analysis of Fig. 3.6-4

The last simulation to be made with Fig. 3.6-4 is the transient response to an input pulse. This simulation will include the 5 pF output capacitor of the previous example and will be made from time zero to 4 microseconds.

Table 3.6-4 shows the SPICE input file. The input pulse is described using the piecewise linear capability (PWL) of SPICE. The output desired is defined by "`.TRAN 0.01U 4U`" which asks for a transient analysis from 0 to 4 microseconds at points spaced every 0.01 microseconds. The output will consist of both $v_{IN}(t)$ and $v_{OUT}(t)$ and is shown in Fig. 3.6-7.

The above examples will serve to introduce the reader to the basic ideas and concepts of using the SPICE program. In addition to what the reader has distilled from these examples, a useful set of guidelines is offered which has resulted from extensive experience in using SPICE. These guidelines are listed as:

1. Never use a simulator unless you know the range of answers beforehand.
2. Never simulate more of the circuit than is necessary.
3. Always use the simplest model that will do the job.
4. Always start a dc solution from the point at which the majority of the devices are on.
5. Use a simulator in exactly the same manner as you would make the measurement on the bench.
6. Never change more than one parameter at a time when using the simulator for design.
7. Learn the basic operating principles of the simulator so that you can enhance its capability. Know how to use its options.
8. Watch out for syntax problems like O and 0.
9. Use the correct multipliers for quantities.
10. Use common sense.

Most problems with simulators can be traced back to a violation of one or more of these guidelines.

Table 3.6-4 SPICE Output for Example 3.6-4.

```
Ex. 3.6-4 Transient Analysis of Fig. 3.6-3.
M1 2 1 0 0 MOSN W=20U L=10U
M2 2 3 4 4 MOSP W=10U L=20U
M3 3 3 4 4 MOSP W=10U L=20U
CL 2 0 5P
R1 3 0 100K
VDD 4 0 DC 5.0
VIN 1 0 PWL(0 0V 1U 0V 1.05U 3V 3U 3V 3.05U 0V 6U 0V)
*VIN 1 0 DC -2.42 AC 1.0
.MODEL MOSN NMOS VTO=0.7 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
.MODEL MOSP PMOS VTO=-0.7 KP=50U GAMMA=0.57 LAMBDA=0.05 PHI=0.8
.TRAN 0.01U 4U
.PRINT TRAN V(2) V(1)
.END
```

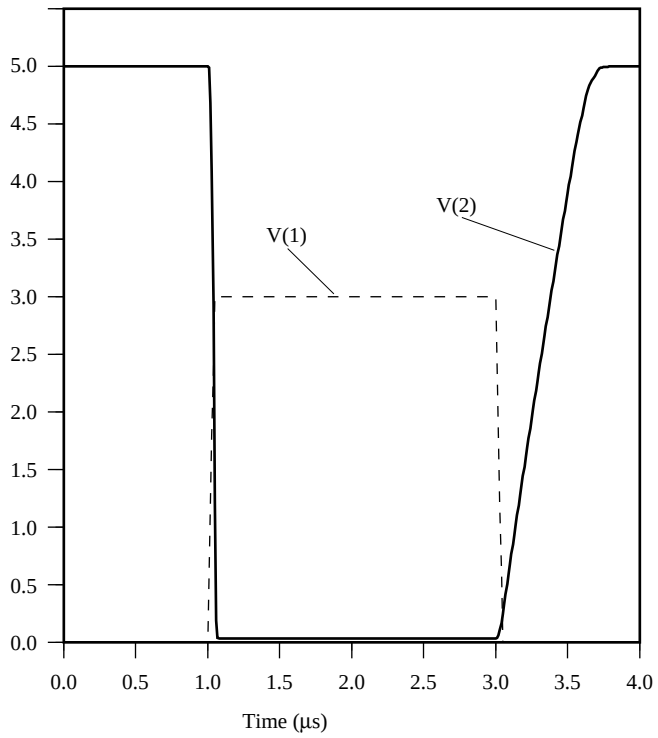


Figure 3.6-7 Transient response of Example 3.6-4

There are many SPICE simulators in use today. The discussion here focused on the more general versions of SPICE and should apply in most cases. However, there is nothing fundamental about the syntax or use of a circuit simulator, so it is prudent to carefully study the manuel of the SPICE simulator you are using.

3.7 Summary

This chapter has tried to give the reader the background necessary to be able to simulate CMOS circuits. The approach used has been based on the SPICE simulation program. This program normally has three levels of MOS models which are available to the user. The function of models is to solve for the dc operating conditions and then use this information to develop a linear small-signal model. Sec. 3.1 described the LEVEL 1 model used by SPICE to solve for the dc operating point. This model also uses the additional model parameters presented in Sec. 3.2. These parameters include bulk resistance, capacitance, and noise. A small-signal model that was developed from the large-signal model was described in Sec. 3.3. These three sections represent the basic modeling concepts for MOS transistors.

Models for computer simulation were presented. The SPICE Level 3 model which is effective for device lengths of 0.8μm and greater was covered. The BSIM3v3 model which is effective for deep-submicron devices was introduced. Large signal models suitable for weak inversion were also described. Further details of these models and other models are found in the references for this chapter. A brief background of simulation methods was presented in Sec. 3.6. Simulation of MOS circuits using SPICE was discussed. After reading this chapter, the reader should be able to use the model information presented along with a SPICE simulator to analyze MOS circuits. This

ability will be very important in the remainder of this text. It will be used to verify intuitive design approaches and to perform analyses beyond the scope of the techniques presented. One of the important aspects of modeling is to determine the model parameters which best fit the MOS process that is being used. The next chapter will be devoted to this subject.

PROBLEMS

1. Sketch to scale the output characteristics of an enhancement n-channel device if $V_T = 0.7$ volt and $I_D = 500\ \mu$A when $V_{GS} = 5$ V in saturation. Choose values of $V_{GS} = 1, 2, 3, 4$, and 5 V. Assume that the channel modulation parameter is zero.
2. Sketch to scale the output characteristics of an enhancement p-channel device if $V_T = -0.7$ volt and $I_D = -500\ \mu$A when $V_{GS} = -1, -2, -3, -4$, and -6 V. Assume that the channel modulation parameter is zero.
3. In Table 3.1-2, why is γ_P greater than γ_N for a n-well, CMOS technology?
4. A large-signal model for the MOSFET which features symmetry for the drain and source is given as

$$i_D = K'\frac{W}{L}\{[(v_{GS} - V_{TS})^2 u(v_{GS} - V_{TS})] - [(v_{GD} - V_{TD})^2 u(v_{GD} - V_{TD})]$$

   where $u(x)$ is 1 if x is greater than or equal to zero and 0 if x is less than zero (step function) and V_{TX} is the threshold voltage evaluated from the gate to X where X is either S (Source) or D (Drain). Sketch this model in the form of i_D versus v_{DS} for a constant value of v_{GS} ($v_{GS} > V_{TS}$) and identify the saturated and nonsaturated regions. Be sure to extend this sketch for both positive and negative values of v_{DS}. Repeat the sketch of i_D versus v_{DS} for a constant value of v_{GD} ($v_{GD} > V_{TD}$). Assume that both V_{TS} and V_{TD} are positive.
5. Equation (11) and Eq. (18) in Sec. 3.1 describe the MOS model in nonsaturation and saturation region, respectively. These equations do not agree at the point of transition between between saturation and nonsaturation regions. For hand calculations, this is not an issue, but for computer analysis, it is. How would you change Eq. (18) so that it would agree with Eq. (11) at $v_{DS} = v_{DS}$ (sat)?
6. Using the values of Tables 3.1-1 and 3.2-1, calculate the values of CGB, CGS, and CGD for a MOS device which has a W of 5 μm and an L of 1 μm for all three regions of operation
7. Find C_{BX} at $V_{BX} = 0$ V and 0.75 V of Fig. P3.7 assuming the values of Table 3.2-1 apply to the MOS device where FC = 0.5 and PB = 1 V. Assume the device is n-channel and repeat for a p-channel device.

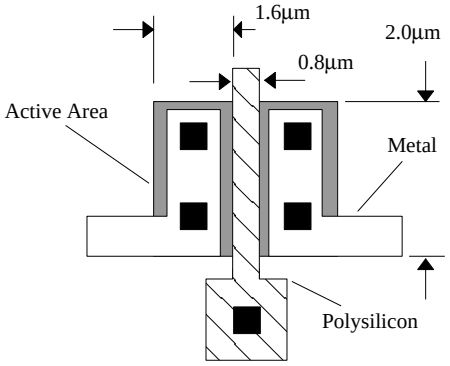


Figure P3.7

8. Calculate the value of C_{GB}, C_{GS}, and C_{GD} for an n-channel device with a length of 1 μm and a width of 5 μm. Assume $V_D = 2$ V, $V_G = 2.4$ V, and $V_S = 0.5$ V and let $V_B = 0$ V. Use model parameters from Tables 3.1-1, 3.1-2, and 3.2-1.
9. Calculate the transfer function $v_{out}(s)/v_{in}(s)$ for the circuit shown in Fig. P3.9. The W/L of M1 is 2µm/0.8µm and the W/L of M2 is 4µm/4µm. Note that this is a small-signal analysis and the input voltage has a dc value of 2 volts.

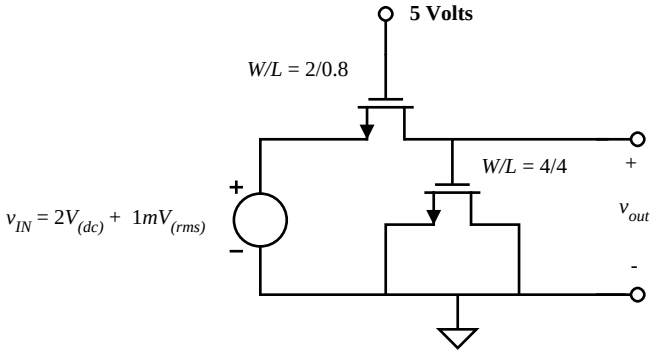


Figure P3.9

10. Design a low-pass filter patterened after the circuit in Fig. P3.9 that achieves a -3dB frequency of 100 KHz.
11. Repeat Examples 3.3-1 and 3.3-2 if the W/L ratio is 100 μm/10 μm.
12. Find the complete small-signal model for an n-channel transistor with the drain at 4 V, gate at 4 V, source at 2 V, and the bulk at 0 V. Assume the model parameters from Tables 3.1-1, 3.1-2, and 3.2-1, and $W/L = 10$ μm/1 μm.
13. Consider the circuit in Fig P3.13. It is a parallel connection of n mosfet transistors. Each transistor has the same length, L, but each transistor can have a different width, W. Derive an expression for W and L for a single transistor that replaces, and is equivalent to, the multiple parallel transistors.

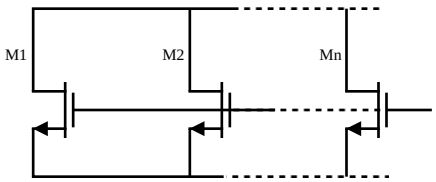


Figure P3.13

14. Consider the circuit in Fig P3.14. It is a series connection of n mosfet transistors. Each transistor has the same width, W, but each transistor can have a different length, L. Derive an expression for W and L for a single transistor that replaces, and is equivalent to, the multiple parallel transistors. When using the simple model, you must ignore body effect.

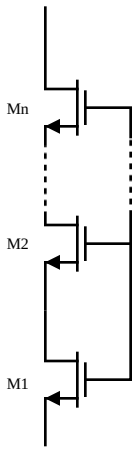


Figure P3.14

15. Calculate the value for V_{ON} for n MOS transistor in weak inversion assuming that *fs* and *fn* can be approximated to be unity (1.0).
16. Develop an expression for the small signal transconductance of a MOS device operating in weak inversion using the large signal expression of Eq. (5) of Sec. 3.5.
17. Another way to approximate the transition from strong inversion to weak inversion is to find the current at which the weak-inversion transconductance and the strong-inversion transconductance are equal. Using this method and the approximation for drain current in weak inversion (Eq. (5) of Sec. 3.5), derive an expression for drain current at the transition between strong and weak inversion.
18. Consider the circuit illustrated in Fig. P3.19. (a) Write a SPICE netlist that describes this circuit. (b) Repeat part (a) with M2 being 2μm/1μm and it is intended that M3 and M2 are ratio matched, 1:2.
19. Use SPICE to perform the following analyses on the circuit shown in Fig. P3.19: (a) Plot v_{OUT} versus v_{IN} for the nominal parameter set shown. (b) Separately, vary K' and V_T by +10% and repeat part (a)—four simulations.

Parameter	N-Channel	P-Channel	Units
V_T	0.7	-0.7	V
K'	110	50	$\mu A/V^2$
l	0.04	0.05	V^{-1}

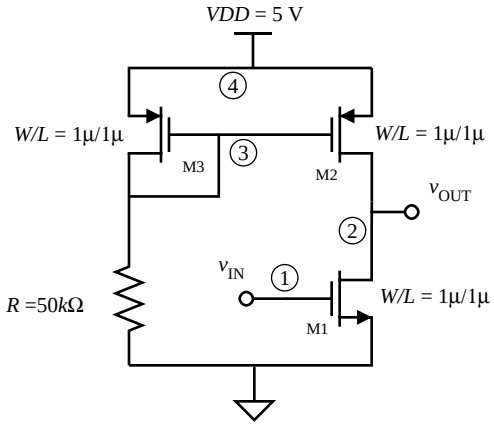


Figure P3.19

20. Use SPICE to plot i_2 as a function of v_2 when i_1 has values of 10, 20, 30, 40, 50, 60, and 70 μA for Fig. P3.20. The maximum value of v_2 is 5 V. Use the model parameters of $V_T = 0.7$ V and $K' = 110$ μA/V^2 and $\lambda = 0.01$ V^{-1}. Repeat with $\lambda = 0.04$ V^{-1}.

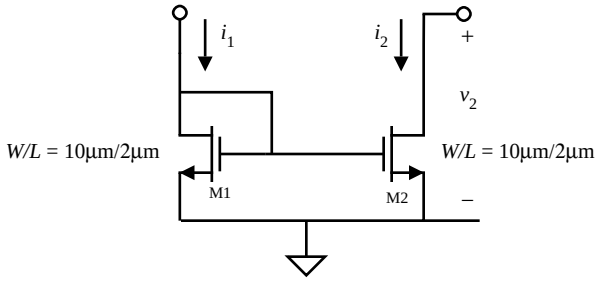


Figure P3.20

21. Use SPICE to plot i_D as a function of v_{DS} for values of v_{GS} = 1, 2, 3, 4 and 5 V for an n-channel transistor with V_T = 1 V, K' = 110 μA/V^2, and l = 0.04 V^{-1}. Show how SPICE can be used to generate and plot these curves simultaneously as illustrated by Fig. 3.1-3.
22. Repeat Example 3.6-1 if the transistor of Fig. 3.6-5 is a PMOS having the model parameters given in Table 3.1-2.
23. Repeat Examples 3.6-2 through 3.6-4 for the circuit of Fig. 3.6-2 if R1 = 200 KΩ.

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Chapter 4 Analog CMOS Subcircuits

From the viewpoint of Table 1.1-2, the previous two chapters have provided the background for understanding the technology and modeling of CMOS devices and components compatible with the CMOS process. The next step toward our objective—methodically developing the subject of CMOS analog-circuit design—is to develop subcircuits. These simple circuits consist of one or more transistors; they are simple; and they generally perform only one function. A subcircuit is typically combined with other simple circuits to generate a more complex circuit function. Consequently, the circuits of this and the next chapter can be considered as building blocks.

The *operational amplifier*, or *op amp*, to be covered in Chapters 6 and 7, is a good example of how simple circuits are combined to perform a complex function. Figure 4.0-1 presents a hierarchy showing how an operational amplifier—a complex circuit—might be related to various simple circuits. Working our way backward, we note that one of the stages of an op amp is the differential amplifier. The differential amplifier consists of simple circuits that might include a current sink, a current-mirror load, and a source-coupled pair. Another stage of the op amp is a second gain stage, which might consist of an inverter and a current-sink load. If the op amp is to be able to drive a low-impedance load, an output stage is necessary. The output stage might consist of a source follower and a current-sink load. It is also necessary to provide a stabilized bias for each of the previous stages. The biasing stage could consist of a current sink and current mirrors to distribute the bias currents to the other stages.

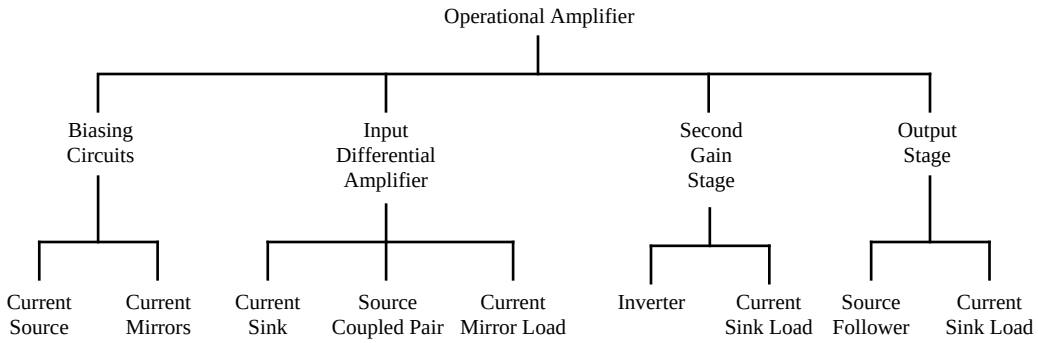


Figure 4.0-1 Illustration of the hierarchy of analog circuits for an operational amplifier.

The subject of basic CMOS analog circuits has been divided into two chapters to avoid one lengthy chapter and yet provide sufficient detail. Chapter 4 covers the simpler subcircuits, including: the MOS switch, active loads, current sinks/sources, current mirrors and current amplifiers, and voltage and current references. Chapter 5 will examine more complex circuits like CMOS amplifiers. That chapter represents a natural extension of the material presented in Chapter 4. Taken together, these two chapters are fundamental for the analog CMOS designer's understanding and capability, as most designs will start at this level and progress upward to synthesize the more complex circuits and systems of Table 1.1-2.

4.1 MOS Switch

The switch finds many applications in integrated-circuit design. In analog circuits, the switch is used to implement such useful functions as the switched simulation of a resistor [1]. The switch is also useful for multiplexing, modulation, and a number of other applications. The switch is used as a transmission gate in digital circuits and adds a dimension of flexibility not found in standard logic circuits. The objective of this section is to study the characteristics of switches that are compatible with CMOS integrated circuits.

We begin with the characteristics of a voltage-controlled switch. Figure 4.1-1 shows a model for such a device. The voltage v_C controls the state of the switch—ON or OFF. The voltage-controlled switch is a three-terminal network with terminals A and B comprising the switch and terminal C providing the means of applying the control voltage v_C. The most important characteristics of a switch are its ON resistance, r_{ON}, and its OFF resistance, r_{OFF}. Ideally r_{ON} is zero and r_{OFF} is infinite. Reality is such that r_{ON} is never zero and r_{OFF} is never infinite. Moreover, these values are never constant with respect to terminal conditions. In general, switches can have some form of voltage offset which is modeled by V_{OS} of Fig. 4.1-1. V_{OS} represents the small voltage that may exist between terminals A and B when the switch is in the ON state and the current is zero. I_{OFF} represents the leakage current that may flow in the OFF state of the switch. Currents I_A and I_B represent leakage currents from the switch terminals to ground (or some other supply potential). The polarities of the offset sources and leakage currents are not known and have been arbitrarily assigned the directions indicated in Fig. 4.1-1. The parasitic capacitors are an important consideration in the application of analog sampled-data circuits. Capacitors C_A, and C_B, are the parasitic capacitors between the switch terminals A and B and ground. Capacitor C_{AB} is the parasitic capacitor between the switch terminals A and B. Capacitors C_{AC} and C_{BC} are parasitic capacitors that may exist between the voltage-control terminal C and the switch terminals A and B. Capacitors C_{AC} and C_{BC} contribute to the effect called *charge feedthrough*—where a portion of the control voltage appears at the switch terminals A and B.

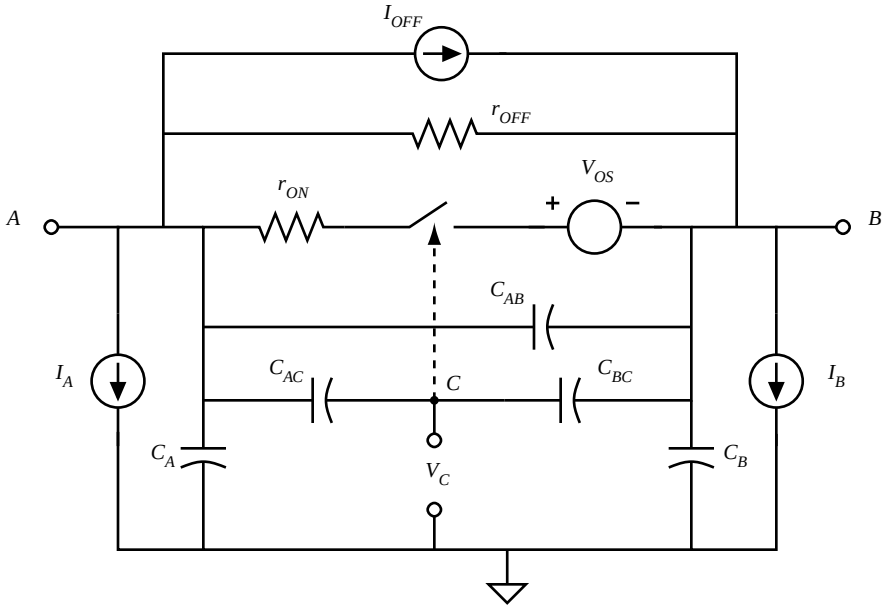


Figure 4.1-1 Model for a nonideal switch.

One advantage of MOS technology is that it provides a good switch. Figure 4.1-2 shows a MOS transistor that is to be used as a switch. Its performance can be determined by comparing Fig. 4.1-1 with the large-signal model for the MOS transistor. We see that either terminal, *A* or *B*, can be the drain or the source of the MOS transistor depending upon the terminal voltages (e.g., for an n-channel transistor, if terminal *A* is at a higher potential than *B*, then terminal *A* is the drain and terminal *B* is the source). The ON resistance consists of the series combination of r_D, r_S, and whatever channel resistance exists. Typically, by design, the contribution from r_D and r_S is small such that the primary consideration is the channel resistance. An expression for the channel resistance can be found as follows. In the ON state of the switch, the voltage across the switch should be small and v_{GS} should be large. Therefore the MOS device is assumed to be in the nonsaturation region. Equation (1) of Sec. 3.1, repeated below, is used to model this state.

$$I_D = \frac{K'W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{1}$$

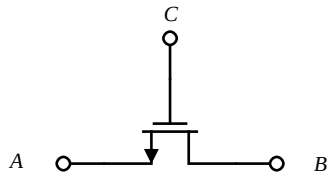


Figure 4.1-2 An n-channel transistor used as a switch.

where V_{DS} is less than $V_{GS} - V_T$ but greater than zero. (V_{GS} becomes V_{GD} if V_{DS} is negative.) The small-signal channel resistance given as

$$r_{\text{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(V_{GS} - V_T - V_{DS})} \tag{2}$$

Figure 4.1-3 illustrates drain current of an n-channel transistor as a function of the voltage across the drain and source terminals, plotted for equal increasing steps of V_{GS} for W/L = 5/1. This figure illustrates some very important principles about MOS transistor operation. Notice that the curves are not symmetrical about $V_1 = 0$. This is because the transistor terminals (drain and source) switch roles as V_1 crosses zero volts. For example, when V_1 is positive, node *B* is the drain and node *A* is the source and V_{BS} is fixed at -2.5 volts and V_{GS} is fixed as well (for a given V_G). When V_1 is negative, node *B* is the source and node *A* is the drain and as V_1 continues to decrease, V_{BS} decreases and V_{GS} increases resulting in an increase in current.

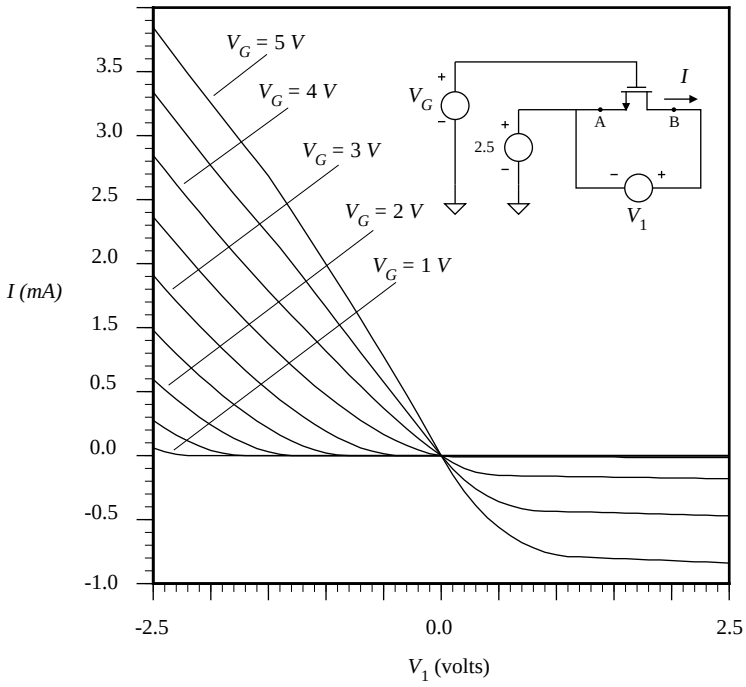


Figure 4.1-3 I-V characteristic of an n-channel transistor operating as a switch.

A plot of r_{ON} as a function of V_{GS} is shown in Fig. 4.1-4 for V_{DS} = 0.1 volts and for W/L = 1, 2, 5, and 10. It is seen that a lower value of r_{ON} is achieved for larger values of W/L. When V_{GS} approaches V_T (V_T = 0.7 volts in this case), r_{ON} approaches infinity because the switch is turning off.

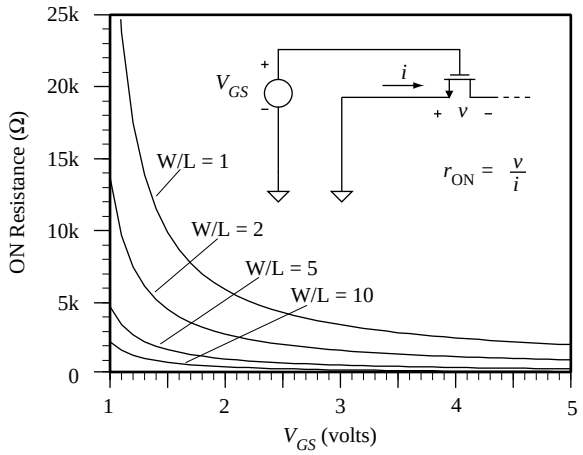


Figure 4.1-4 Illustration of on resistance for an n-channel transistor.

When, V_{GS} is less than or equal to V_T the switch is OFF and r_{OFF} is ideally infinite. Of course, it is never infinite, but because it is so large, the performance in the OFF state is dominated by the drain-bulk and source-bulk leakage current as well as subthreshold leakage from drain to source. The leakage from drain and source to bulk is primarily due to the pn junction leakage current and is modeled in Fig. 4.1-1 as I_A and I_B. Typically this

leakage current is on the order of 1 fA/μm^2 at room temperature and doubles for every 8 °C increase (see Ex. 2.5-1).

The offset voltage modeled in Fig. 4.1-1 does not exist in MOS switches and thus is not a consideration in MOS switch performance. The capacitors C_A, C_B, C_{AC}, and C_{BC} of Fig. 4.1-1 correspond directly to the capacitors C_{BS}, C_{BD}, C_{GS}, and C_{GD} of the MOS transistor (see Fig. 3.2-1). C_{AB} is small for the MOS transistor and is usually negligible.

One important aspect of the switch is the range of voltages on the switch terminals compared to the control voltage. For the n-channel MOS transistor we see that the gate voltage must be considerably larger than either the drain or source voltage in order to ensure that the MOS transistor is ON. (For the p-channel transistor, the gate voltage must be considerably less than either the drain or source voltage.) Typically, the bulk is taken to the most negative potential for the n-channel switch (positive for the p-channel switch). This requirement can be illustrated as follows for the n-channel switch. Suppose that the ON voltage of the gate is the positive power supply V_{DD}. With the bulk to ground this should keep the n-channel switch ON until the signal on the switch terminals (which should be approximately identical at the source and drain) approaches $V_{DD} - V_T$. As the signal approaches $V_{DD} - V_T$ the switch begins to turn OFF. Typical voltages used for an n-channel switch are shown in Fig. 4.1-5 where the switch is connected between the two networks shown.

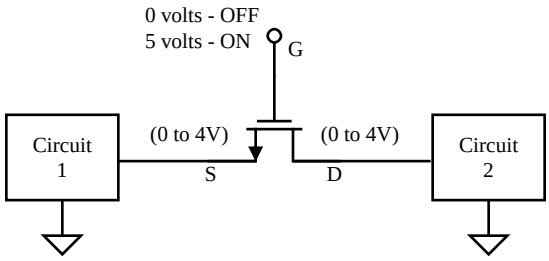


Figure 4.1-5 Application of an n-channel transistor as a switch with typical terminal voltages indicated.

Consider the use of a switch to charge a capacitor as shown in Fig. 4.1-6. An n-channel transistor used as a switch and ϕ is the control voltage (clock) applied to the gate. The ON resistance of the switch is important during the charge transfer phase of this circuit. For example, when ϕ goes high ($V_\phi > v_{\text{in}} + V_T$), M1 connects C to the voltage source v_{in}. The equivalent circuit at this time is shown in Fig. 4.1-7. It can be seen that C will charge to v_{in} with the time constant of $r_{\text{ON}}C$. For successful operation $r_{\text{ON}}C << T$ where T is the time ϕ is high. Clearly, r_{ON}varies greatly with v_{gs}, as illustrated in Fig. 4.1-4. The worst-case value for r_{ON} (the highest value) during the charging of C, is when $v_{ds} = 0$ and $v_{gs} = V_\phi - v_{\text{in}}$. This value should be used when sizing the transistor to achieve the desired charging time.

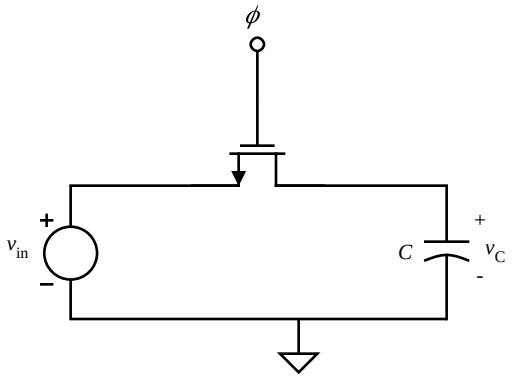


Figure 4.1-6 An application of a MOS switch.

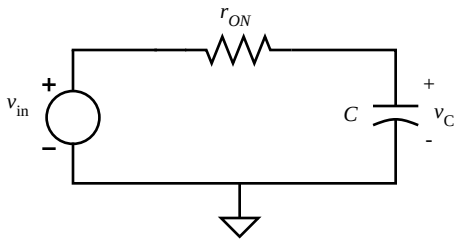


Figure 4.1-7 Model for the ON state of the switch in Fig 4.1-6.

Consider a case where the time ϕ is high is $T = 0.1\ \mu$s and $C = 0.2$ pF, then r_{ON} must be less than 100 kΩ if sufficient charge transfer occurs in five time constants. For a 5-volt clock swing, v_{in} of 2.5 volts, the MOS device of Fig. 4.1-4 with $W = L$ gives r_{ON} on the order of 2.8 kΩ, which is sufficiently small to transfer the charge in the desired time. It is desirable to keep the switch size as small as possible (minimize $W \times L$) to minimize charge feedthrough from the gate.

The OFF state of the switch has little influence upon the performance of the circuit in Fig. 4.1-6 except for the leakage current. Figure 4.1-8 shows a sample-and-hold circuit where the leakage current can create serious problems. If C_H is not large enough, then in the hold mode where the MOS switch is OFF the leakage current can charge or discharge C_H a significant amount.

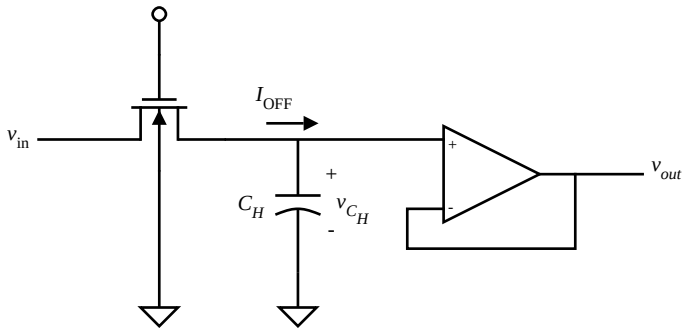


Figure 4.1-8 Example of the influence of I_{off} in a sample-and-hold circuit.

One of the most serious limitations of monolithic switches is the clock feedthrough effect. Clock feedthrough (also called *charge injection, and charge feedthrough*) is due to the coupling capacitance from the gate to both source and drain. This coupling allows charge to be transferred from the gate signal (which is generally a clock) to the drain and source nodes—an undesirable but unavoidable effect. Charge injection involves a complex process whose resulting effects depend upon a number of factors such as the layout of the transistor, its dimensions, impedance levels at the source and drain nodes, and gate waveform. It is hopeless to attempt to describe all of these effects precisely analytically—we have computers to do that! Nevertheless, it is useful to develop a qualitative understanding of this important effect.

Consider a simple circuit suitable for studying charge injection analysis shown in Fig. 4.1-9(a). Figure 4.1-9(b) illustrates modeling a transistor with the channel symbolized as a resistor, $R_{channel}$, and gate-channel coupling capacitance denoted $C_{channel}$. The characters of $C_{channel}$ and $R_{channel}$ depend upon the terminal conditions of the device. The gate-channel coupling is distributed across the channel as is the channel resistance, $R_{channel}$. In addition to the channel capacitance, there is the overlap capacitance, CGS0 and CGD0. It is convenient to approximate the total channel capacitance by splitting it into two capacitors of equal size placed at the gate-source and gate-drain terminals as illustrated in Fig. 4.1-9(c).

For the circuit in Fig. 4.1-9, charge injection is of interest during a high to low transition at the gate of ϕ_1. Moreover, it is convenient to consider two cases regarding the gate transition—a fast transition time, and a slow transition time. Consider the slow-transition case first (what is meant by slow and fast will be covered shortly). As the gate is falling, some charge is being injected into the channel. However, initially, the transistor remains on so that whatever charge is injected flows in the input voltage source, V_S . None of this charge will appear on the load capacitor, C_L . As the gate voltage falls, at some point, the transistor turns off (when the gate voltage reaches $V_S + V_T$). When the transistor turns off, there is no other path for the charge injection other than into C_L .

For the fast case, the time constant associated with the channel resistance and the channel capacitance limits the amount of charge that can flow to the source voltage so that some of the channel charge that is injected while the transistor is on contributes to the total charge on C_L .

To develop some intuition about the fast and slow cases, it is useful to model the gate voltage as a piecewise constant waveform (a quantized waveform) and consider the

charge flow at each transition as illustrated in Fig 4.1-10(a) and (b). In this figure, the range of voltage at C_L illustrated represent the period while the transistor is on. In both cases, the quantized voltage step is the same, but the time between steps is different. The voltage across C_L is observed to be an exponential whose time constant is due to the channel resistance and channel capacitance and does not change from fast case to slow case.

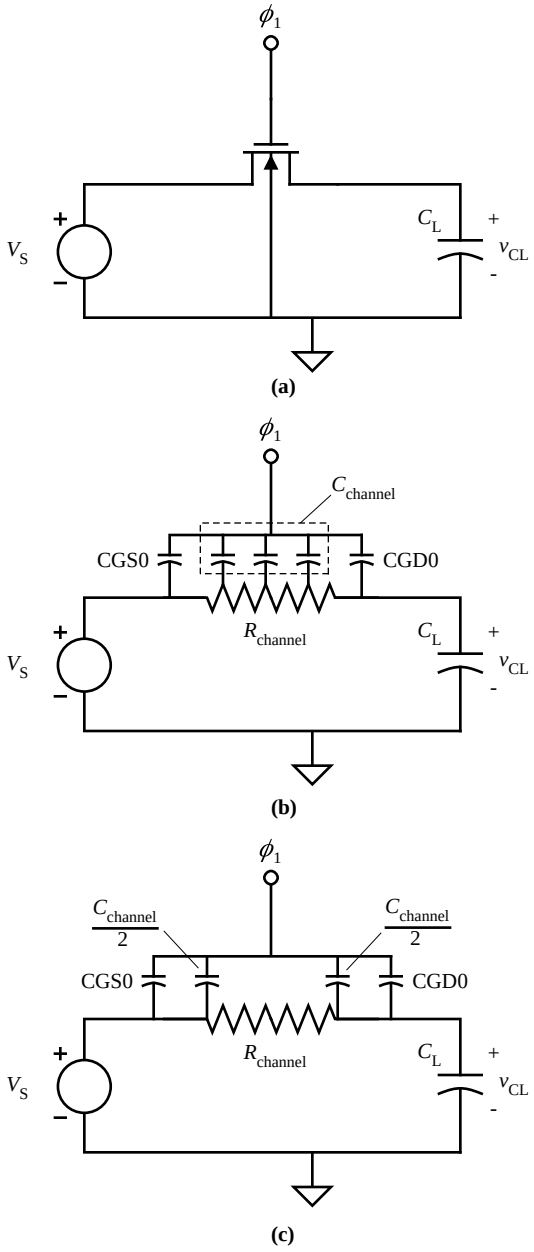


Figure 4.1-9 (a) Simple switch circuit useful for studying charge injection.
(b) Distributed model for the transistor switch. (c) Lumped model of Fig. 4.1-9(a).

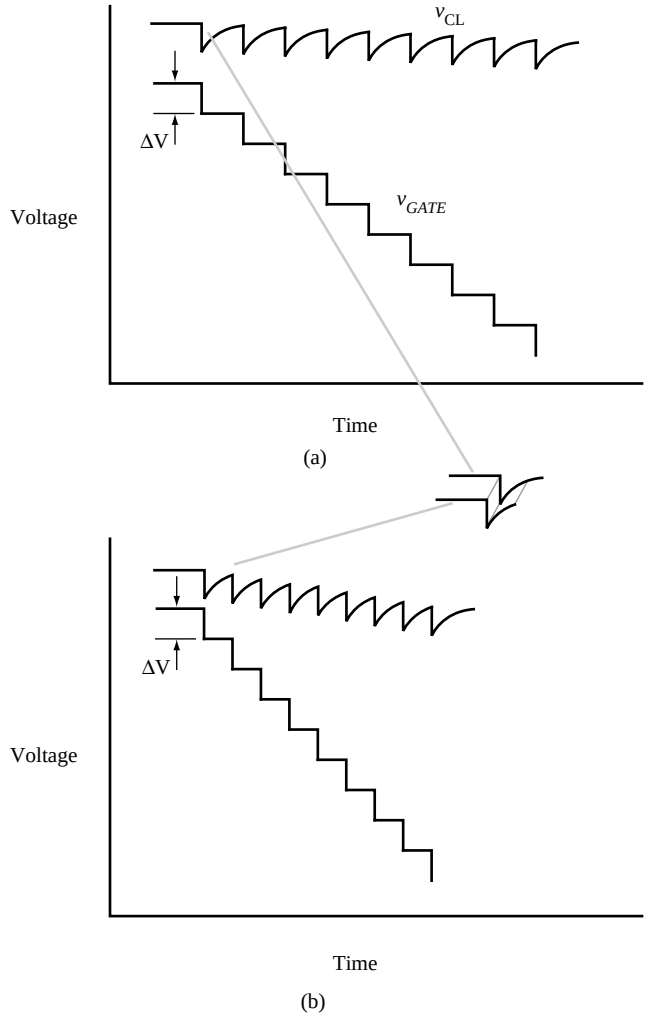


Figure 4.1-10 (a) Illustration of slow ramp and (b) fast ramp using a quantized voltage ramp to illustrate the effects due to the time constant of the channel resistance and capacitance.

Analytical expressions have been derived which describe the approximate operation of a transistor in the slow and fast regimes[2]. Consider the gate voltage traversing from V_H to V_L (e.g., 5.0 volts to 0.0 volts, respectively) described in the time domain as

$$v_G = V_H - Ut \tag{3}$$

When operating in the slow regime defined by the relationship

$$\frac{\beta V_{HT}^2}{2C_L} >> U \tag{4}$$

where V_{HT} is defined as

$$V_{HT} = V_H - V_S - V_T \tag{5}$$

the error (the difference between the desired voltage V_S and the actual voltage, V_{C_L}) due to charge injection can be described as

$$V_{error} = \left(\frac{W \cdot \text{CGD0} + \frac{C_{channel}}{2}}{C_L} \right) \sqrt{\frac{\pi U C_L}{2\beta}} + \frac{W \cdot \text{CGD0}}{C_L} (V_S + V_T - V_L) \quad (6)$$

In the fast switching regime defined by the relationship

$$\frac{\beta V_{HT}^2}{2C_L} << U \quad (7)$$

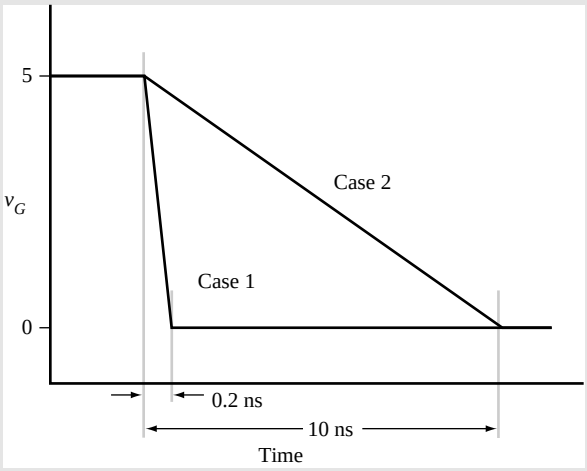
the error voltage is given as

$$V_{error} = \left(\frac{W \cdot \text{CGD0} + \frac{C_{channel}}{2}}{C_L} \right) \left(V_{HT} - \frac{\beta V_{HT}^3}{6U C_L} \right) + \frac{W \cdot \text{CGD0}}{C_L} (V_S + V_T - V_L) \quad (8)$$

The following example illustrates the application of the charge-feedthrough model given by Eq's. (3) through (8).

Example 4.1-1 Calculation of Charge Feedthrough Error

Calculate the effect of charge feedthrough on the circuit shown in Fig. 4.1-9 where V_S = 1.0 volts, C_L = 200 fF, W/L = 0.8µm/0.8µm, and V_G is given for two cases illustrated below. Use model parameters from Tables 3.1-2 and 3.2-1. Neglect ΔL and ΔW effects.



Case 1:

The first step is to determine the value of U in the expression

$v_G = V_H - Ut$

For a transition from 5 volts to 0 volts in 0.2 ns, $U = 25 \times 10^9$ V/s.

In order to determine operating regime, the following relationship must be tested.

$$\frac{\beta V_{HT}^2}{2C_L} >> U \text{ for slow or } \frac{\beta V_{HT}^2}{2C_L} << U \text{ for fast}$$

Observing that there is a backbias on the transistor switch effecting V_T, V_{HT} is

$$V_{HT} = V_H - V_S - V_T = 5 - 1 - 0.887 = 3.113$$

giving

$$\frac{\beta V_{HT}^2}{2C_L} = \frac{110\times10^{-6}\times 3.113^2}{2\times 200\text{f}} = 2.66\times10^9 << 25\times10^9 \quad \text{thus fast regime.}$$

Applying Eq. (8) for the fast regime yields

$$V_{error} = \left(\frac{176\times10^{-18} + \frac{1.58\times10^{-15}}{2}}{200\times10^{-15}}\right)\left(3.113 - \frac{3.32\times10^{-3}}{30\times10^{-3}}\right) + \frac{176\times10^{-18}}{200\times10^{-15}}(5 + 0.887 - 0)$$

$$V_{error} = 19.7 \text{ mV}$$

Case 2:
The first step is to determine the value of U in the expression

$$v_G = V_H - Ut$$

For a transition from 5 volts to 0 volts in 10 ns, $U = 5\times10^8$ thus indicating the slow regime according to the following test

$$2.66\times10^9 >> 5\times10^8$$

$$V_{error} = \left(\frac{176\times10^{-18} + \frac{1.58\times10^{-15}}{2}}{200\times10^{-15}}\right)\sqrt{\frac{314\times10^{-6}}{220\times10^{-6}}} + \frac{176\times10^{-18}}{200\times10^{-15}}(5 + 0.887 - 0)$$

$$V_{error} = 10.95 \text{ mV}$$

This example illustrates the application of the charge-feedthrough model. The reader should be cautioned not to expect Eq's (3) through (8) to give precise answers regarding the amount of charge feedthrough one should expect in an actual circuit. The model should be used as a guide in understanding the effects of various circuit elements and terminal conditions in order to minimize unwanted behavior by design.

It is possible to partially cancel some of the feedthrough effects using the technique illustrated in Fig. 4.1-11. Here a dummy MOS transistor *MD* (with source and drain both attached to the signal line and the gate attached to the inverse clock) is used to apply an opposing clock feedthrough due to M1. The area of *MD* can be designed to provide

minimum clock feedthrough. Unfortunately, this method never completely removes the feedthrough and in some cases may worsen it. Also it is necessary to generate an inverted clock, which is applied to the dummy switch. Clock feedthrough can be reduced by using the largest capacitors possible, using minimum-geometry switches, and keeping the clock swings as small as possible. Typically, these solutions will create problems in other areas, requiring some compromises.

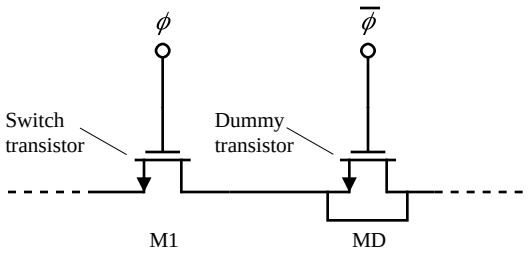


Figure 4.1-11 The use of a dummy transistor to cancel clock feedthrough.

The dynamic range limitations associated with single-channel MOS switches can be avoided with the CMOS switch shown in Fig. 4.1-12. Using CMOS technology, a switch is usually constructed by connecting p-channel and n-channel enhancement transistors in parallel as illustrated. For this configuration, when ϕ is low, both transistors are off, creating an effective open circuit. When ϕ is high, both transistors are on, giving a low-impedance state. The bulk potentials of the p-channel and the n-channel devices are taken to the highest and lowest potentials, respectively.

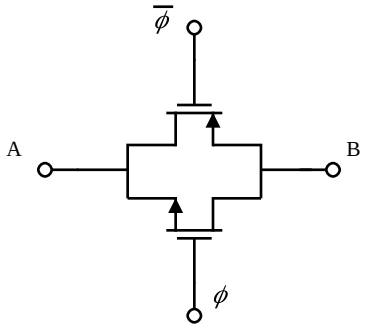


Figure 4.1-12 A CMOS switch

The primary advantage of the CMOS switch over the single-channel MOS switch is that the dynamic analog-signal range in the ON state is greatly increased.

The increased dynamic range of the analog signal is evident in Fig. 4.1-13 where the on resistance of a CMOS switch is plotted as a function of the input voltage. In this figure, the p-channel and n-channel devices are sized in such a way so that they have equivalent resistance with identical terminal conditions. The double-peak behavior is due to the n-channel device dominating when v_{in} is low and the p-channel dominating when v_{in} is high (near V_{DD}). At the mid range (near V_{DD} /2), the parallel combination of the two devices results in a minima.

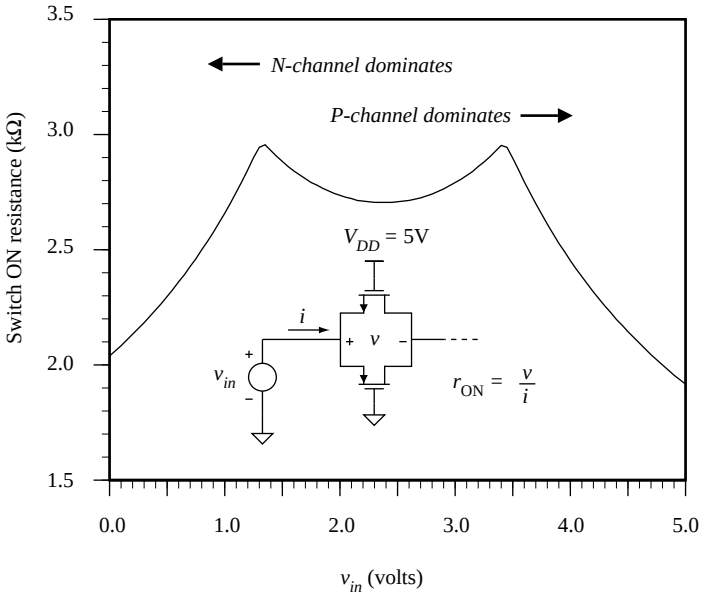


Figure 4.1-13 r_{ON} of Fig 4.1-12 as a function of the voltage v_{in}.

In this section we have seen that MOS transistors make one of the best switch realizations available in integrated-circuit form. They require small area, dissipate very little power, and provide reasonable values of r_{ON} and r_{OFF} for most applications. The inclusion of a good realization of a switch into the designer's basic building blocks will produce some interesting and useful circuits and systems which will be studied in the following chapters.

4.2 MOS Diode/Active Resistor

When the gate and drain of an MOS transistor are tied together as illustrated in Fig. 4.2-1(a) and (b), the *I-V* characteristics are qualitatively similar to a pn-junction diode, thus the name *MOS diode*. The MOS diode is used as a component of a current mirror (Sec. 4.4) and for level translation (voltage drop).

The I-V characteristics of the MOS diode are illustrated in Fig. 4.2-1(c) and described by the large-signal equation for drain current in saturation (the connection of the gate to the drain guarantees operation in the saturation region) shown below.

$$I = I_D = \left(\frac{K'W}{2L}\right)[(V_{GS} - V_T)^2] = \frac{\beta}{2}(V_{GS} - V_T)^2 \qquad (1)$$

or

$$V = V_{GS} = V_{DS} = V_T + \sqrt{2I_D/\beta} \qquad (2)$$

If V or I is given, then the remaining variable can be designed using either Eq. (1) or Eq. (2) and solving for the value of β.

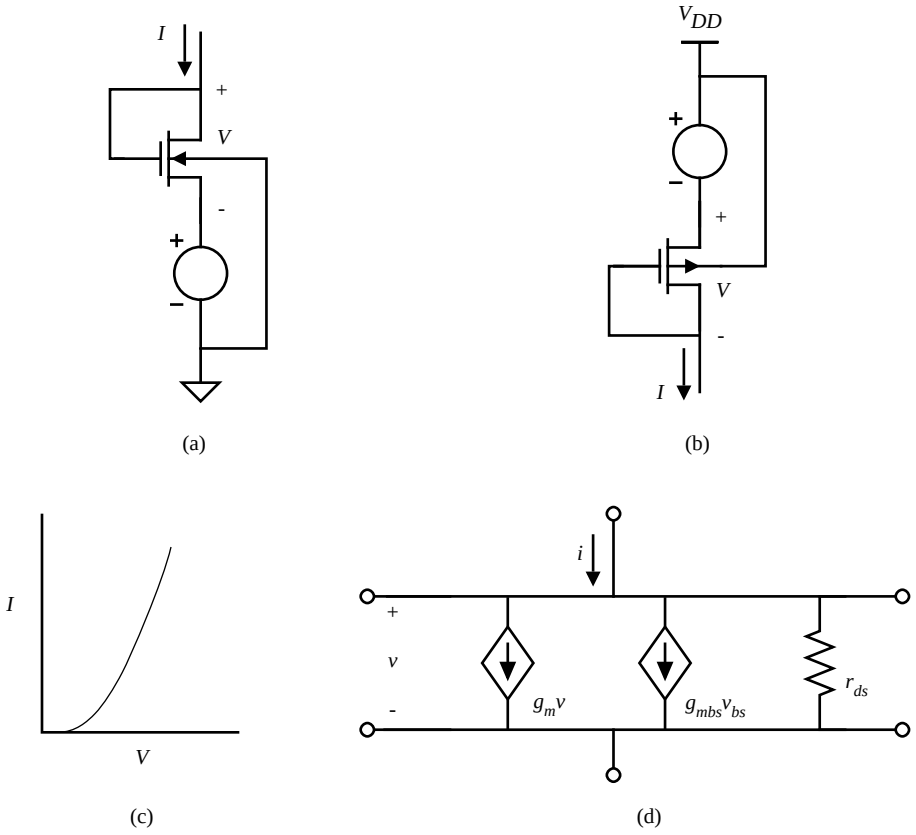


Figure 4.2-1 Active resistor. (a) N-channel. (b) P-channel. (c) I-V characteristics for n-channel case. (d) Small-signal model.

Connecting the gate to the drain means that v_{DS} controls i_D and therefore the channel transconductance becomes a channel conductance. The small-signal model of an MOS diode (excluding capacitors) is shown in Fig. 4.2-1(d). It is easily seen that the small-signal resistance of an MOS diode is

$$r_{\text{out}} = \frac{1}{g_m + g_{mbs} + g_{ds}} \cong \frac{1}{g_m} \tag{3}$$

where g_m is greater than g_{mbs} or g_{ds}.

An illustration of the application of the MOS diode is shown in Fig. 4.2-2 where a bias voltage is generated with respect to ground (the value of such a circuit will become obvious later). Noting that $V_{DS} = V_{GS}$ for both devices,

$$V_{DS} = \sqrt{\frac{2I}{\beta}} + V_T = V_{ON} + V_T \tag{4}$$

$$V_{BIAS} = V_{DS1} + V_{DS2} = 2V_{ON} + 2V_T \tag{5}$$

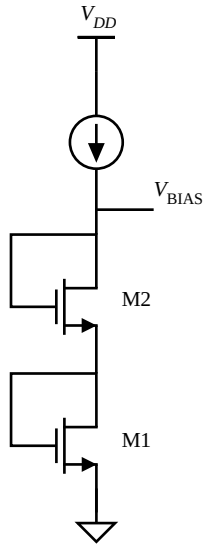


Figure 4.2-2 Voltage division using active resistors.

The MOS switch described in Sec 4.1 and illustrated in Fig. 4.1-2 can be viewed as a resistor, albeit rather nonlinear as illustrated in Fig. 4.1-4. The nonlinearity can be mitigated where the drain and source voltages vary over a small range so that the transistor ON resistance can be approximated as small signal resistance. Figure 4.2-3 illustrates this point showing a configuration where the transistor's drain and source form the two ends of a "floating" resistor. For the small-signal premise to be valid, v_{DS} is assumed small. The *I-V* characteristics of the floating resistor are given by Fig. 4.1-3. Consequently, the range of resistance values is large but nonlinear. When the transistor is operated in the nonsaturation region, the resistance can be calculated from Eq. (2) of Sec. 4.1 and repeated below, where v_{DS} is assumed small.

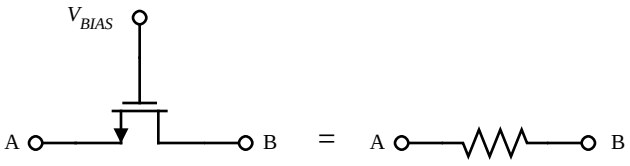


Figure 4.2-3 Floating active resistor using a single MOS transistor.

$$r_{ds} = \frac{L}{K'W(V_{GS} - V_T)} \tag{6}$$

Example 4.2-1 Calculation of the Resistance of an Active Resistor

The floating active resistor of Fig. 4.2-3 is to be used to design a 1 kΩ resistance. The dc value of $V_{A,B} = 2$ V. Use the device parameters in Table 3.1-2 and assume the active resistor is an n-channel transistor with the gate voltage at 5 V. Assume that

V_{DS} = 0.0. Calculate the required *W/L* to achieve 1 kΩ resistance. The bulk terminal is 0.0 V.

Before applying Eq. (6), it is necessary to calculate the new threshold voltage, V_T, due to V_{BS} not being zero ($|V_{BS}|$ = 2 V). From Eq. (2) of Sec. 3.1 the new V_T is found to be 1.022 volts. Equating Eq. (5) to 1000 Ω gives a *W/L* of 4.597 ≅ 4.6.

4.3 Current Sinks and Sources

A current sink and current source are two terminal components whose current at any instant of time is independent of the voltage across their terminals. The current of a current sink or source flows from the positive node, through the sink or source to the negative node. A current sink typically has the negative node at V_{SS} and the current source has the positive node at V_{DD}. Figure 4.3-1 (a) shows the MOS implementation of a current sink. The gate is taken to whatever voltage necessary to create the desired value of current. The voltage divider of Fig. 4.2-2 can be used to provide this voltage. We note that in the nonsaturation region the MOS device is not a good current source. In fact the voltage across the current sink must be larger than V_{MIN} in order for the current sink to perform properly. For Fig. 4.3-1(a) this means that

$$v_{\text{OUT}} \geq V_{GG} - V_{T0} - V_{SS} \tag{1}$$

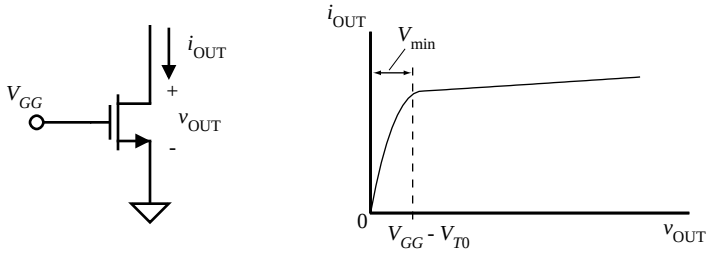


Figure 4.3-1 (a) Current sink. (b) Current-voltage characteristics of (a).

If the gate-source voltage is held constant, then the large-signal characteristics of the MOS transistor are given by the output characteristics of Fig. 3.1-3. An example is shown in Fig. 4.3-1 (b). If the source and bulk are both connected to V_{SS}, then the small-signal output resistance is given by (see Eq. (9) of Sec. 3.3)

$$r_{\text{out}} = \frac{1 + \lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D} \tag{2}$$

If the source and bulk are not connected to the same potential, the characteristics will not change as long as V_{BS} is a constant.

Figure 4.3-2 (a) shows an implementation of a current source using a p-channel transistor. Again, the gate is taken to a constant potential as is the source. With the definition of v_{OUT} and i_{OUT} of the source as shown in Fig. 4.3-2(a), the large-signal *V-I* characteristic is shown in Fig. 4.3-2(b). The small-signal output resistance of the current source is given by Eq. (2). The source-drain voltage must be larger than V_{MIN} for this current source to work properly. This current source only works for values of v_{OUT} given by

$$v_{\text{OUT}} \leq V_{GG} + |V_{T0}| \tag{3}$$

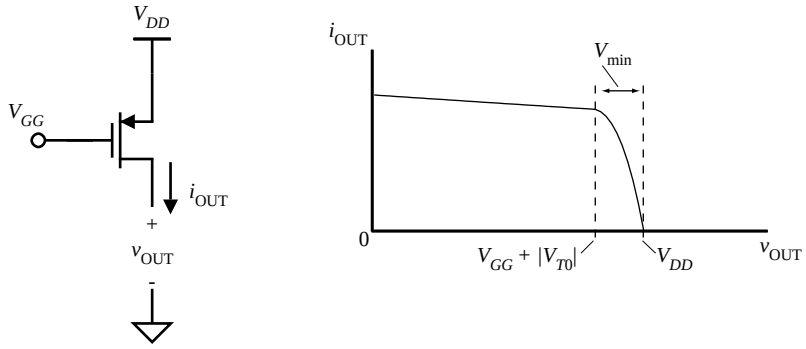


Figure 4.3-2 (a) Current source. (b) Current-voltage characteristics of (a).

The advantage of the current sink and source of Figs. 4.3-1(a) and 4.3-2(a) is their simplicity. However, there are two areas in which their performance may need to be improved for certain applications. One improvement is to increase the small-signal output resistance—resulting in a more constant current over the range of v_{OUT} values. The second is to reduce the value of V_{MIN}, thus allowing a larger range of v_{OUT} over which the current sink/source works properly. We shall illustrate methods to improve both areas of performance. First, the small-signal output resistance can be increased using the principle illustrated in Fig. 4.3-3(a). This principle uses the common-gate configuration to multiply the source resistance r by the approximate voltage gain of the common-gate configuration with an infinite load resistance. The exact small-signal output resistance r_{out} can be calculated from the small-signal model of Fig. 4.3-3(b) as

$$r_{\text{out}} = \frac{v_{\text{out}}}{i_{\text{out}}} = r + r_{ds2} + [(g_{m2} + g_{mbs2})r_{ds2}]r \cong (g_{m2}r_{ds2})r \tag{4}$$

where $g_{m2}r_{ds2} >> 1$ and $g_{m2} > g_{mbs2}$.

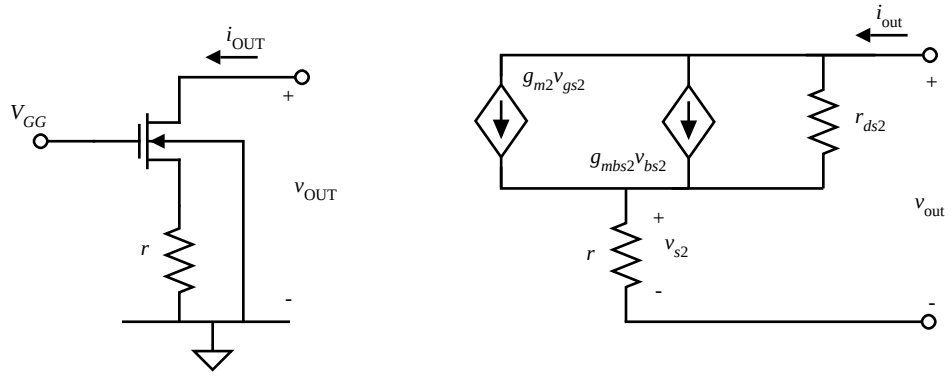


Figure 4.3-3 (a) Technique for increasing the output resistance of a resistor r. (b) Small-signal model for the circuit in (a).

The above principle is implemented in Fig. 4.3-4(a) where the output resistance (r_{ds1}) of the current sink of Fig. 4.3-1(a) should be increased by the common-gate voltage gain of M2. To verify the principle, the small-signal output resistance of the cascode current sink of Fig. 4.3-4(a) will be calculated using the model of Fig. 4.3-4(b). Since $v_{gs2} = -v_1$ and $v_{gs1} = 0$, summing the currents at the output node gives

$$i_{\text{out}} + g_{m2}v_1 + g_{mbs2}v_1 = g_{ds2}(v_{\text{out}} - v_1) \tag{5}$$

Since $v_1 = i_{\text{out}}r_{ds1}$, we can solve for r_{out} as

$$r_{\text{out}} = \frac{v_{\text{out}}}{i_{\text{out}}} = r_{ds2}(1 + g_{m2}r_{ds1} + g_{mbs2}r_{ds1} + g_{ds2}r_{ds1}) \tag{6}$$

$$= r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2}(1 + \eta_2)$$

Typically, $g_{m2}r_{ds2}$ is greater than unity so that Eq. (6) simplifies to

$$r_{\text{out}} \cong (g_{m2}r_{ds2})r_{ds1} \tag{7}$$

We see that the small-signal output resistance of the current sink of Fig. 4.3-4(a) is increased by the factor of $g_{m2}r_{ds2}$.

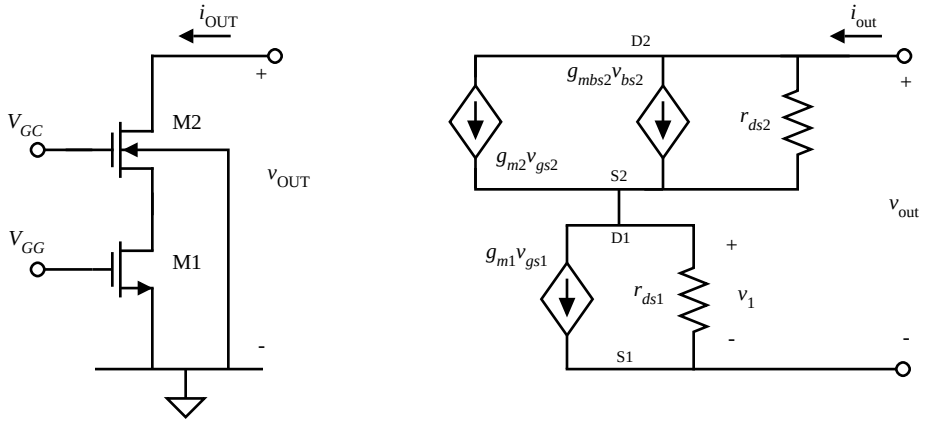


Figure 4.3-4 (a) Circuit for increasing r_{out} of a current sink. (b) Small-signal model for the circuit in (a).

Example 4.3-1 Calculation of Output Resistance for a Current Sink

Use the model parameters of Table 3.1-2 to calculate: (a) the small-signal output resistance for the simple current sink of Fig. 4.3-1(a) if $I_{\text{OUT}} = 100\ \mu$A; and (b) the small-signal output resistance if the simple current sink of (a) is inserted into the cascode current-sink configuration of Fig. 4.3-4(a). Assume that $W_1/L_1 = W_2/L_2 = 1$.

(a) Using $\lambda = 0.04$ and $I_{\text{OUT}} = 100\ \mu$A gives a small-signal output resistance of 250 kΩ. (b) The body-effect term, g_{mbs2} can be ignored with little error in the result. Equation (6) of Sec. 3.3 gives $g_{m1} = g_{m2} = 148\ \mu$A/V. Substituting these values into Eq. (7) gives the small-signal output resistance of the cascode current sink as 9.25 MΩ.

The other performance limitation of the simple current sink/source was the fact that the constant output current could not be obtained for all values of v_{OUT}. This was illustrated in Figs. 4.3-1(b) and 4.3-2(b). While this problem may not be serious in the simple current sink/source, it becomes more severe in the cascode current-sink/source configuration that was used to increase the small-signal output resistance. It therefore becomes necessary to examine methods of reducing the value of V_{MIN} [3] Obviously, V_{MIN} can be reduced by increasing the value of W/L and adjusting the gate-source

voltage to get the same output current. However, another method which works well for the cascode current-sink/source configuration will be presented.

We must introduce an important principle used in biasing MOS devices before showing the method of reducing V_{MIN} of the cascode current sink/source. This principle can be best illustrated by considering two MOS devices, M1 and M2. Assume that the applied dc gate-source voltage V_{GS} can be divided into two parts, given as

$$V_{GS} = V_{ON} + V_T \tag{8}$$

where V_{ON} is that part of V_{GS} which is in excess of the threshold voltage, V_T. This definition allows us to express the minimum value of v_{DS} for which the device will remain in saturation as

$$v_{DS}(\text{sat}) = V_{GS} - V_{\text{T}} = V_{ON} \tag{9}$$

Thus, V_{ON} can be thought of as the minimum drain-source voltage for which the device remains saturated. In saturation, the drain current can be written as

$$i_D = \frac{K'W}{2L}(V_{ON})^2 \tag{10}$$

The principle to be illustrated is based upon Eq. (10). If the currents of two MOS devices are equal (because they are in series), then the following relationship holds.

$$\frac{K'_1 W_1}{L_1}(V_{ON1})^2 = \frac{K'_2 W_2}{L_2}(V_{ON2})^2 \tag{11}$$

If both MOS transistors are of the same type, then Eq. (11) reduces to

$$\frac{W_1}{L_1}(V_{ON1})^2 = \frac{W_2}{L_2}(V_{ON2})^2 \tag{12}$$

or

$$\frac{\left(\frac{W_1}{L_1}\right)}{\left(\frac{W_2}{L_2}\right)} = \frac{(V_{ON2})^2}{(V_{ON1})^2} \tag{13}$$

The principle above can also be used to define a relationship between the current and W/L ratios. If the gate-source voltages of two similar MOS devices are equal (because they are physically connected), then V_{ON1} is equal to V_{ON2}. From Eq. (10) we can write

$$i_{D1}\left(\frac{W_2}{L_2}\right) = i_{D2}\left(\frac{W_1}{L_1}\right) \tag{14}$$

Eq. (13) is useful even though the gate-source terminals of M1 and M2 may not be physically connected because voltages can be identical without being physically connected as will be seen in later material. Eq's. (13) and (14) represent a very important principle that will be used not only in the material immediately following but throughout this text to determine biasing relationships.

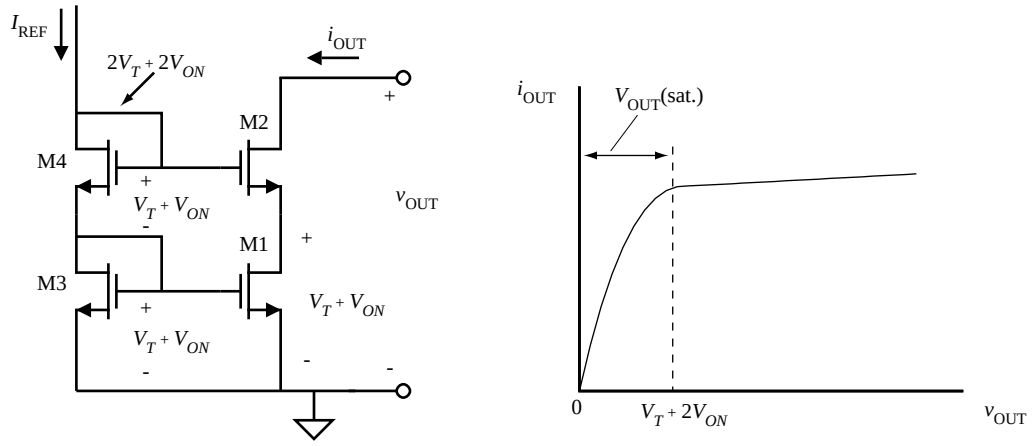


Figure 4.3-5 (a) Standard cascode current sink. (b) Output characteristics of circuit in (a).

Consider the cascode current sink of Fig. 4.3-5(a). Our objective is to use the above principle to reduce the value of V_{MIN} [=V_{OUT}(sat)]. If we ignore the bulk effects on M2 and M4 and assume that M1, M2, M3, and M4 are all matched with identical W/L ratios, then the gate-source voltage of each transistor can be expressed as $V_T + V_{ON}$ as shown in Fig. 4.3-5(a). At the gate of M2 we see that the voltage with respect to the lower power supply is $2V_T + 2V_{ON}$. In order to maintain current-sink/source operation, it will be assumed that M1 and M2 must have at least a voltage of V_{ON} as given in Eq. (9). In order to find V_{MIN} [=V_{OUT}(sat)] of Fig. 4.3-5(a) we can rewrite Eq. (10) of Sec. 3.1 as

$$v_D \geq v_G - V_T \tag{15}$$

Since $V_{G2} = 2V_T + 2V_{ON}$, substituting this value into Eq. (15) gives

$$V_{D2}(\text{min}) = V_{\text{MIN}} = V_T + 2V_{ON} \tag{16}$$

The current-voltage characteristics of Fig. 4.3-5(a) are illustrated in Fig. 4.3-5(b) where the value of V_{MIN} of Eq. (16) is shown.

V_{MIN} of Eq. (16) is dropped across both M1 and M2. The drop across M2 is V_{ON} while the drop across M1 is $V_T + V_{ON}$. From the results of Eq. (9), this implies that V_{MIN} of Fig. 4.3-5 could be reduced by V_T and still keep both M1 and M2 in saturation. Figure 4.3-6(a) shows how this can be accomplished[12]. The W/L ratio of M4 is made 1/4 of the identical W/L ratios of M1 through M3. This causes the gate-source voltage across M4 to be $V_T + 2V_{ON}$ rather than $V_T + V_{ON}$. Consequently, the voltage at the gate of M2 is now $V_T + 2V_{ON}$. Substituting this value into Eq. (15) gives

$$V_{D2}(\text{min}) = V_{\text{MIN}} = 2V_{ON} \tag{17}$$

The resulting current-voltage relationship is shown in Fig. 4.3-6(b). It can be seen that a voltage of $2V_{ON}$ is across both M1 and M2 giving the lowest value of V_{MIN} and still keeping both M1 and M2 in saturation. Using this approach and increasing the W/L ratios will result in minimum values of V_{MIN}.

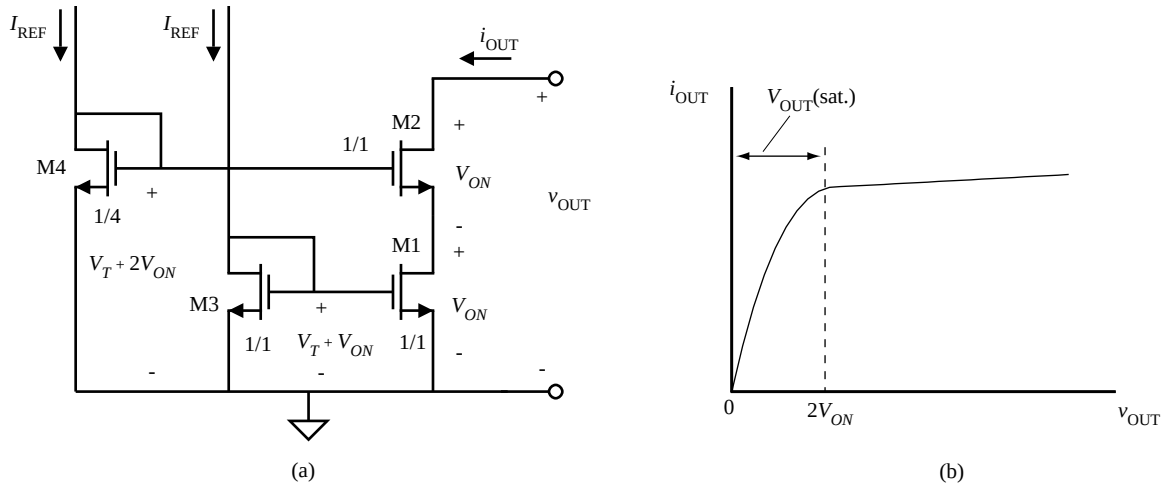


Figure 4.3-6 (a) High-swing cascode. (b) Output characteristics of circuit in (a).

Example 4.3-2 Designing the Cascode Current Sink for a Given V_{MIN}

Use the cascode current-sink configuration of Fig. 4.3-6(a) to design a current sink of 100 μA and a V_{MIN} of 1 V. Assume the device parameters of Table 3.1-2. With V_{MIN} of 1 V, choose $V_{ON} = 0.5$ V. Using the saturation model, the *W*/*L* ratio of M1 through M3 can be found from

$$\frac{W}{L} = \frac{2\, i_{OUT}}{K'\, V_{ON}^2} = \frac{2 \times 100 \times 10^{-6}}{110 \times 10^{-6} \times 0.25} = 7.27$$

The *W* /*L* ratio of M4 will be 1/4 this value or 1.82.

A problem exists with the circuit in Fig. 4.3-6. The V_{DS} of M1 and the V_{DS} of M3 are not equal. Therefore, the current i_{OUT} will not be an accurate replica of I_{REF} due to channel-length modulation as well as drain-induced threshold shift. If precise mirroring of the current I_{REF} to I_{out} is desired, a slight modification of the circuit of Fig. 4.3-6 will minimize this problem. Figure 4.3-7 illustrates this fix. An additional transistor, M5, is added in series with M3 so as to force the drain voltages of M3 and M1 to be equal, thus eliminating and errors due to channel-length modulation and drain-induced threshold shift.

The above technique will be useful in maximizing the voltage-signal swings of cascode configurations to be studied later. This section has presented implementations of the current sink/source and has shown how to boost the output resistance of a MOS device. A very important principle that will be used in biasing was based on relationships between the excess gate-source voltage V_{ON}, the drain current, and the *W*/*L* ratios of MOS devices. This principle was applied to reduce the voltage V_{MIN} of the cascode current source.

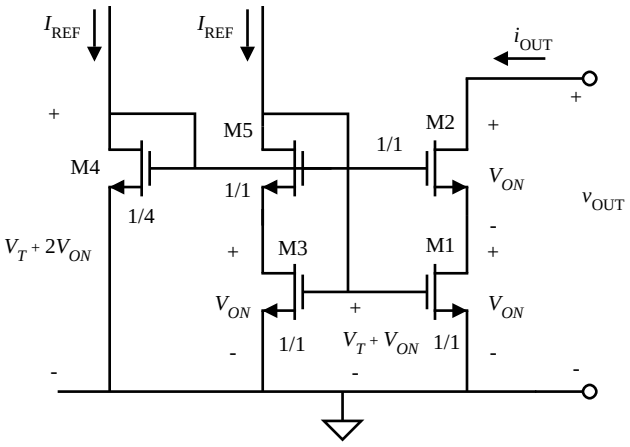


Figure 4.3-7 Improved high-swing cascode.

When power dissipation must be kept at a minimum, the circuit in Fig. 4.3-7 can be modified to eliminate one of the I_{REF} currents. Figure 4.3-8 illustrates a self-biased cascode current source that requires only one reference current[4].

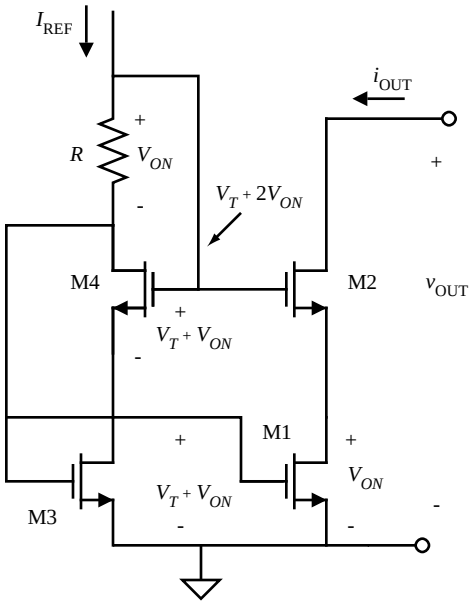


Figure 4.3-8 Self-biased high-swing cascode current source.

Example 4.3-3 Designing the Self-Biased High-Swing Cascode Current Sink for a Given V_{MIN}

Use the cascode current-sink configuration of Fig. 4.3-8 to design a current sink of 250 μA and a V_{MIN} of 0.5 V. Assume the device parameters of Table 3.1-2. With V_{MIN} of 0.5 V, choose $V_{ON} = 0.25$ V. Using the saturation model, the *W/L* ratio of M1 and M3 can be found from

$$\frac{W}{L} = \frac{2\, i_{OUT}}{K'\, V_{ON}^2} = \frac{2 \times 500 \times 10^{-6}}{110 \times 10^{-6} \times 0.0625} = 72.73$$

The back-gate bias on M2 and M4 is −0.25 V. Therefore, the threshold voltage for M2 and M4 is calculated to be

$$V_{TH} = 0.7 + 0.4\left[\sqrt{0.25 + 0.7} - \sqrt{0.7}\right] = 0.755$$

Taking into account the increased value of the threshold voltage, the gate voltage of M4 and M2 is

$$V_{G4} = 0.755 + 0.25 + 0.25 \quad = 1.255$$

The gate voltage of M1 and M3 is

$$V_{G1} = 0.70 + 0.25 = 0.95$$

Both terminals of the resistor are now defined so that the required resistance value is easily calculated to be

$$R \quad = \frac{V_{G4} - V_{G1}}{250 \times 10^{-6}} = \frac{1.255 - 0.95}{250 \times 10^{-6}} \quad = 1220\ \Omega$$

4.4 Current Mirrors

Current mirrors are simply an extension of the current sink/source of the previous section. In fact, it is unlikely that one would ever build a current sink/source that was not biased as a current mirror. The current mirror uses the principle that if the gate-source potential of two identical MOS transistors are equal, the channel currents should be equal. Figure 4.4-1 shows the implementation of a simple n-channel current mirror. The current i_I is assumed to be defined by a current source or some other means and i_O is the output or "mirrored" current. M1 is in saturation because $v_{DS1} = v_{GS1}$. Assuming that $v_{DS2} \geq v_{GS} - V_{T2}$ is greater than V_{T2} allows us to use the equations in the saturation region of the MOS transistor. In the most general case, the ratio of i_O to i_I is

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}}\right)^2 \left[\frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}\left(\frac{K'_2}{K'_1}\right)\right] \tag{1}$$

Normally, the components of a current mirror are processed on the same integrated circuit and thus all of the physical parameters such as V_T, K', etc., are identical for both devices. As a result, Eq. (1) simplifies to

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}\right) \tag{2}$$

If $v_{DS2} = v_{DS1}$ (not always a good assumption), then the ratio of i_O/i_I becomes

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right) \tag{3}$$

Consequently, i_O/i_I is a function of the aspect ratios that are under the control of the designer.

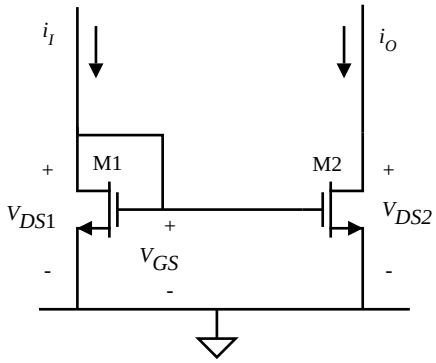


Figure 4.4-1 N-channel current mirror.

There are three effects that cause the current mirror to be different than the ideal situation of Eq. (3). These effects are: (1) channel-length modulation, (2) threshold offset between the two transistors, and (3) imperfect geometrical matching. Each of these effects will be analyzed separately.

Consider the channel-length modulation effect. Assuming all other aspects of the transistor are ideal and the aspect ratios of the two transistors are both unity, then Eq. (2) simplifies to

$$\frac{i_O}{i_I} = \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}} \tag{4}$$

with the assumption that λ is the same for both transistors. This equation shows that differences in drain-source voltages of the two transistors can cause a deviation for the ideal unity current gain or current mirroring. Figure 4.4-2 shows a plot of current ratio error versus $v_{DS2} - v_{DS1}$ for different values of λ with both transistors in the saturation region. Two important facts should be recognized from this plot. The first is that significant ratio error can exist when the mirror transistors do not have the same drain-source voltage and secondly, for a given difference in drain-source voltages, the ratio of the mirror current to the reference current improves as λ becomes smaller (output resistance becomes larger). Thus, a good current mirror or current amplifier should have identical drain-source voltages and a high output resistance.

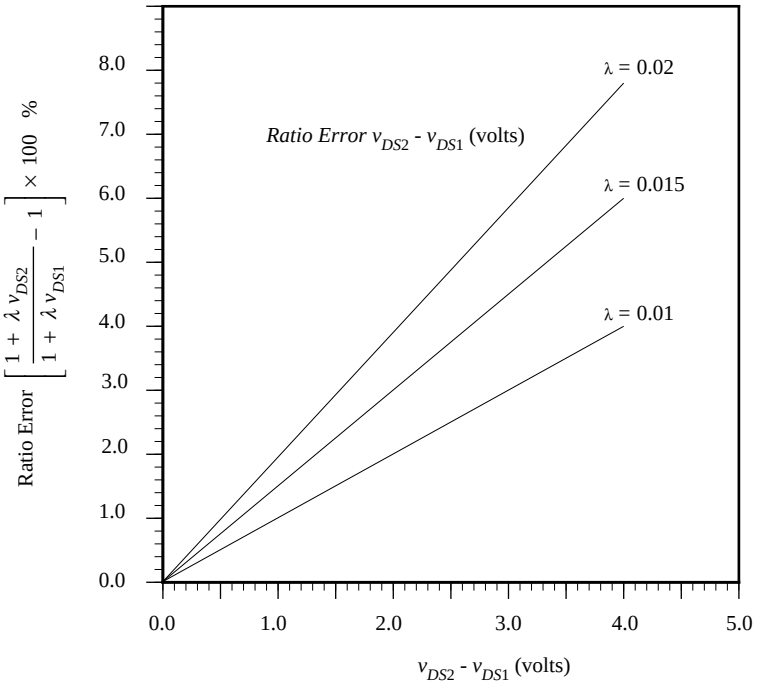


Figure 4.4-2 Plot of ratio error (in %) versus drain voltage difference for the current mirror of Fig. 4.4-1. For this plot, v_{DS1} = 2.0 volts.

The second nonideal effect is that of offset between the threshold voltage of the two transistors. For clean silicon-gate CMOS processes, the threshold offset is typically less than 10 mV for transistors that are identical and in close proximity to one another. Consider two transistors in a mirror configuration where both have the same drain-source voltage and all other aspects of the transistors are identical except V_T. In this case, Eq. (1) simplifies to

$$\frac{i_O}{i_I} = \left(\frac{v_{GS} - V_{T2}}{v_{GS} - V_{T1}}\right)^2 \tag{5}$$

Figure 4.4-3 shows a plot of the ratio error versus ΔV_T where $\Delta V_T = V_{T1} - V_{T2}$. It is obvious from this graph that better current-mirror performance is obtained at higher currents, because v_{GS} is higher for higher currents and thus ΔV_T becomes a smaller percentage of v_{GS}.

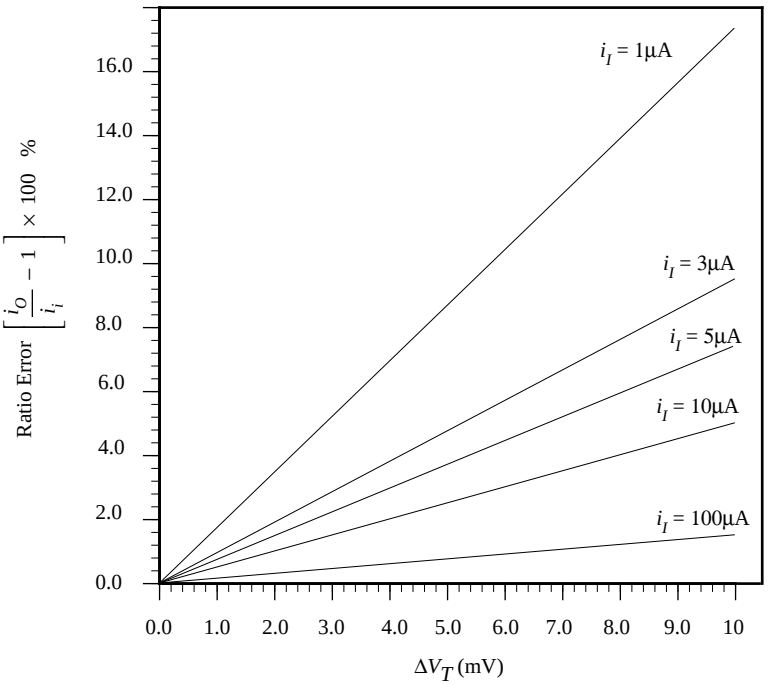


Figure 4.4-3 Plot of ratio error (in %) versus offset voltage for the current mirror of Fig. 4.4-1. For this plot, v_{T1} = 0.7 volts, K'W/L = 110µA/V^2

It is also possible that the transconductance gain K' of the current mirror is also mismatched (due to oxide gradients). A quantitative analysis approach to variations in both K' and V_T is now given. Let us assume that the W/L ratios of the two mirror devices are exactly equal but that K' and V_T may be mismatched. Eq. (5) can be rewritten as

$$\frac{i_O}{i_I} = \frac{K'_2(v_{GS} - V_{T2})^2}{K'_1(v_{GS} - V_{T1})^2} \tag{6}$$

where $v_{GS1} = v_{GS2} = v_{GS}$. Defining $\Delta K' = K'_2 - K'_1$ and $K' = 0.5(K'_2 + K'_1)$ and $\Delta V_T = V_{T2} - V_{T1}$ and $V_T = 0.5(V_{T2} + V_{T1})$ gives

$$K'_1 = K' - 0.5\Delta K' \tag{7}$$

$$K'_2 = K' + 0.5\Delta K' \tag{8}$$

$$V_{T1} = V_T - 0.5\Delta V_T \tag{9}$$

$$V_{T2} = V_T + 0.5\Delta V_T \tag{10}$$

Substituting Eq's. (7) through (10) into Eq. (6) gives

$$\frac{i_O}{i_I} = \frac{(K' + 0.5\Delta K')(v_{GS} - V_T - 0.5\Delta V_T)^2}{(K' - 0.5\Delta K')(v_{GS} - V_T + 0.5\Delta V_T)^2} \tag{11}$$

Factoring out K' and $(v_{GS} - V_T)$ gives

$$\frac{i_O}{i_I} = \frac{\left(1 + \frac{\Delta K'}{2K}\right)\left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2}{\left(1 - \frac{\Delta K'}{2K}\right)\left(1 + \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2} \tag{12}$$

Assuming that the quantities in Eq. (12) following the "1" are small, Eq. (12) can be approximated as

$$\frac{i_O}{i_I} \cong \left(1 + \frac{\Delta K'}{2K'}\right)\left(1 + \frac{\Delta K'}{2K'}\right)\left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2 \left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2 \tag{13}$$

Retaining only first order products gives

$$\frac{i_O}{i_I} \cong 1 + \frac{\Delta K'}{K'} - \frac{2\Delta V_T}{(v_{GS} - V_T)} \tag{14}$$

If the percentage change of K' and V_T are known, Eq. (14) can be used on a worst-case basis to predict the error in the current-mirror gain. For example, assume that $\Delta K'/K' = \pm 5\%$ and $\Delta V_T/(v_{GS} - V_T) = \pm 10\%$. Then the current-mirror gain would be given as $i_O/i_I \cong 1 \pm 0.05 \pm (-0.20)$ or $1 \pm (-0.15)$ amounting to a 15% error in gain.

The third nonideal effect of current mirrors is the error in the aspect ratio of the two devices. We saw in Chapter 3 that there are differences in the drawn values of W and L. These are due to mask, photolithographic, etch, and out-diffusion variations. These variations can be different even for two transistors placed side by side. One way to avoid the effects of these variations is to make the dimensions of the transistors much larger than the typical variation one might see. For transistors of identical size with W and L greater than 10 μm, the errors due to geometrical mismatch will generally be insignificant compared to offset-voltage and v_{DS}-induced errors.

In some applications, the current mirror is used to multiply current and function as a current amplifier. In this case, the aspect ratio of the multiplier transistor (M2) is much greater than the aspect ratio of the reference transistor (M1). To obtain the best performance, the geometrical aspects must be considered. An example will illustrate this concept.

Example 4.4-1 Aspect Ratio Errors in Current Amplifiers

Figure 4.4-4 shows the layout of a one-to-four current amplifier. Assume that the lengths are identical ($L_1 = L_2$) and find the ratio error if $W_1 = 5 \pm 0.05$ μm. The actual widths of the two transistors are

$$W_1 = 5 \pm 0.05 \ \mu\text{m}$$

and

$$W_2 = 20 \pm 0.05 \ \mu\text{m}$$

We note that the tolerance is not multiplied by the nominal gain factor of 5. The ratio of W_2 to W_1 and consequently the gain of the current amplifier is

$$\frac{i_O}{i_I} = \frac{W_2}{W_1} = \frac{20 \pm 0.05}{5 \pm 0.05} = 4 \pm 0.05$$

where we have assumed that the variations would both have the same sign. It is seen that this ratio error is 1.25% of the desired current ratio or gain.

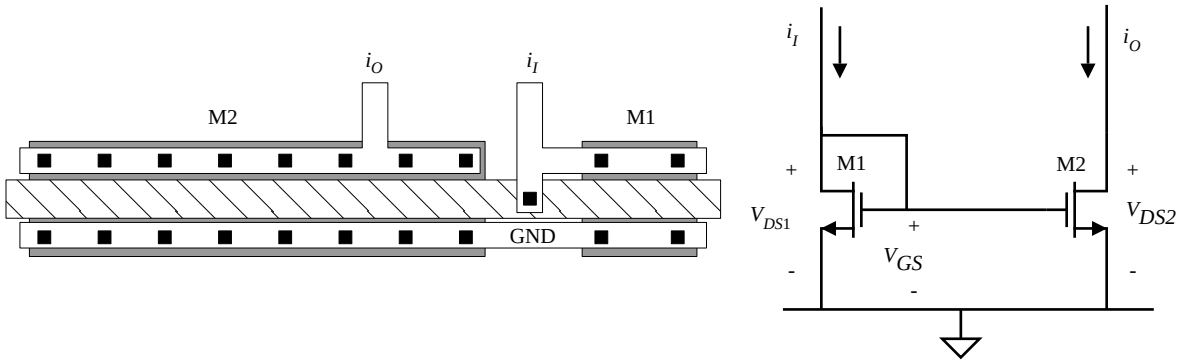


Figure 4.4-4 Layout of current mirror without ΔW correction.

The error noted above would be valid if every other aspect of the transistor were matched perfectly. A solution to this problem can be achieved by using proper layout techniques. The correct one-to-five ratio should be implemented using five duplicates of the transistor M1. In this way, the tolerance on W_2 is multiplied by the nominal current gain. Let us reconsider the above example using this approach.

Example 4.4-2 Reduction of the Aspect Ratio Error in Current Amplifiers

Use the layout technique illustrated in Fig. 4.4-5 and calculate the ratio error of a current amplifier having the specifications of the previous example.
The actual widths of M1 and M2 are

$$W_1 = 5 \pm 0.05\ \mu\text{m}$$

and

$$W_2 = 4(5 \pm 0.05)\ \mu\text{m}$$

The ratio of W_2 to W_1 and consequently the current gain is seen to be

$$\frac{i_O}{i_I} = \frac{4(5 \pm 0.05)}{5 \pm 0.05} = 4$$

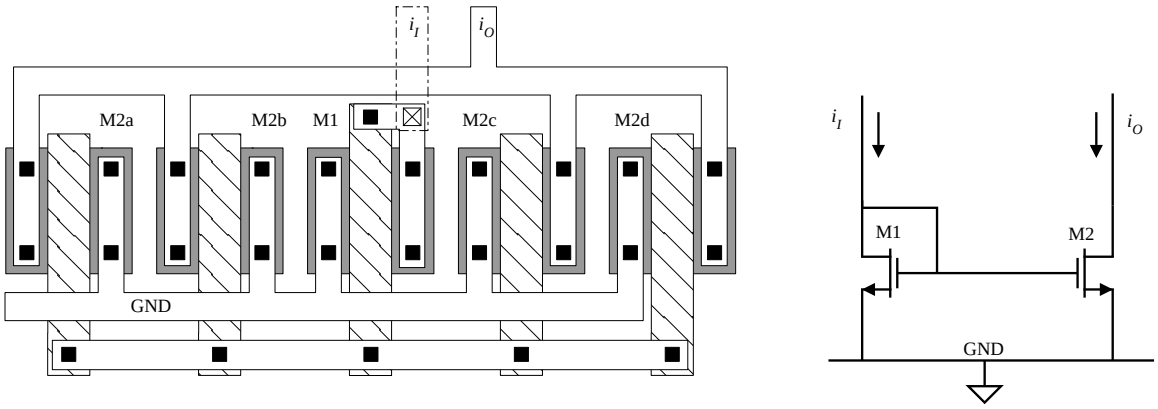


Figure 4.4-5 Layout of current mirror with ΔW correction as well as common centroid layout techniques.

In the above examples we made the assumption that ΔW should be the same for all transistors. Unfortunately this is not true, but the ΔW matching errors will be small compared to the other error contributions. If the widths of two transistors are equal but the lengths differ, the scaling approach discussed above for the width is also applicable to the length. Usually one does not try to scale the length because the tolerances are greater than the width tolerances due to diffusion (out diffusion) under the polysilicon gate.

We have seen that the small-signal output resistance is a good measure of the perfection of the current mirror or amplifier. The output resistance of the simple n-channel mirror of Fig. 4.4-1 is given as

$$r_{\text{out}} = \frac{1}{g_{ds}} \cong \frac{1}{\lambda I_D} \tag{15}$$

Higher-performance current mirrors will attempt to increase the value of r_{out}. Eq. (15) will be the point of comparison.

Up to this point we have discussed aspects of and improvements on the current mirror or current amplifier shown in Fig. 4.4-1, but there are ways of improving current mirror performance using the same principles employed in Section 4.3. The current mirror shown in Fig. 4.4-6, applies the cascode technique which reduces ratio errors due to differences in output and input voltage.

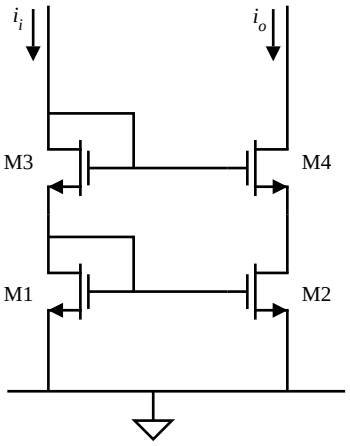


Figure 4.4-6 Standard cascode current sink.

Figure 4.4-7 shows an equivalent small-signal model of Fig. 4.4-6. Since $i_i = 0$, the small-signal voltages v_1 and v_3 are both zero. Therefore, Fig. 4.4-7 is exactly equivalent to the circuit of Example 4.3-1. Using the correct subscripts for Fig. 4.4-7, we can use the results of Eq. (6) of Sec. 4.3 to write

$$r_{\text{out}} = r_{ds2} + r_{ds4} + g_{m4}r_{ds2}r_{ds4}(1 + \eta_4) \tag{16}$$

We have already seen from Example 4.3-1 that the small-signal output resistance of this configuration is much larger than for the simple mirror of Eq. (15).

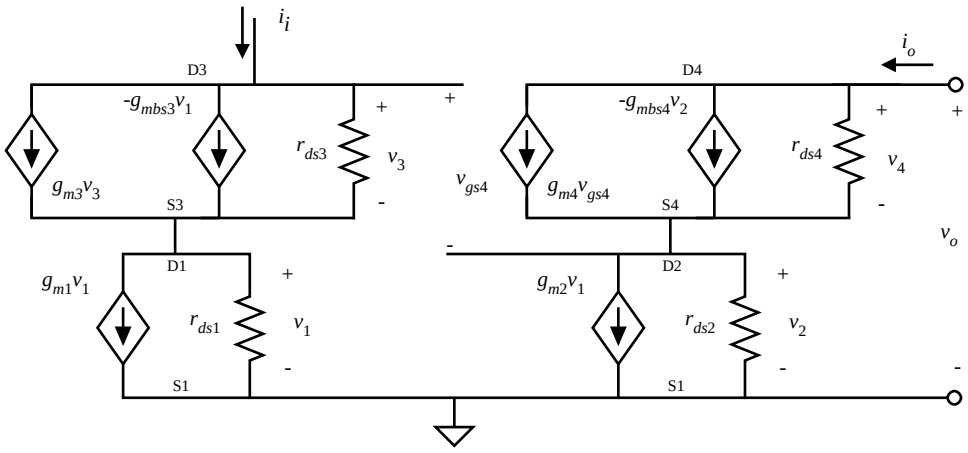


Figure 4.4-7 Small-signal model for the circuit of Fig. 4.4-6.

Another current mirror is shown in Fig. 4.4-8. This circuit is an n-channel implementation of the well-known Wilson current mirror [5]. The output resistance of the Wilson current mirror is increased through the use of negative, current feedback. If i_O increases, then the current through M2 also increases. However, the mirroring action of M1 and M2 causes the current in M1 to increase. If i_I is constant and if we assume there is some resistance from the gate of M3 (drain of M1) to ground, then the gate voltage of M3 is decreased if the current i_O increases. The loop gain is essentially the product of g_{m1} and the small signal resistance seen from the drain of M1 to ground.

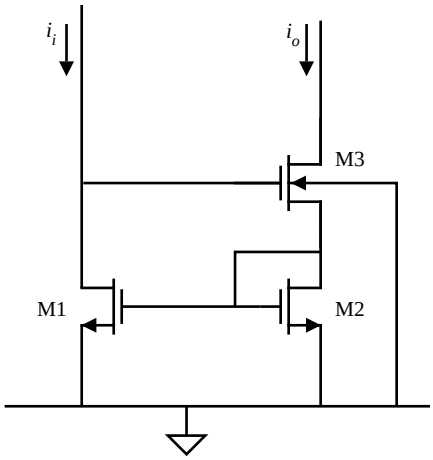


Figure 4.4-8 Wilson current mirror.

It can be shown that the small-signal output resistance of the Wilson current source of Fig. 4.4-8 is

$$r_{\text{out}} = r_{ds3} + r_{ds2}\left(\frac{1 + r_{ds3}g_{m3}(1 + \eta_3) + g_{m1}r_{ds1}g_{m3}r_{ds3}}{1 + g_{m2}r_{ds2}}\right) \tag{17}$$

The output resistance of Fig. 4.4-8 is seen to be comparable with that of Fig. 4.4-6.

Unfortunately, the behavior described above for the current mirrors or amplifier requires a non-zero voltage at the input and output before it is achieved. Consider the cascode current mirror of Fig. 4.4-6 from a large-signal viewpoint. This voltage at the input, designated as $V_I(\text{min})$, can be shown to depend upon the value of i_I as follows. Since $v_{DG} = 0$ for both M1 and M3, these devices are always in saturation. Therefore we may express $V_I(\text{min})$ as

$$V_I(\text{min}) = \left(\frac{2i_I}{K'}\right)^{1/2}\left[\left(\frac{L_1}{W_1}\right)^{1/2} + \left(\frac{L_3}{W_3}\right)^{1/2}\right] + (V_{T1} + V_{T3}) \tag{18}$$

It is seen that for a given i_I the only way to decrease $V_I(\text{min})$ is to increase the W/L ratios of both M1 and M3. One must also remember that V_{T3} will be larger due to the back gate bias on M3. The techniques used to reduce V_{MIN} of the cascode current-sink/source in Sec. 4.3 are not applicable here.

We are also interested in the voltage, $V_{\text{OUT}}(\text{sat})$, where M4 makes the transition from the nonsaturated region to the saturated region. This voltage can be found from the relationship

$$v_{DS4} \geq (v_{GS4} - V_{T4}) \tag{19}$$

or

$$v_{D4} \geq v_{G4} - V_{T4} \tag{20}$$

which is when M4 is on the threshold between the two regions. Equation (20) can be used to obtain the value of $V_{\text{OUT}}(\text{sat})$ as

$$V_{\text{OUT}}(\text{sat}) = V_I - V_{T4} = \left(\frac{2I_I}{K'}\right)^{1/2}\left[\left(\frac{L_1}{W_1}\right)^{1/2} + \left(\frac{L_3}{W_3}\right)^{1/2}\right] + (V_{T1} + V_{T3} - V_{T4}) \quad (21)$$

For voltages above $V_{\text{OUT}}(\text{sat})$, the transistor M4 is in saturation and the output resistance should be that calculated in Eq. (16). Since the value of voltage across M2 is greater than necessary for saturation, the technique used to decrease V_{MIN} in Sec. 5.3 can be used to decrease $V_{\text{OUT}}(\text{sat})$. Unfortunately, the value of $V_I(\text{min})$ will be increased.

Similar relationships can be developed for the Wilson current mirror or amplifier. If M3 is saturated, then $V_I(\text{min})$ is expressed as

$$V_I(\text{min}) = \left(\frac{2I_O}{K'}\right)^{1/2}\left[\left(\frac{L_2}{W_2}\right)^{1/2} + \left(\frac{L_3}{W_3}\right)^{1/2}\right] + (V_{T2} + V_{T3}) \quad (22)$$

For M3 to be saturated, v_{OUT} must be greater than $V_{\text{OUT}}(\text{sat})$ given as

$$V_{\text{OUT}}(\text{sat}) = V_I - V_{T3} = \left(\frac{2\,I_O}{K'}\right)^{1/2}\left[\left(\frac{L_2}{W_2}\right)^{1/2} + \left(\frac{L_3}{W_3}\right)^{1/2}\right] + V_{T2} \quad (23)$$

It is seen that both of these circuits require at least $2V_T$ across the input before they behave as described above. Larger W/L ratios will decrease $V_I(\text{min})$ and $V_{\text{OUT}}(\text{sat})$.

An improvement on the Wilson current mirror can be developed by viewing from a different perspective. Consider the Wilson current mirror redrawn in Fig. 4.4-9. Note that the resistance looking into the diode-connection of M2 is

$$r_{\text{M2}} = \frac{r_{ds2}}{1 + g_{m2}r_{ds2}} \quad (24)$$

If the gate of M2 is tied to a bias voltage so that r_{M2} becomes

$$r_{\text{M2}} = \frac{r_{ds2}}{1 + g_{m2}r_{ds2}} \qquad \Rightarrow \qquad r_{\text{M2}} = r_{ds2} \quad (25)$$

then the expression for r_{out} is given as

$$r_{\text{out}} = r_{ds3} + r_{ds2}\left(\frac{1 + r_{ds3}g_{m3}(1 + \eta_3) + g_{m1}r_{ds1}g_{m3}r_{ds3}}{1}\right) \quad (26)$$

$$r_{\text{out}} \cong r_{ds2}\, g_{m1}r_{ds1}g_{m3}r_{ds3} \quad (27)$$

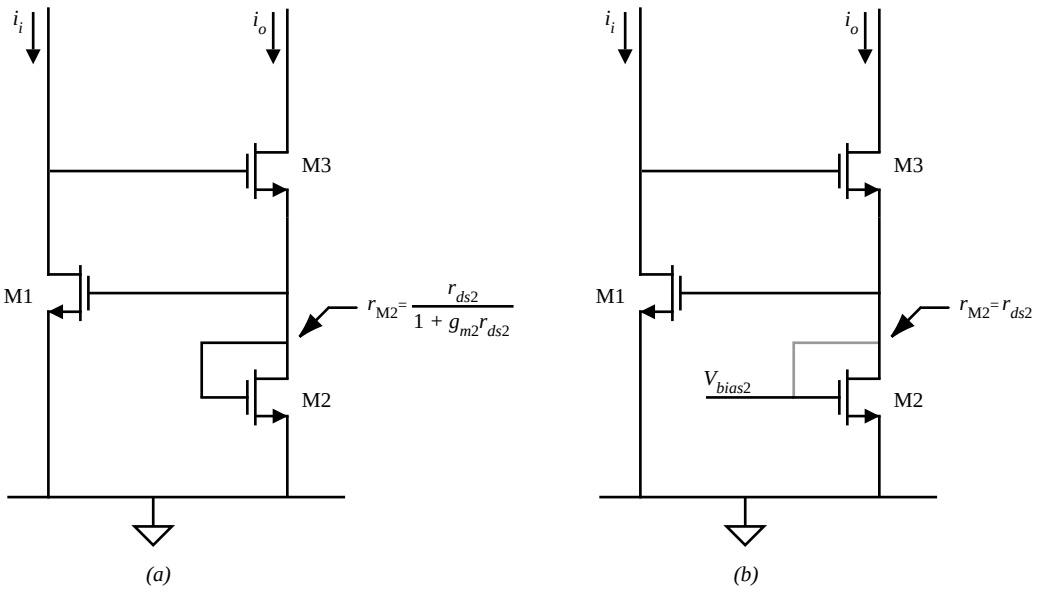


Figure 4.4-9 (a) Wilson current mirror redrawn. (b) Wilson modified to increase r_{out} at M2

This new current mirror illustrated fully in Fig 4.4-10 is called a *regulated cascode* and it achieves an output resistance on the order of $g_m^2 r^3$.

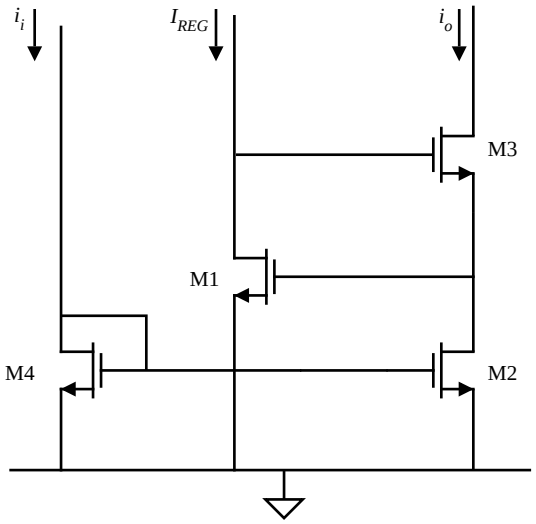


Figure 4.4-10 Regulated cascode current mirror.

Each of the current mirrors discussed above can be implemented using p-channel devices. The circuits perform in an identical manner and exhibit the same small-signal output resistance. The use of n-channel and p-channel current mirrors will be useful in dc biasing of CMOS circuits.

4.5 Current and Voltage References

An ideal voltage or current reference is independent of power supply and temperature. Many applications in analog circuits require such a building block, which

provides a stable voltage or current. The large-signal voltage and current characteristics of an ideal voltage and current reference are shown in Fig. 4.5-1. These characteristics are identical to those of the ideal voltage and current source. The term *reference* is used when the voltage or current values have more precision and stability than ordinarily found in a source. A reference is typically dependent upon the load connected to it. It will always be possible to use a buffer amplifier to isolate the reference from the load and maintain the high performance of the reference. In the discussion that follows, it will be assumed that a high-performance voltage reference can be used to implement a high-performance current reference and vice versa.

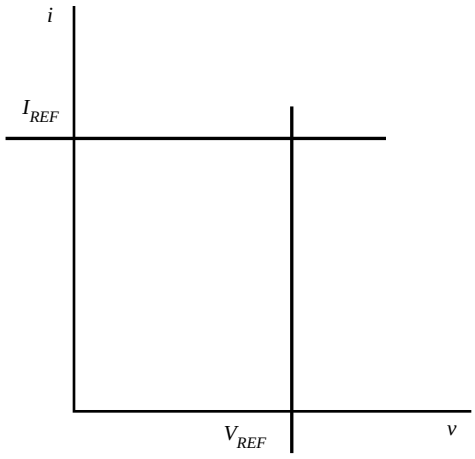


Figure 4.5-1 *V-I* characteristics of ideal voltage and current references.

A very crude voltage reference can be made from a voltage divider between the power supplies. Passive or active components can be used as the divider elements. Figure 4.5-2(a) and (b) shows an example of each. Unfortunately, the value of V_{REF} is directly proportional to the power supply. Let us quantify this relationship by introducing the concept of *sensitivity* S. The sensitivity of V_{REF} of Fig. 4.5-2(a) to V_{DD} can be expressed as

$$\mathrm{S}_{V_{DD}}^{V_{\mathrm{REF}}} = \frac{(\partial V_{\mathrm{REF}}/V_{\mathrm{REF}})}{(\partial V_{DD}/V_{DD})} = \frac{V_{DD}}{V_{\mathrm{REF}}}\left(\frac{\partial V_{\mathrm{REF}}}{\partial V_{DD}}\right) \tag{1}$$

Eq. (1) can be interpreted as: if the sensitivity is 1, then a 10% change in V_{DD} will result in a 10% change in V_{REF} (which is undesirable for a voltage reference). It may also be shown that the sensitivity of V_{REF} of Fig. 4.5-2(b) with respect to V_{DD} is unity (see Problem 5.24).

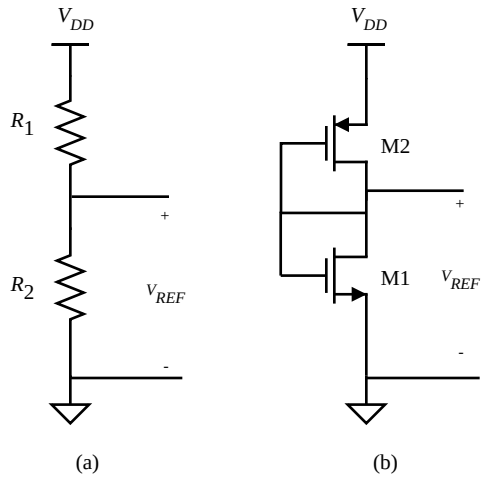


Figure 4.5-2 Voltage references using voltage division. (a) Resistor implementation. (b) Active device implementation.

A simple way of obtaining a voltage reference is to use an active device as shown in Fig. 4.5-3(a) and (b). In Fig. 4.5-3(a), the substrate BJT has been connected to power supply through a resistance *R*. The voltage across the pn junction is given as

$$V_{\text{REF}} = V_{EB} = \frac{kT}{q} \ln\left(\frac{I}{I_s}\right) \tag{2}$$

where I_s is the junction-saturation current defined in Eq. (4) of Sec. 2.5. If V_{DD} is much greater than V_{EB}, then the current I is given as

$$I = \frac{V_{DD} - V_{EB}}{R} \cong \frac{V_{DD}}{R} \tag{3}$$

Thus the reference voltage of this circuit is given as

$$V_{\text{REF}} \cong \frac{kT}{q} \ln\left(\frac{V_{DD}}{RI_s}\right) \tag{4}$$

The sensitivity of V_{REF} of Fig. 4.5-3(a) to V_{DD} is shown to be

$$S_{V_{DD}}^{V_{\text{REF}}} = \frac{1}{\ln[V_{DD}/(RI_s)]} = \frac{1}{\ln(I/I_s)} \tag{5}$$

Interestingly enough, since I is normally greater than I_s, the sensitivity of V_{REF} of Fig. 4.5-3(a) is less than unity. For example, if $I = 1$ mA and $I_s = 10^{-15}$ amperes, then Eq. (5) becomes 0.0362. Thus, a 10% change in V_{DD} creates only a 0.362% change in V_{REF}. Figure 4.5-3(b) shows a method of increasing the value of V_{REF} in Fig. 4.5-3(a). The reference voltage of Fig. 4.5-3(b) can be written as

$$V_{\text{REF}} \cong V_{EB}\left(\frac{R_1 + R_2}{R_1}\right) \tag{6}$$

In order to find the value of V_{EB}, it is necessary to assume that the transistor beta is large and/or the resistance $R_1 + R_2$ is large. The larger V_{REF} becomes in Fig. 4.5-3(b), the more the current I becomes a function of V_{REF} and eventually an iterative solution is necessary.

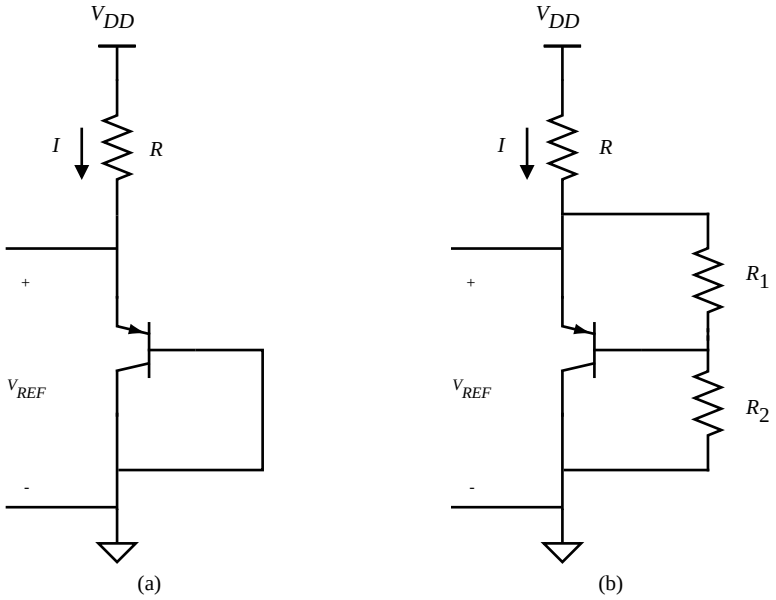


Figure 4.5-3 (a) PN junction voltage reference. (b) Increasing V_{REF} of (a).

The BJT of Fig. 4.5-3(a) may be replaced with a MOS enhancement device to achieve a voltage which is less dependent on V_{DD} than Fig. 4.5-2(a). V_{REF} can be found from Eq. (2) of Sec. 4.2, which gives V_{GS} as

$$V_{GS} = V_T + \sqrt{\frac{2I}{\beta}} \tag{7}$$

Ignoring channel-length modulation, V_{REF} is

$$V_{\text{REF}} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD} - V_T)}{\beta R} + \frac{1}{\beta^2 R^2}} \tag{8}$$

If $V_{DD} = 5$ volts, $W/L = 2$, and R is 100 kΩ, the values of Table 3.1-2 give a reference voltage of 1.281 volts. The sensitivity of Fig. 4.5-4(a) can be found as

$$S_{V_{DD}}^{V_{\text{REF}}} = \left[\frac{1}{1 + \beta (V_{\text{REF}} - V_T) R}\right]\left[\frac{V_{DD}}{V_{\text{REF}}}\right] \tag{9}$$

Using the previous values gives a sensitivity of V_{REF} to V_{DD} of 0.281. This sensitivity is not as good as the BJT because the logarithmic function is much less sensitive to its argument than the square root. The value of V_{REF} of Fig. 4.5-4(a) can be increased using the technique employed for the BJT reference of Fig. 4.5-3(b), with the result shown in Fig. 4.5-4(b), where the reference voltage is given as

$$V_{\text{REF}} = V_{GS}\left(1 + \frac{R_2}{R_1}\right) \tag{10}$$

In the types of voltage references illustrated in Fig. 4.5-3 and Fig. 4.5-4, the designer can use geometry to adjust the value of V_{REF}. In the BJT reference the geometric-dependent parameter is I_s and for the MOS reference it is W/L. The small-signal output resistance of these references is a measure of how dependent the reference will be on the load (see Problem 5.28).

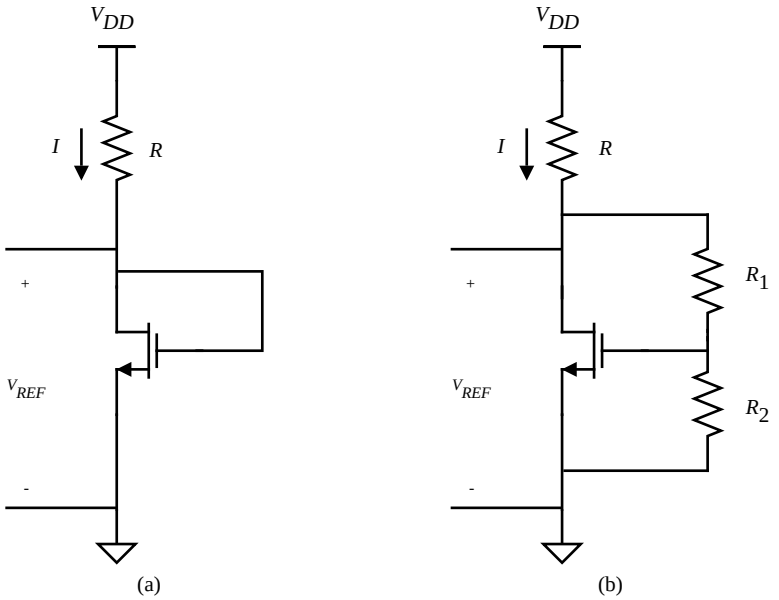


Figure 4.5-4 (a) MOS equivalent of the pn junction voltage reference. (b) Increasing V_{REF} of (a).

A voltage reference can be implemented using the breakdown phenomenon that occurs in the reverse-bias condition of a heavily-doped pn junction discussed in Sec. 2.2. The symbol and current-voltage characteristics of the breakdown diode are shown in Fig. 4.5-5. The breakdown in the reverse direction (v and i are defined for reverse bias in Fig. 4.5-5) occurs at a voltage BV. BV falls in the range of 6 to 8 volts, depending on the doping concentrations of the n^+ and p^+ regions. The knee of the curve depends upon the material parameters and should be very sharp. The small-signal output resistance in the breakdown region is low, typically 30 to 100 Ω, which makes an excellent voltage reference or voltage source. The temperature coefficient of the breakdown diode will vary with the value of breakdown voltage BV as seen in Fig. 4.5-6. Breakdown by the Zener mechanism has a negative temperature coefficient while the avalanche breakdown has a positive temperature coefficient. The breakdown voltage for typical CMOS technologies is around 6.5 to 7.5 volts which gives a temperature coefficient around +3 mV/°C.

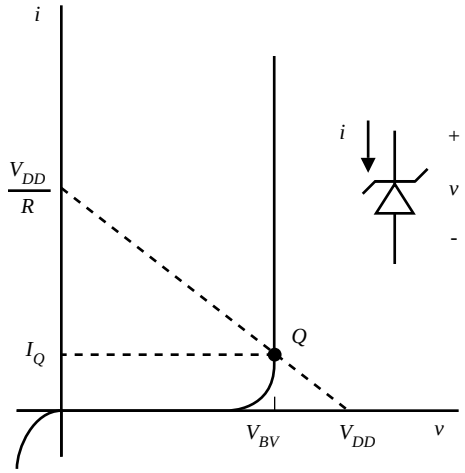


Figure 4.5-5 *V-I* characteristics of a breakdown diode.

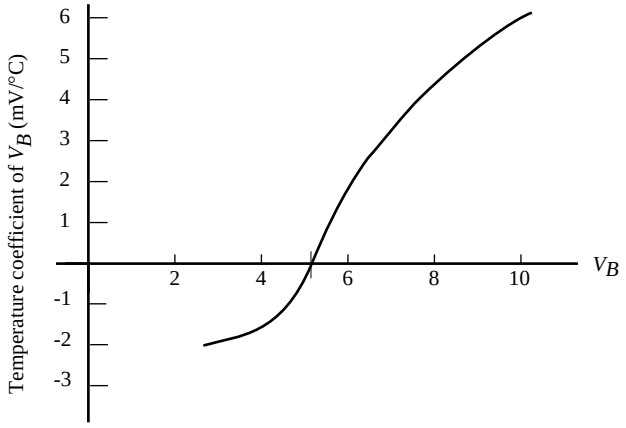


Figure 4.5-6 Variation of the temperature coefficient of the breakdown diode as a function of the breakdown voltage, BV. (By permission from John Wiley & Sons, Inc.)

The breakdown diode can be used as a voltage reference by simply connecting it in series with a voltage-dropping element (resistor or active device) to V_{DD} or V_{SS} as illustrated in Fig. 4.5-7(a). The dotted load line on Fig. 4.5-5 illustrates the operation of the breakdown-diode voltage reference. If V_{DD} or R should vary, little change in BV will result because of the steepness of the curve in the breakdown region. The sensitivity of the breakdown-diode voltage reference can easily be found by replacing the circuit in Fig. 4.5-7(a) with its small-signal equivalent model. The resistor r_Z is equal to the inverse of the slope of Fig. 4.5-5 at the point Q. The sensitivity of V_{REF} to V_{DD} can be expressed as

$$S_{V_{DD}}^{V_{\text{REF}}} = \left(\frac{\partial V_{\text{REF}}}{\partial V_{DD}}\right)\left(\frac{V_{DD}}{V_{\text{REF}}}\right) \cong \left(\frac{v_{ref}}{v_{dd}}\right)\left(\frac{V_{DD}}{BV}\right) = \left(\frac{r_Z}{r_Z + R}\right)\left(\frac{V_{DD}}{BV}\right) \tag{11}$$

Assume that $V_{DD} = 10$ volts, $BV = 6.5$ volts, $r_Z = 100\ \Omega$, and $R = 35\ \text{k}\Omega$. Eq. (11) gives the sensitivity of this breakdown-diode voltage reference as 0.0044. Thus a 10% change in V_{DD} would cause only a 0.044% change in V_{REF}. Other configurations of a voltage reference that uses the breakdown diode are considered in the problems.

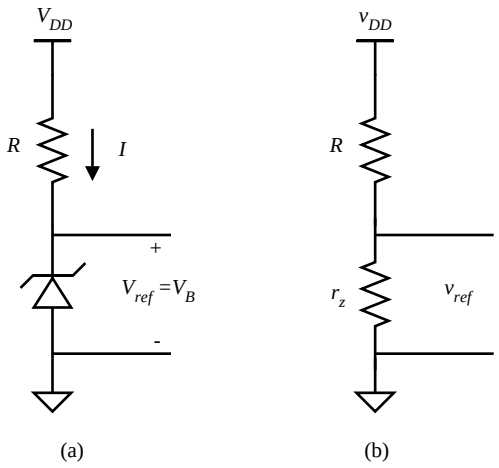


Figure 4.5-7 (a) Breakdown diode voltage reference. (b) Small-signal model of (a).

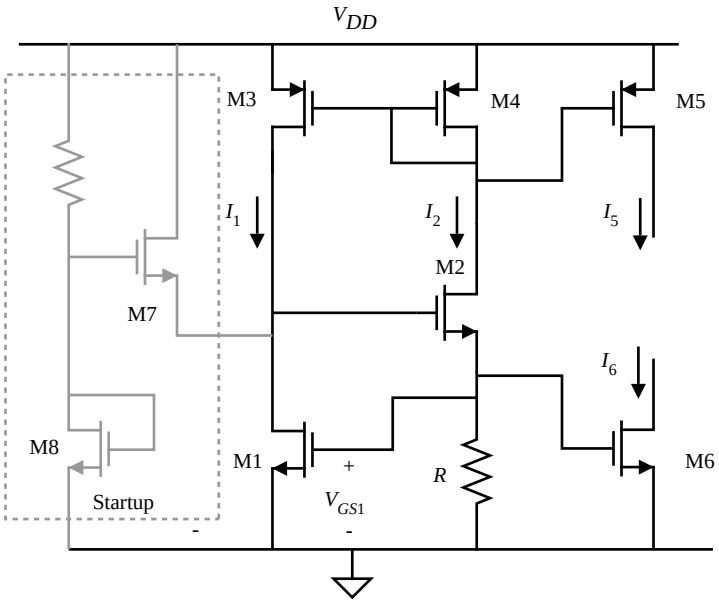
We have noted in Fig. 4.5-3(a) and Fig. 4.5-4(a) that the sensitivity of the voltage across an active device is less than unity. If the voltage across the active device is used to create a current and this current is somehow used to provide the original current through the device, then a current or voltage will be obtained that is for all practical purposes independent of V_{DD}. This technique is called a V_T *referenced source.* This technique is also called a *bootstrap reference.* Fig. 4.5-8(a) shows an example of this technique using all MOS devices. M3 and M4 cause the currents I_1 and I_2 to be equal. I_1 flows through M1 creating a voltage V_{GS1}. I_2 flows through R creating a voltage I_2R. Because these two voltages are connected together, an equilibrium point is established. Figure 4.5-8(b) illustrates how the equilibrium point is achieved. On this curve, I_1 and I_2 are plotted as a function of V. The intersection of these curves defines the equilibrium point indicated by Q. The equation describing this equilibrium point is given as

$$I_2R = V_{T1} + \left(\frac{2I_1L_1}{K'_N W_1}\right)^{1/2} \tag{12}$$

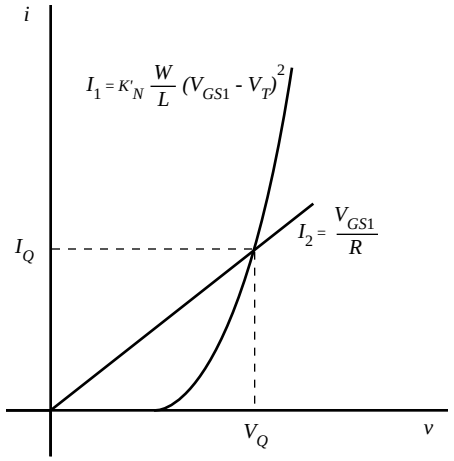
This equation can be solved for $I_1 = I_2 = I_Q$ so giving (ignoring λ)

$$I_Q = I_2 = \frac{V_{T1}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{\mathrm{R}}\sqrt{\frac{2V_{T1}}{\beta_1 R} + \frac{1}{\beta_1^2 R^2}} \tag{13}$$

To the first order, neither I_1 nor I_2 changes as a function of V_{DD}, thus the sensitivity of I_Q to V_{DD} is essentially zero. A voltage reference can be achieved by mirroring I_2 (= I_Q) through M5 or M6 and using a resistor.



(a)



(b)

Figure 4.5-8 (a) Threshold-referenced circuit. (b) *V-I* characteristics of (a) illustrating how the bias point is established.

Unfortunately, there are two possible equilibrium points on Fig. 4.5-8(b). One is at *Q* and the other is at the origin. In order to prevent the circuit from choosing the wrong equilibrium point, a start-up circuit is necessary. The circuit within the dotted box in Fig. 4.5-8(a) functions as a start-up circuit. If the circuit is at the undesired equilibrium point, then I_1 and I_2 are zero. However, M7 will provide a current in M1 that will cause the circuit to move to the equilibrium point at *Q*. As the circuit approaches the point *Q*, the source voltage of M7 increases causing the current through M7 to decrease. At *Q* the current through M1 is essentially the current through M3.

An alternate version of Fig. 4.5-8(a) that uses V_{BE} to reference the voltage or current is shown in Fig. 4.5-9. It can be shown that the equilibrium point is defined by the relationship

$$I_2R = V_{BE1} = V_T \ln\left(\frac{I_1}{I_s}\right) \tag{14}$$

This reference circuit also has two equilibrium points and a start-up circuit similar to Fig. 4.5-8(a) is necessary. The reference circuits in Fig. 4.5-8(a) and Fig. 4.5-9 represent a very good method of implementing power supply independent references. Either circuit can be operated in the weak-threshold inversion in order to develop a low-power, low-supply voltage reference.

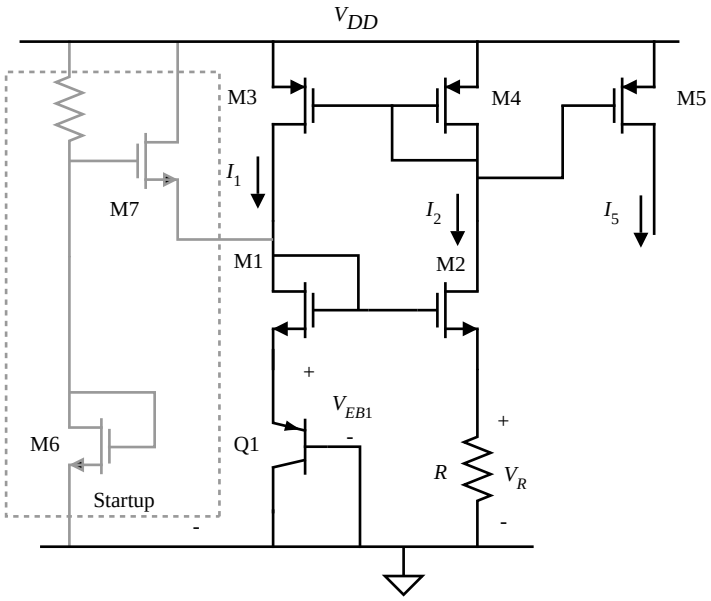


Figure 4.5-9 Base-emitter voltage-referenced circuit.

Unfortunately, supply-independent references are not necessarily temperature independent because the pn junction and gate-source voltage drops are temperature dependent as noted in Sec. 2.5. The concept of *fractional temperature coefficient* (TC_F), defined in Eq. (7) of Sec. 2.5 will be used to characterize the temperature dependence of voltage and current references. We see that TC_F is related to the sensitivity as defined in Eq. (1)

$$TC_F = \frac{1}{T}\left(\begin{matrix}\mathrm{X}\\ \mathrm{S}\\ \mathrm{T}\end{matrix}\right) \tag{15}$$

where $X = V_{\mathrm{REF}}$ or I_{REF}. Let us now consider the temperature characteristics of the simple pn junction of Fig. 4.5-3(a). If we assume that V_{DD} is much greater than V_{REF}, then Eq. (4) describes the reference voltage. Although V_{DD} is independent of temperature, R is not and must be considered. The fractional temperature coefficient of this voltage reference can be expressed using the results of Eq. (17) of Sec. 2.5 as

$$TC_F = \frac{1}{V_{\text{REF}}}\frac{dV_{\text{REF}}}{dT} \cong \frac{V_{\text{REF}} - V_{G0}}{V_{\text{REF}}T} - \frac{3k}{V_{\text{REF}}q} \tag{16}$$

if $v_E = V_{\text{REF}}$. Assuming a V_{REF} of 0.6 volts at room temperature, the TC_F of the simple pn voltage reference is approximately –2500 ppm/°C.

Figure 4.5-4(a) is the MOS equivalent of the simple pn junction voltage reference. The temperature dependence of V_{REF} of this circuit can be written as

$$\frac{dV_{\text{REF}}}{dT} = \frac{-\alpha + \sqrt{\frac{V_{DD} - V_{\text{REF}}}{2\beta R}}\left(\frac{1.5}{T} - \frac{1}{R}\frac{dR}{dT}\right)}{1 + \frac{1}{\sqrt{2\beta R\,(V_{DD} - V_{\text{REF}})}}} \tag{17}$$

Example 4.5-1 Calculation of Threshold Voltage Reference Circuit

Calculate the temperature coefficient of the circuit in Fig. 4.5-4(a) where W/L=2, V_{DD} = 5, R =100 kΩ using the parameters of Table 3.1-2. Resistor, R, is polysilicon and has a temperature coefficient of 1500 ppm/°C.

Using Eq. (9) of section 4.5

$$V_{\text{REF}} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD} - V_T)}{\beta R} + \frac{1}{\beta^2 R^2}}$$

$$\beta R = 220 \times 10^{-6} \times 10^5 = 22$$

$$V_{\text{REF}} = 0.7 - \frac{1}{22} + \sqrt{\frac{2(5 - 0.7)}{22} + \left(\frac{1}{22}\right)^2}$$

$$V_{\text{REF}} = 1.281$$

$$\frac{1}{R}\frac{dR}{dT} = 1500 \text{ ppm/°C}$$

$$\frac{dV_{\text{REF}}}{dT} = \frac{-\alpha + \sqrt{\frac{V_{DD} - V_{\text{REF}}}{2\beta R}}\left(\frac{1.5}{T} - \frac{1}{R}\frac{dR}{dT}\right)}{1 + \frac{1}{\sqrt{2\beta R\,(V_{DD} - V_{\text{REF}})}}}$$

$$\frac{dV_{REF}}{dT} = \frac{-2.3\times10^{-3} + \sqrt{\frac{5-1.281}{2(22)}}\left(\frac{1.5}{300} - 1500\times10^{-6}\right)}{1+\frac{1}{\sqrt{2(22)\ (5-1.281)}}}$$

$$\frac{dV_{REF}}{dT} = -1.189\times10^{-3}\ \text{V/°C}$$

The fractional temperature coefficient is given by

$$TC_F = \frac{1}{V_{REF}}\frac{dV_{REF}}{dT}$$

giving, for this example,

$$TC_F = -1.189\times10^{-3}\left(\frac{1}{1.281}\right) = -928\ \text{ppm/°C}$$

Unfortunately, the TC_F of this example is not realistic because the values of α and the TC_F of the resistor do not have the implied accuracy.

The temperature characteristics of the breakdown diode were illustrated in Fig. 4.5-6. Typically, the temperature coefficient of the breakdown diode is positive. If the breakdown diode can be suitably combined with a negative temperature coefficient, then the possibility of temperature independence exists. Unfortunately, the temperature coefficient depends upon the processing parameters and cannot be well defined, so this approach is not attractive.

The bootstrap reference circuit of Fig. 4.5-8(a) has its current I_2 given by Eq. (13) if the product of R and β are large, the TC_F of the bootstrap reference circuit can be approximated as

$$TC_F = \frac{1}{V_T}\frac{dV_T}{dT} - \frac{1}{R}\frac{dR}{dT} = \frac{-a}{V_T} - \frac{1}{R}\frac{dR}{dT} \qquad (18)$$

Example 4.5-2 Calculation of Bootstrap Reference Circuit

Calculate the temperature coefficient of the circuit in Fig. 4.5-8(a) where $(W/L)_1 = 20$, $V_{DD} = 5$, $R = 100\ k\Omega$ using the parameters of Table 3.1-2. Resistor, R, is polysilicon and has a temperature coefficient of 1500 ppm/°C.

Using Eq. (13) of section 4.5

$$I_Q = I_2 = \frac{V_{T1}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{\mathrm{R}}\sqrt{\frac{2V_{T1}}{\beta_1 R} + \frac{1}{\beta_1^2 R^2}}$$

$$\beta_1 R = 220 \times 10^{-5} \times 10^5 = 220$$

$$\beta_1 R^2 = 220 \times 10^{-5} \times 10^{10} = 22 \times 10^6$$

$$I_Q = \frac{0.7}{10^5} - \frac{1}{22 \times 10^6} + \frac{1}{10^5}\sqrt{\frac{2 \times 0.7}{220} + \left(\frac{1}{220}\right)^2}$$

$$I_Q = 7.75\ \mu\mathrm{A}$$

$$\frac{1}{R}\frac{dR}{dT} = 1500\ \text{ppm/°C}$$

$$TC_F = \frac{-2.3 \times 10^{-3}}{0.7} - 1500 \times 10^{-6} = -4.79 \times 10^{-3}$$

The temperature behavior of the base-emitter-referenced circuit of Fig. 4.5-9 is identical to that of the threshold-referenced circuit of Fig. 4.5-8(a). Eq. (14) showed that I_2 is equal to V_{BE1} divided by R. Thus, Eq. (18) above expresses the TC_F of this reference if V_T is replaced by V_{BE} as follows.

$$TC_F = \frac{1}{V_{BE}}\frac{dV_{BE}}{dT} - \frac{1}{R}\frac{dR}{dT} \tag{19}$$

Assuming V_{BE} of 0.6 volts gives a TC_F −2333 ppm/°C.

The voltage and current references presented in this section have the objective of providing a stable value of current with respect to changes in power supply and temperature. It was seen that while power-supply independence could thus be obtained, satisfactory temperature performance could not.

4.6 Bandgap Reference

In this section we present a technique that results in references which have very little dependence upon temperature and power supply. The *bandgap reference* [7,8,9,10,11] can generate references having a temperature coefficient on the order of 10 ppm/°C over the temperature range of 0 °C to 70 °C. The principle behind the bandgap reference is illustrated in Fig. 4.6-1. A voltage V_{BE} is generated from a pn-junction diode having a temperature coefficient of approximately −2.2 mV/°C at room temperature. Also generated is a thermal voltage V_t ($V_t = k\,T/q$) which is proportional to absolute temperature (PTAT) and has a temperature coefficient of +0.085 mV/°C at room

temperature. If the V_t voltage is multiplied by a constant K and summed with the V_{BE} voltage, then the output voltage is given as

$$V_{\text{REF}} = V_{BE} + KV_t \tag{1}$$

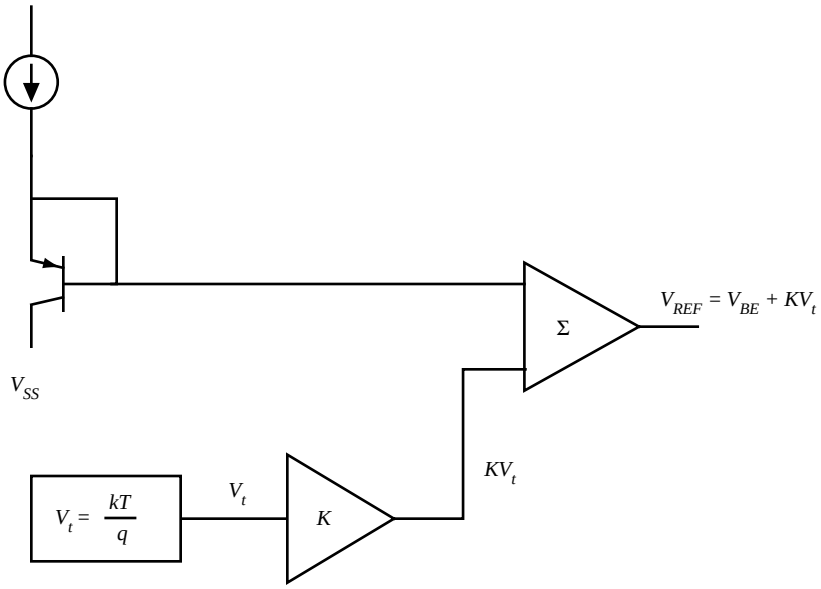


Figure 4.6-1 General principle of the bandgap reference.

Differentiating Eq. (1) with respect to temperature and using the temperature coefficients for V_{BE} and V_t leads to a value of K that should theoretically give zero temperature dependence. In order to achieve the desired performance, it is necessary to develop the temperature dependence of V_{BE} in more detail. One can see that since V_{BE} can have little dependence upon the power supply (i.e. the bootstrapped references of Sec. 4.5), the power-supply dependence of the bandgap reference will be quite small.

To understand thoroughly how the bandgap reference works, we must first develop the temperature dependence of V_{BE}. Consider the relationship for the collector-current density in a bipolar transistor

$$J_C = \frac{qD_n n_{po}}{W_B} \exp\left(\frac{V_{BE}}{V_t}\right) \tag{2}$$

where

J_C = collector current density (A/m^2)

n_{po} = equilibrium concentration of electrons in the base

D_n = average diffusion constant for electrons

W_B = base width

The equilibrium concentration can be expressed as

$$n_{po} = \frac{n_i^2}{N_A} \tag{3}$$

where

$$n_i^2 = DT^3 \exp(-V_{G0}/V_t) \tag{4}$$

The term D is a temperature independent constant and V_{G0} is the bandgap voltage (1.205 volts). Combining Eq's. (2) through (4) result in the following equation for collector current density

$$J_C = \frac{q D_n}{N_A W_B} DT^3 \exp\left(\frac{V_{BE} - V_{G0}}{V_t}\right) \tag{5}$$

$$= AT^{\gamma} \exp\left(\frac{V_{BE} - V_{G0}}{V_t}\right) \tag{6}$$

In Eq. (6), the temperature independent constants of Eq. (5) are combined into a single constant A. The coefficient of temperature γ is slightly different from 3 due to the temperature dependence of D_n.

A relation for V_{BE} can be developed from Eq. (6) and is given as

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{J_C}{AT^{\gamma}}\right) + V_{G0} \tag{7}$$

Now consider J_C at a temperature T_0.

$$J_{C0} = AT_0^{\gamma} \exp\left[\frac{q}{kT_0}(V_{BE0} - V_{G0})\right] \tag{8}$$

The ratio of J_C to J_{C0} is

$$\frac{J_C}{J_{C0}} = \left(\frac{T}{T_0}\right)^{\gamma} \exp\left[\frac{q}{k}\left(\frac{V_{BE} - V_{G0}}{T} - \frac{V_{BE0} - V_{G0}}{T_0}\right)\right] \tag{9}$$

Eq. (9) can be rearranged to get V_{BE}

$$V_{BE} = V_{GO}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{\gamma kT}{q} \ln\left(\frac{T_0}{T}\right) + \frac{kT}{q} \ln\left(\frac{J_C}{J_{C0}}\right) \tag{10}$$

By taking the derivative of Eq. (10) at T_0 with respect to temperature, (assuming that J_C has a temperature dependence of T^{α}), the dependence of V_{BE} on temperature is clearly seen to be

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_{T=T0} = \frac{V_{BE} - V_{G0}}{T_0} + (\alpha - \gamma)\left(\frac{k}{q}\right) \tag{11}$$

At 300 °K the change of V_{BE} with respect to temperature is approximately –2.2 mV/°C. We have thus derived a suitable relationship for the V_{BE} term shown in Fig. 4.6-1. Now, it is also necessary to develop the relationship for ΔV_{BE} for two bipolar transistors having different current densities. Using the relationship given in Eq. (7), a relationship for ΔV_{BE} can be given as

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{J_{C1}}{J_{C2}}\right) \tag{12}$$

Therefore

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{V_t}{T} \ln\left(\frac{J_{C1}}{J_{C2}}\right) \tag{13}$$

In order to achieve zero temperature coefficient at T_0, the variations of V_{BE} and ΔV_{BE} as given in Eq's. (11) and (13) must add up to zero. This is expressed mathematically as

$$0 = K'' \left(\frac{V_{t0}}{T_0}\right) \ln\left(\frac{J_{C1}}{J_{C2}}\right) + \frac{V_{BE0} - V_{G0}}{T_0} + \frac{(\alpha - \gamma)V_{t0}}{T_0} \tag{14}$$

where K'' is a circuit constant adjusted to make Eq. (14) true.

$$0 = K \left(\frac{V_{t0}}{T_0}\right) + \frac{V_{BE0} - V_{G0}}{T_0} + \frac{(\alpha - \gamma)V_{t0}}{T_0} \tag{15}$$

Solving for K yields

$$K = \frac{V_{G0} - V_{BE0} + (\gamma - \alpha)V_{t0}}{V_{t0}} \tag{16}$$

The term K ($K = K'' \ln[J_{C1}/J_{C2}]$) is under the designer's control, so that it can be designed to achieve zero temperature coefficient. Rearranging Eq. (16) yields

$$KV_{t0} = V_{G0} - V_{BE0} + V_{t0}(\gamma - \alpha) \tag{17}$$

Noting that K in Eq. (17) is the same as that in Eq. (1), as both are constants required to achieve a zero temperature coefficient, then substituting of Eq. (17) into Eq. (1) gives

$$V_{\text{REF}}\Big|_{T=T0} = V_{G0} + V_{t0}(\gamma - \alpha) \tag{18}$$

For typical values of $\gamma = 3.2$ and $\alpha = 1$, $V_{\text{REF}} = 1.262$ at 300 °K. A typical family of reference-voltage variations as a function of T for various values of T_0 is shown in Fig. 4.6-2.

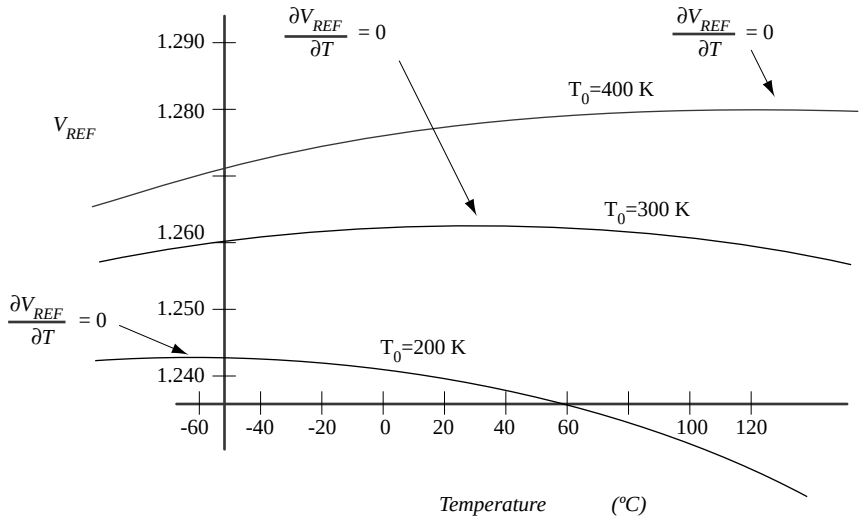


Figure 4.6-2 Variation of bandgap reference output with temperature (© John Wiley and Sons, Inc.).

A conventional CMOS bandgap reference for an n-well process is illustrated in Fig. 4.6-3. The input-offset voltage of the otherwise ideal op amp (V_{OS}) has been included in the circuit. Transistors Q1 and Q2 are assumed to have emitter-base areas of A_{E1} and A_{E2}, respectively. If we assume for the present that V_{OS} is zero, then the voltage across R_1 is given as

$$V_{R1} = V_{EB2} - V_{EB1} = V_t \ln\left(\frac{J_2}{J_{S2}}\right) - V_t \ln\left(\frac{J_1}{J_{S2}}\right) = V_t \ln\left(\frac{I_2 A_{E1}}{I_1 A_{E2}}\right) \tag{19}$$

However, the op amp also forces the relationship

$$I_1 R_2 = I_2 R_3 \tag{20}$$

The reference voltage of Fig. 4.6-3 can be written as

$$V_{\text{REF}} = V_{EB2} + I_2 R_3 = V_{BE2} + V_{R1}\left(\frac{R_2}{R_1}\right) \tag{21}$$

Substituting Eq. (20) into Eq. (19) and the result into Eq. (21) gives

$$V_{\text{REF}} = V_{EB2} + \left(\frac{R_2}{R_1}\right) V_t \ln\left(\frac{R_2 A_{E1}}{R_3 A_{E2}}\right) \tag{22}$$

Comparing Eq. (22) with Eq. (1) defines the constant K as

$$K = \left(\frac{R_2}{R_1}\right) \ln\left(\frac{R_2 A_{E1}}{R_3 A_{E2}}\right) \tag{23}$$

Thus, the constant K is defined in terms of resistor and emitter-base area ratios. It can be shown that if the input-offset voltage is not zero, that Eq. (22) becomes

$$V_{\text{REF}} = V_{EB2} - \left(1 + \frac{R_2}{R_1}\right) V_{OS} + \frac{R_2}{R_1} V_t \ln\left[\frac{R_2 A_{E1}}{R_3 A_{E2}}\left(1 - \frac{V_{OS}}{I_1 R_2}\right)\right] \tag{24}$$

It is clear that the input-offset voltage of the op amp should be small and independent of temperature in order not to deteriorate the performance of V_{REF}.

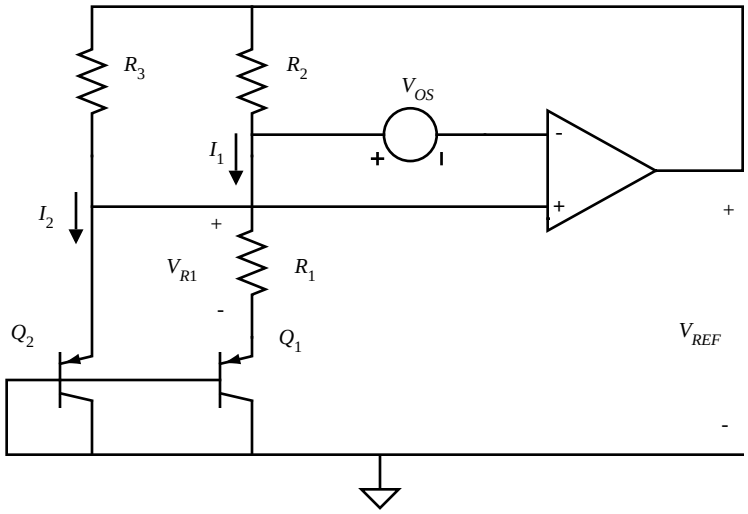


Figure 4.6-3 A conventional bandgap reference.

The dependence of V_{REF} upon power supply can now be investigated. In Eq. (24), the only possible parameters which may depend upon power supply are V_{EB2}, V_{OS} and I_1. Since V_{EB2} and I_1 are derived from V_{REF}, the only way in which V_{REF} can depend upon the power supply is through a finite power-supply rejection ratio of the op amp (manifesting itself as a variation in V_{OS}). If the PSRR of the op amp is large, then Fig. 4.6-3 is for all practical purposes a power supply independent reference as well as a temperature independent reference.

Example 4.6-1 The Design of a Bandgap-Voltage Reference

Assume that $A_{E1} = 10\ A_{E2}$, $V_{EB2} = 0.7$ V, $R_2 = R_3$, and $V_t = 0.026$ V at room temperature. Find R_2/R_1 to give a zero temperature coefficient at room temperature. If $V_{OS} = 10$ mV, find the change in V_{REF}. Note that $I_1 R_2 = V_{\text{REF}} - V_{EB2} - V_{\text{OS}}$.

Using the values of V_{EB2} and V_t in Eq. (1) and assuming that $V_{\text{REF}} = 1.262$ V gives a value of K equal to 21.62. Eq. (23) gives $R_2/R_1 = 9.39$. In order to use Eq. (24), we must know the approximate value of V_{REF} and iterate if necessary. Assuming V_{REF} to be 1.262, we obtain from Eq. (24) a new value $V_{\text{REF}} = 1.153$ V. The second iteration makes little difference on the result because V_{REF} is in the argument of the logarithm.

The temperature dependence of the conventional bandgap reference of Fig. 4.6-3 is capable of realizing temperature coefficients in the vicinity of 100 ppm/°C. Unfortunately, there are several important second-order effects that must be considered in order to approach the 10 ppm/°C behavior [3]. One of these effects, as we have already

seen, is the input-offset voltage V_{OS} of the op amp. We have seen in Eq. (24) how the magnitude of V_{OS} can contribute a significant error in the output of the reference circuit. Furthermore, V_{OS} is itself a function of temperature and will introduce further deviations from ideal behavior. A further source of error is the temperature coefficient of the resistors. Other effects include the mismatch in the betas of Q1 and Q2 and the mismatch in the finite base resistors of Q1 and Q2. Yet another source of complication is that the silicon bandgap voltage varies as a function of temperature over wide temperature ranges. A scheme for compensating the V_{G0} curvature and canceling V_{OS}, the mismatches in β (bipolar current gain), and the mismatches in base resistance, has permitted temperature coefficients of the reference circuit to be as small as 13 ppm/°C over the range of 0 °C to 70 °C.

Suppose that a temperature-independent current is desired. A first attempt in achieving this would be to place the bandgap voltage across a resistor thus generating a V_{BE}/R current. The obvious problem with this is the lack of a temperature-independent resistor! The solution to achieving a near temperature independent current source lies in recognizing that the bandgap reference voltage developed in this chapter is not perfectly temperature independent as illustrated in Fig. 4.5-2. In fact, a positive or negative temperature coefficient can be achieved by designing the circuit so that at the nominal temperature (T_0), the temperature coefficient is either positive or negative. By adjusting the slope of the circuit's temperature characteristic so that it is the same as a resistor, a near zero-temperature coefficient circuit is achieved. Equation (25) illustrates the equivalence required to achieve the near zero temperature coefficient for the circuit shown in Fig. 4.6-4.

$$\frac{\partial R_4}{\partial T} = K'' \left(\frac{V_{t0}}{T_0}\right) \ln\left(\frac{J_{C1}}{J_{C2}}\right) + \frac{V_{BE0} - V_{G0}}{T_0} + \frac{(\alpha - \gamma)V_{t0}}{T_0} \tag{25}$$

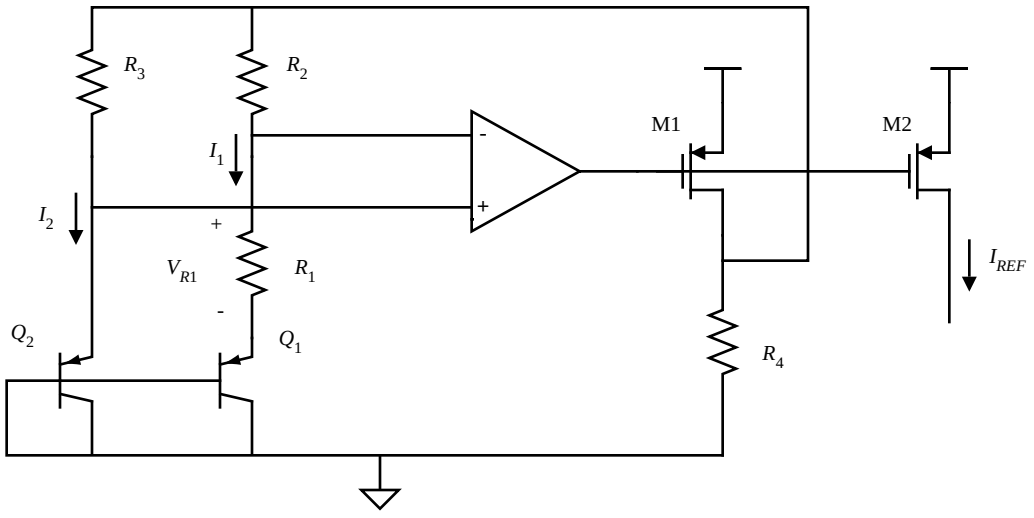


Figure 4.6-4 A temperature-independent reference current.

Although other techniques have been used to develop power-supply and temperature-independent references, the bandgap circuit has proven the best to date. In this section we have used the bandgap concept to develop precision references. As the requirement for higher precision increases, the designer will find it necessary to begin including second-order and sometimes third-order effects that might normally be neglected. These higher-order effects require the designer to be familiar with the physics and operation of the MOS devices.

4.7 Summary

This chapter has introduced CMOS subcircuits, including the switch, active resistors, current sinks/sources, current mirrors or amplifiers, and voltage and current references. The general principles of each circuit were covered as was their large-signal and small-signal performance. Remember that the circuits presented in this chapter are rarely used by themselves, rather they are joined with other such circuits to implement a desired analog function.

The approach used in each case was to present a general understanding of the circuit and how it works. This presentation was followed by analysis of large-signal performance, typically a voltage-transfer function or a voltage-current characteristic. Limitations such as signal swing or nonlinearity were identified and characterized. This was followed by the analysis of small-signal performance. The important parameters of small-signal performance include ac resistance, voltage gain, and bandwidth.

The subject matter presented in this chapter will be continued and extended in the next chapter. A good understanding of the circuits in this and the next chapter will provide a firm foundation for the later chapters and subject material.

Problems

1. Using SPICE, generate a set of parametric I-V curves similar to Fig. 4.1-3 for a transistor with a W/L = 10/1. Use model parameters from Table 3.1-2.
2. The circuit shown in Fig. P4.1 illustrates a single-channel MOS resistor with a W/L of 2μm/1μm. Using Table 3.1-2 model parameters, calculate the small-signal on resistance of the MOS transistor at various values for V_S and fill in the table below.

V_S (volts)	R (ohms)
0.0	
1.0	
2.0	
3.0	
4.0	
5.0	

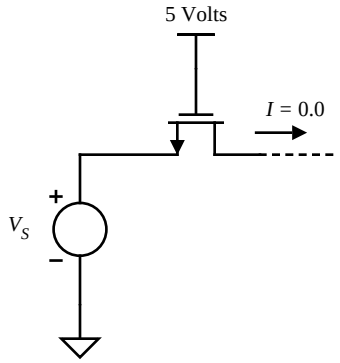


Figure P4.1

3. The circuit shown in Fig. P4.2 illustrates a single-channel MOS resistor with a W/L of 4μm/1μm. Using Table 3.1-2 model parameters, calculate the small-signal on resistance of the MOS transistor at various values for V_S and fill in the table below. Note that the most positive supply voltage is 5 volts.

V_S (volts)	R (ohms)
0.0	
1.0	
2.0	
3.0	
4.0	
5.0	

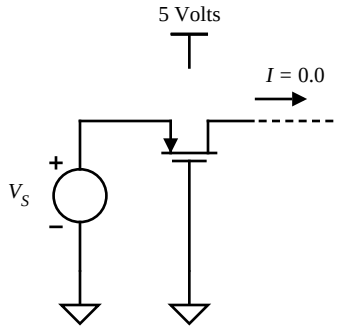


Figure P4.2

3. The circuit shown in Fig. P4.3 illustrates a complementary MOS resistor with an n-channel W/L of 2μm/1μm and a p-channel W/L of 4μm/1μm. Using Table 3.1-2 model parameters, calculate the small-signal on resistance of the complementary MOS resistor at various values for V_S and fill in the table below. Note that the most positive supply voltage is 5 volts.

V_S (volts)	R (ohms)
0.0	
1.0	
2.0	
3.0	
4.0	
5.0	

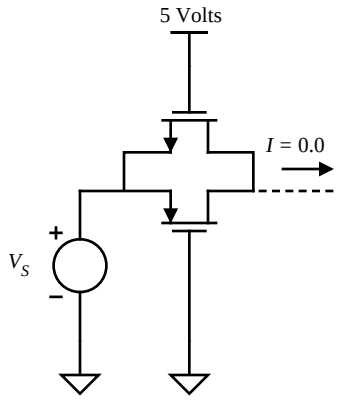


Figure P4.3

4. For the circuit in Figure P4.4 assume that there are NO capacitance parasitics associated with M1. The voltage source v_{in} is a small-signal value whereas voltage source V_{dc} has a dc value of 3 volts. Design M1 to achieve the following frequency response.

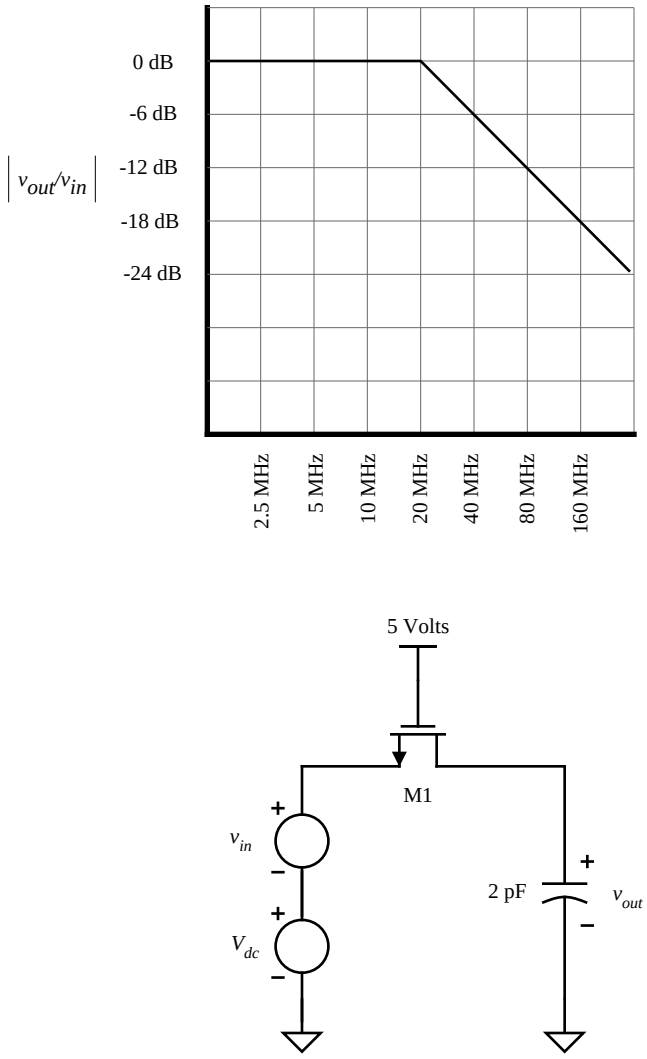


Figure P4.4

5. Using the result of Problem 4, calculate the frequency response resulting from changing the gate voltage of M1 to 4.5 volts. Draw a Bode diagram of the resulting frequency response.
6. Consider the circuit shown in Fig. P4.6 Assume that the *slow regime* of charge injection is valid for this circuit. Initially, the charge on C_1 is zero. Calculate v_{OUT} at time t_1 after ϕ_1 pulse occurs. Assume that CGS0 and CGD0 are both 5 fF. C_1=30 fF. You cannot ignore body effect.

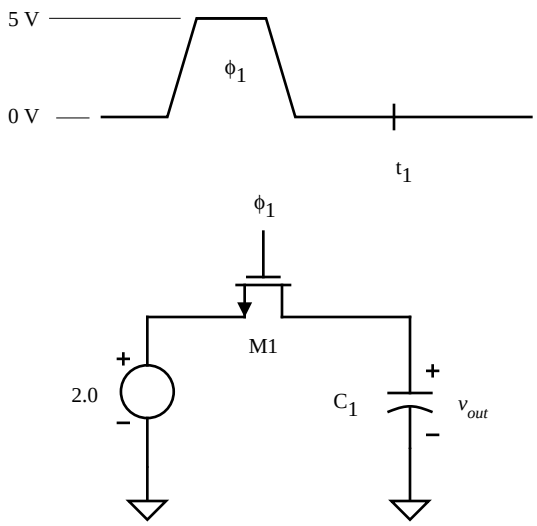


Figure P4.6

7. In Problem 6, how long must ϕ_1 remain high for C_1 to charge up to 99% of the desired final value (2.0 volts)?
8. In Problem, the charge feedthrough could be reduced by reducing the size of M1. What impact does reducing the size (W/L) of M1 have on the requirements on the width of the ϕ_1 pulse width?
9. Considering charge feedthrough due to slow regime only, will reducing the magnitude of the ϕ_1 pulse impact the resulting charge feedthrough? What impact does reducing the magnitude of the ϕ_1 pulse have on the accuracy of the voltage transfer to the output?
10. Repeat Example 4.1-1 with the following conditions. Calculate the effect of charge feedthrough on the circuit shown in Fig. 4.1-9 where V_S = 1.5 volts, C_L = 150 fF, W/L = 1.6μm/0.8μm, and V_G is given for two cases illustrated below. The fall time is 8ns instead of 10ns.
11. Figure P4.11 illustrates a circuit that contains a charge-cancellation scheme. Design the size of M2 to minimize the effects of charge feedthrough. Assume slow regime.

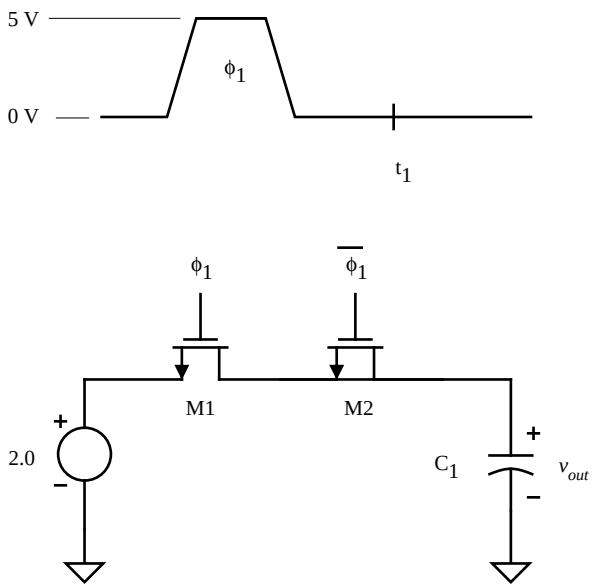


Figure P4.11

12. Figure P4.12 illustrates a source-degenerated current source. Using Table 3.1-2 model parameters calculate the output resistance at the given current bias.

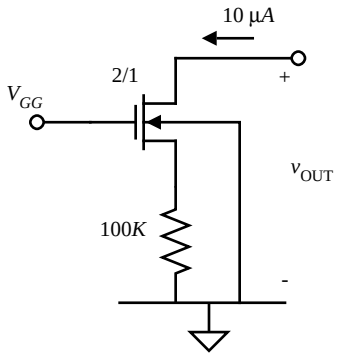


Figure P4.12

13. Calculate the minimum output voltage required to keep device in saturation in Problem 12.
14. Using the cascode circuit shown in Fig. P4.14, design the W/L of M1 to achieve the same output resistance as the circuit in Fig. P4.12.

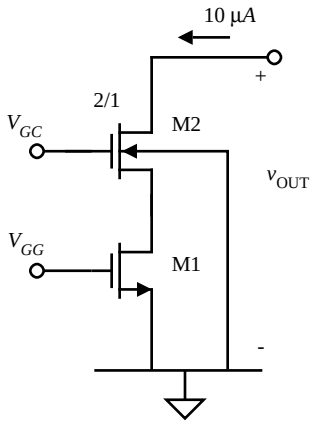


Figure P4.14

15. Calculate the minimum output voltage required to keep device in saturation in Problem 14. Compare this result with that of Problem 13. Which circuit is a better choice in most cases?
16. Calculate the output resistance and the minimum output voltage, while maintaining all devices in saturation, for the circuit shown in Fig. P4.16. Assume that I_{OUT} is actually 10μA. Simulate this circuit using SPICE Level 3 model (Table 3.4-1) and determine the actual output current, I_{OUT} . Use Table 3.1-2 for device model information.

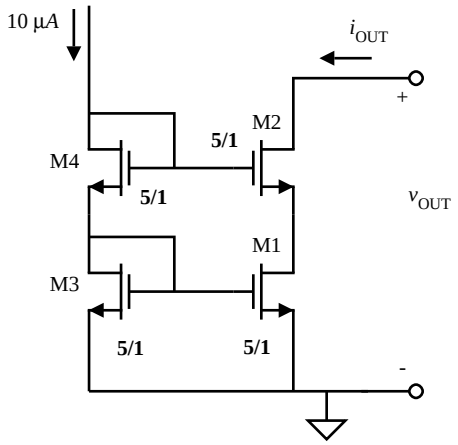


Figure P4.16

17. Calculate the output resistance, and the minimum output voltage, while maintaining all devices in saturation, for the circuit shown in Fig. P4.17. Assume that I_{OUT} is actually 10μA. Simulate this circuit using SPICE Level 3 model (Table 3.4-1) and determine the actual output current, I_{OUT} . Use Table 3.1-2 for device model information.

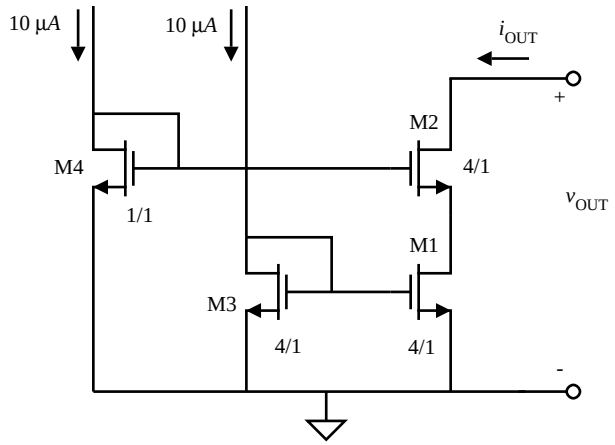


Figure P4.17

18. Design M3 and M4 of Fig. P4.18 so that the output characteristics are identical to the circuit shown in Fig. P4.17. It is desired that I_{OUT} is ideally 10μA.

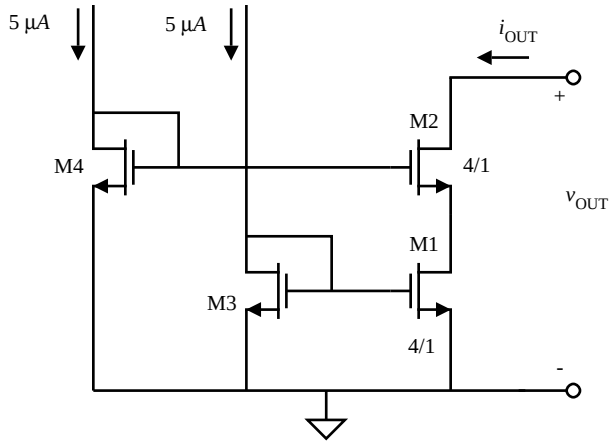


Figure P4.18

19. For the circuit shown in Fig. P4.19, determine I_{OUT} by simulating it using SPICE Level 3 model (Table 3.4-1). Use Table 3.1-2 for device model information. Compare the results with the SPICE results from Problem 17.

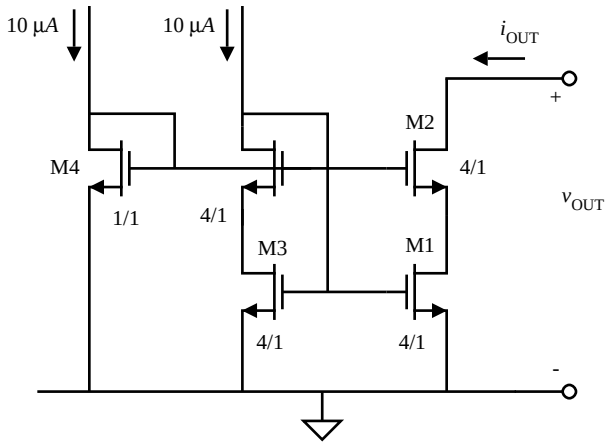


Figure P4.19

20. Consider the simple current mirror illustrated in Fig. P4.20. Over process, the absolute variations of physical parameters are as follows:

Width variation	+/- 5%
Length variation	+/- 5%
K' variation	+/- 5%
V_T variation	+/- 5mV

Assuming that the drain voltages are identical, what is the minimum and maximum output current measured over the process variations given above.

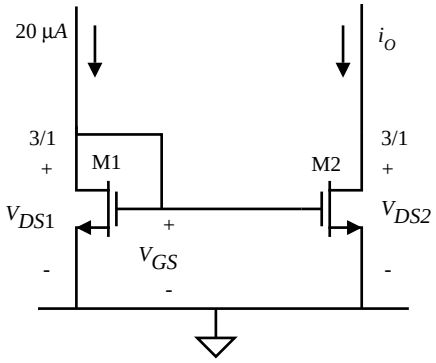


Figure P4.20

21. Consider the circuit in Fig. P4.21 where a single MOS diode (M2) drives two current mirrors (M1 and M3). A signal (v_{sig}) is present at the drain of M3 (due to other circuitry not shown). What is the effect of v_{sig} on the signal at the drain of M1, v_{OUT} ? Derive the transfer function v_{sig}(s)/ v_{OUT}(s). You must take into account the gate-drain capacitance of M3 but you can ignore the gate-drain capacitance of M1. Given that I_{BIAS}=10μA, W/L of all transistors is 2μm/1μm, and

using the data from Table 3.1-2 and Table 3.2-1, calculate v_{OUT} for v_{sig} =100mV at 1MHz.

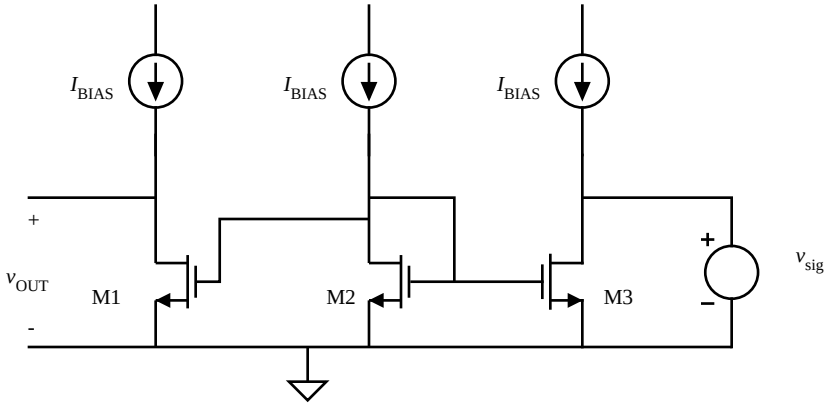


Figure P4.21

22 An improved bandgap reference generator is illustrated in Fig. P4-22. Assume that the devices M1 through M5 are identical in W/L. Further assume that the area ratio for the bipolar transistors is 10:1. Design the components to achieve an output reference voltage of 1.262 volts. Assume that the amplifier is ideal. What advantage, if any, is there in stacking the bipolar transistors?

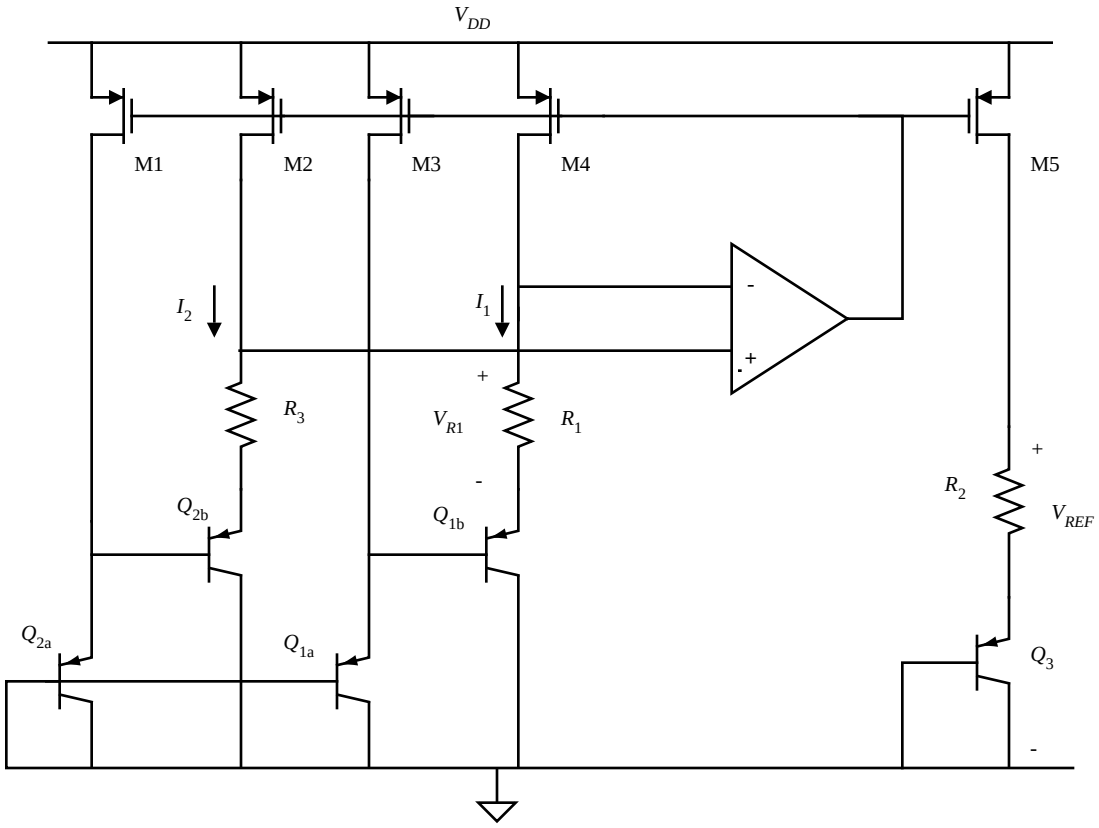


Figure P4-22

23. In an attempt to reduce the noise output of the reference circuit shown in Fig. P4-22, a capacitor is placed on the gate of M5. Where should the other side of the capacitor be connected and why?
24. In qualitative terms, explain the effect of low Beta for the bipolar transistors in Fig. P4-22?
25. Consider the circuit shown in Fig. P4-25. It is a variation of the circuit shown in Fig. P4-22. What is the purpose of the circuit made up of M6-M9 and Q4?
26. Extend Example 4.6-1 to the design of a temperature-independent current based upon the circuit shown in Fig. 4.6-4. The temperature coefficient of the resistor, R_4, is +1500 ppm/°C.

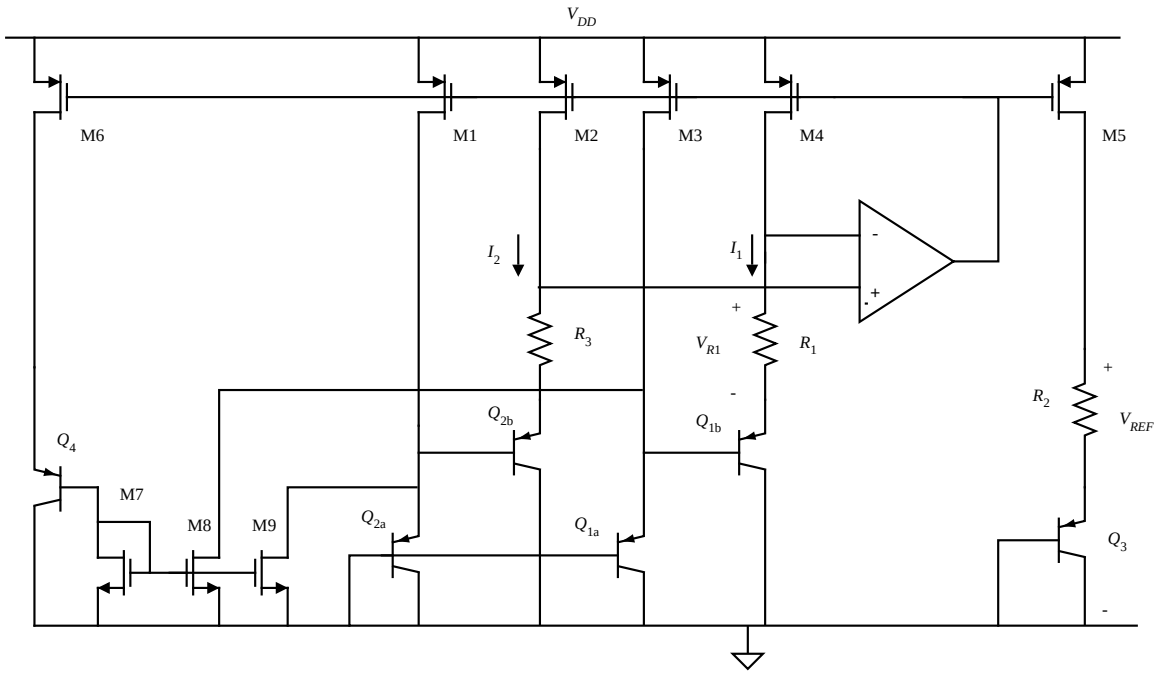


Figure P4-25

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Chapter 9 - Switched Capacitor Circuits

Until the early 1970's, analog signal processing circuits used continuous time circuits consisting of resistors, capacitors and op amps. Unfortunately, the absolute tolerances of resistors and capacitors available in standard CMOS technologies are not good enough to perform most analog signal processing functions. In the early 1970's, analog sampled data techniques were used to replace the resistor resulting in circuits consisting of only MOSFET switches, capacitors and op amps [1,2]. These circuits are called *switched capacitor circuits* and have become a popular method of implementing analog signal processing circuits in standard CMOS technologies. One the important reasons for the success of switched capacitor circuits is that the accuracy of the signal processing function is proportional to the accuracy of capacitor ratios. We have seen in previous chapters that the relative accuracy of capacitors implemented on standard CMOS technology can be quite good. The primary advantages of switched capacitor circuits include (1) compatibility with CMOS technology, (2) good accuracy of time constants, (3) good voltage linearity, and (4) good temperature characteristics. The primary disadvantages are (1) clock feedthrough, (2) the requirement of a nonoverlapping clock, and (3) the bandwidth of the signal must be less than the clock frequency.

The important component of signal processing circuits are the signals. Signals can be characterized by their time and amplitude properties. From a time viewpoint, signals are categorized as continuous and discrete. A *continuous time signal* is defined for all time whereas a *discrete time signal* is defined only over a range of times (often only a point in time). Signals can also be continuous or discrete in amplitude. An *analog signal* is defined as a signal that is continuous in amplitude (can have all possible amplitude values). A *digital signal* is a signal that is defined only for certain amplitude values. For example, a binary digital signal has only two amplitude states normally designated as 1 and 0. Switched capacitor circuits are continuous in amplitude and discrete in time. They are often called *analog sampled data circuits* [3].

The concepts of switched capacitor circuits are introduced in this chapter. While a strong background on analog sampled data circuits and z-domain techniques would be helpful, the approach used in this chapter is based on standard circuit analysis methods for capacitive circuits. The first section focuses on the use of switched capacitor circuits to emulate resistors. We will only consider the basic, two-phase, non-overlapping clock schemes. The analysis methods will be developed in the next section. The following two sections applies the concepts to switched capacitor amplifiers followed by switched capacitor integrators. These two blocks form the basis of switched capacitor circuits. Next, we consider z-domain models for switched capacitor circuits. This will help in the analysis and design of switched capacitor circuits. Switched capacitor filter builiding blocks will be considered next. This will include first-order and second-order building blocks. Finally, the chapter concludes by examining aliasing and the methods that are used to prevent its influence on switched capacitor circuits.

9.1 Switched Capacitor Circuits

The basic concepts of transferring charge among capacitors will be given in this section. The emulation of resistors with circuits containing switches and capacitors will be developed. This will be followed by a review of circuit analysis techniques that allow the analysis of switched capacitor circuits. A first-order, low pass filter will be examined to illustrate the methods developed.

Resistor Emulation

The first recorded use of switches and capacitors to emulate (measure) resistance is found in a text written by James Clerk Maxwell in 1873 [4]. On pages 420 through 425 he describes how to measure the resistance of a galvanometer by connecting it in series with a battery, ammeter and capacitor and periodically reversing the capacitor. Using a similar approach, we can illustrate how to emulate a resistor. Consider the switched capacitor circuit of Fig. 9.1-1(a). This configuration is called the *parallel switched capacitor equivalent resistor*. Next, we show how Fig. 9.1-1(a) is equivalent to the resistor R in Fig. 9.1-1(b.)

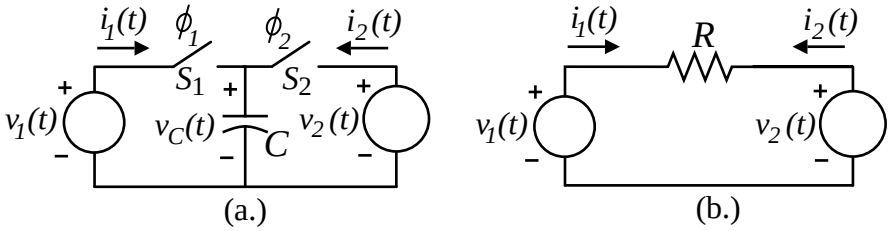


Figure 9.1-1 (a.) Parallel switched capacitor equivalent resistor.
(b.) Continuous time resistor of value R.

The parallel switched capacitor equivalent resistor circuit in Fig. 9.1-1(a) consists two independent voltage sources, $v_1(t)$ and $v_2(t)$, two controlled switches, S_1 and S_2 and a capacitor, C. The switches, S_1 and S_2 are controlled by the clock waveforms. These clock waveforms are illustrated in Fig. 9.1-2. There are two clock waveforms, ϕ_1 and ϕ_2. When a clock waveform has the value of 1, the switch is closed. When the value of the clock waveform is 0, the switch is open. Note, that ϕ_1 and ϕ_2 never have the value of 1 at the same time. This type of clock is called a *nonoverlapping clock*. The period of the clock waveforms in Fig. 9.1-2 is T. The width of each individual clock is slightly less than $T/2$.

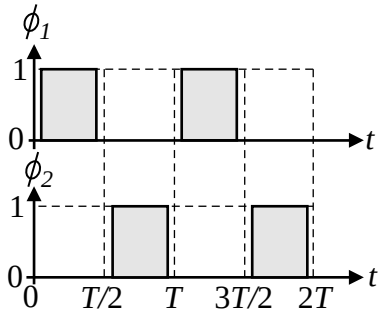


Figure 9.1-2 - Waveforms of a typical two-phase, nonoverlapping clock scheme.

Assume that the voltages $v_1(t)$ and $v_2(t)$ in Fig. 9.1-1(a) do not change very much during the period of the clock, T. Thus, we can approximately assume that $v_1(t)$ and $v_2(t)$ are nearly constant during the time T. Now let us find the average value of the current, $i_1(t)$, flowing from $v_1(t)$ into the capacitor C. The definition of the average current is

$$i_1(average) = \frac{1}{T}\int_0^T i_1(t)dt \ . \tag{1}$$

Because, $i_1(t)$ only flows during the time $0 \le t \le T/2$, we can rewrite Eq. (1) as

$$i_1(average) = \frac{1}{T}\int_0^{T/2} i_1(t)dt \ . \tag{2}$$

However, we know that charge and current are related as follows.

$$i_1(t) = \frac{dq_1(t)}{dt} \tag{3}$$

Substituting Eq. (3) into Eq. (2) gives

$$i_1(average) = \frac{1}{T}\int_0^{T/2} dq_1(t) = \frac{q_1(T/2) - q_1(0)}{T} \ . \tag{4}$$

The charge associated with a time-invariant capacitor is expressed as

$$q_C(t) = Cv_C(t) \ . \tag{5}$$

Substituting Eq. (5) into Eq. (4) gives the desired result of

$$i_1(average) = \frac{C[v_C(T/2) - v_C(0)]}{T} \ . \tag{6}$$

The clock waveforms of Fig. 9.1-2 applied to the parallel switched capacitor circuit of Fig. 9.1-1(a), show that the voltage $v_C(T/2)$ is equal to the value of $v_1(T/2)$ and the value of $v_C(0)$ is equal to the value of $v_2(0)$. Therefore, Eq. (6) becomes

$$i_1(average) = \frac{C[v_1(T/2) - v_2(0)]}{T} \ . \tag{7}$$

However, if $v_1(t)$ and $v_2(t)$ are approximately constant over the period T, then

$$v_1(0) \approx v_1(T/2) \approx v_1(T) \approx V_1 \tag{8}$$

and

$$v_2(0) \approx v_2(T/2) \approx v_2(T) \approx V_2 \ . \tag{9}$$

$v_1(t)$ and $v_2(t)$ can be considered a constant over a clock period, T, if the signal frequency is much less than the clock frequency. Substituting the approximations of Eqs. (8) and (9) into Eq. (7) gives the average current flowing into the capacitor C as

$$i_1(average) = \frac{C(V_1 - V_2)}{T}. \tag{10}$$

Now let us find the average current, $i_1(average)$, flowing into the resistor R of Fig. 9.1-1(b). This value is easily written as

$$i_1(average) = \frac{V_1 - V_2}{R}. \tag{11}$$

Equating the average currents of Eqs. (10) and (11) gives the desired result of

$$R = \frac{T}{C}. \tag{12}$$

Eq. (12) shows that the parallel switched capacitor circuit of Fig. 9.1-1(a) is equivalent to a resistor if the changes in $v_1(t)$ and $v_2(t)$ can be neglected during the period T. It is noted that the parallel switched capacitor resistor emulation is a three-terminal network that emulates a resistance between two ungrounded terminals.

Example 9.1-1

Design of a Parallel Switched Capacitor Resistor Emulation

If the clock frequency of Fig. 9.1-1(a) is 100kHz, find the value of the capacitor C that will emulate a 1MΩ resistor.

Solution

The period of a 100kHz clock waveform is 10μsec. Therefore, using Eq. (12) we get that

$$C = \frac{T}{R} = \frac{10^{-5}}{10^{6}} = 10pF$$

We know from previous considerations that the area required for 10pF capacitor is much less than for a 1MΩ resistor when implemented in CMOS technology.

Figure 9.1-3 shows three more switched capacitor circuits that can emulate a resistor. Fig. 9.1-3(a) is called a *series switched capacitor resistor*, Fig. 9.1-3(b) is called a *series-parallel switched capacitor resistor*, and Fig. 9.1-3(c) is called the *bilinear switched capacitor resistor*. Note that the series and bilinear switched capacitor resistor circuits are two-terminal rather than three-terminal. It can be shown that the equivalent resistance of the series switched capacitor resistor circuit is given by Eq. (12). We will illustrate how to find the equivalent resistance of the series-parallel switched capacitor resistor circuit of Fig. 9.1-3(b).

For the series-parallel switched capacitor resistor of Fig. 9.1-3(b), we see that the current, $i_1(t)$, flows during both the ϕ_1 and ϕ_2 clock half periods or phases. Therefore, we rewrite Eq. (1) as

$$i_1(average) = \frac{1}{T}\int_0^T i_1(t)dt = \frac{1}{T}\left(\int_0^{T/2} i_1(t)dt + \int_{T/2}^{T} i_1(t)dt\right). \tag{13}$$

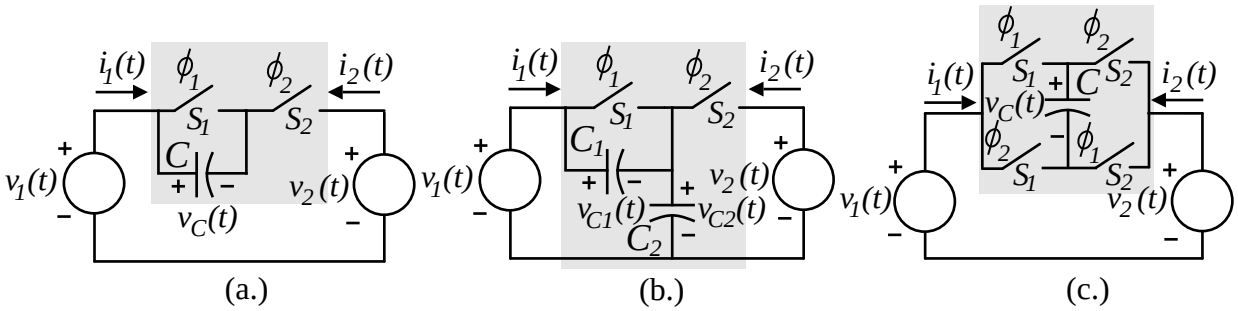


Figure 9.1-3 - Switched capacitor circuits that emulate a resistor. (a.) Series. (b.) Series-parallel. (c.) Bilinear.

Using the result of Eq. (4) we can express the average value of I_1 as

$$i_1(average) = \frac{1}{T}\int_0^{T/2} dq_1(t) + \frac{1}{T}\int_{T/2}^{T} dq_1(t) = \frac{q_1(T/2) - q_1(0)}{T} + \frac{q_1(T) - q_1(T/2)}{T} \quad (14)$$

Therefore, $i_1(average)$ can be written in terms of C_1, C_2, v_{C1}, and v_{C2} as

$$i_1(average) = \frac{C_2[v_{C2}(T/2) - v_{C2}(0)]}{T} + \frac{C_1[v_{C1}(T) - v_{C1}(T/2)]}{T} \quad . \quad (15)$$

At $t = 0$, $T/2$, and T, the capacitors in the circuit have the voltage that was last across them before S_1 and S_2 opened. Thus the sequence of switches in Fig. 9.1-3(b) cause $v_{C2}(0) = V_2$, $v_{C2}(T/2) = V_1$, $v_{C1}(T/2) = 0$, and $v_{C1}(T) = V_1 - V_2$. Applying these results to Eq. (15) gives

$$i_1(average) = \frac{C_2[V_1 - V_2]}{T} + \frac{C_1[V_1 - V_2 - 0]}{T} = \frac{(C_1 + C_2)(V_1 - V_2)}{T} \quad . \quad (16)$$

Equating Eqs. (11) and (16) gives the desired relationship which is

$$R = \frac{T}{C_1 + C_2} \quad . \quad (17)$$

Example 9.1-2

Design of a Series-Parallel Switched Capacitor Resistor Emulation

If C1 = C2 = C, find the value of C that will emulate a 1MΩ resistor if the clock frequency is 250kHz.

Solution

The period of the clock waveform is 4μsec. Using Eq. (17) we find that C is given as

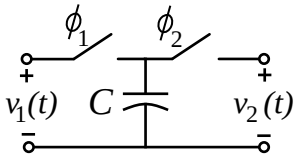
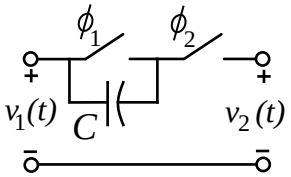
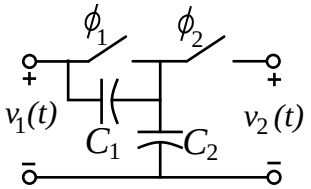
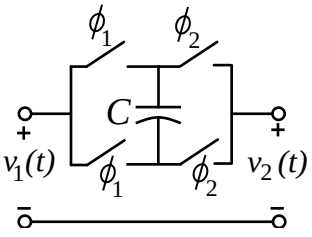
$$2C = \frac{T}{R} = \frac{4x10^{-6}}{106} = 4pF$$

Therefore, C1 = C2 = C = 2pF.

Table 9.1-1 summarizes the equivalent resistance of each of the four switched capacitor resistor emulation circuits that we have considered. It is significant to note that in each case, the emulated resistance is proportional to the reciprocal of the capacitance. This is the characteristic of switched capacitor circuits implemented in CMOS technology that yields much more accurate time constants than continuous time circuits.

Table 9.1-1

Summary of the Emulated Resistance of Four Switched Capacitor Resistor Circuits.

Switched Capacitor Resistor Emulation Circuit	Schematic	Equivalent Resistance
Parallel		$\frac{T}{C}$
Series		$\frac{T}{C}$
Series-Parallel		$\frac{T}{C_1 + C_2}$
Bilinear		$\frac{T}{4C}$

Accuracy of Switched Capacitor Circuits

The frequency or time precision of an analog signal processing circuit is determined by the accuracy of the circuit time constants. To illustrate this, consider the simple first-order, lowpass filter shown in Fig. 9.1-4. The voltage transfer function of this circuit in the frequency domain is

$$H(j\omega) = \frac{V_2(j\omega)}{V_1(j\omega)} = \frac{1}{j\omega R_1 C_2 + 1} = \frac{1}{j\omega\tau_1 + 1} \tag{18}$$

where

$$\tau_1 = R_1 C_2 \ . \tag{19}$$

τ_1 is called the *time constant* of the circuit. In order to compare the accuracy of a continuous time circuit with a discrete time, or switched capacitor circuit, let us designate τ_1 as τ_C. The accuracy of τ_C can be expressed as

$$\frac{d\tau_C}{\tau_C} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} \ . \tag{20}$$

We see that the accuracy is equal to the sum of the accuracy of the resistor, R_1, and the accuracy of the capacitor, C_2. In standard CMOS technology, the accuracy of τ_C can vary between 5% to 20% depending on the type of components and their physical size. This accuracy is not good enough for most signal processing applications.

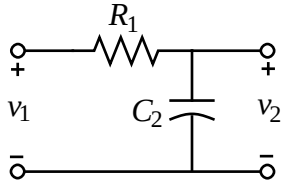


Figure 9.1-4 - Continuous time, first-order, low pass circuit.

Now let us consider the case where the resistor, R_1, of Fig. 9.1-4 is replaced by one of the switched capacitor circuits of Table 9.1-1. For example, let us select the parallel switched capacitor emulation of R_1. If we designate the time constant for this case as τ_D, then the equivalent time constant can be written as

$$\tau_D = \left(\frac{T}{C_1}\right) C_2 \ = \left(\frac{1}{f_c C_1}\right) C_2 \tag{21}$$

where f_c is the frequency of the clock. The accuracy of τ_D can be expressed as

$$\frac{d\tau_D}{\tau_D} = \frac{dC_2}{C_2} - \frac{dC_1}{C_1} - \frac{df_c}{f_c} \ . \tag{22}$$

This is an extremely significant result. It states that the accuracy of the discrete time constant, τ_D, is equal to the relative accuracy of C_1 and C_2 and the accuracy of the clock frequency. Assuming that the clock frequency is perfectly accurate, then the accuracy of τ_D can be as small as 0.1% in standard CMOS technology. This accuracy is more than sufficient for most signal processing applications and is the primary reason for the widespread use of switched capacitor circuits in CMOS technology.

Analysis Methods for Switched Capacitor Circuits using Two-phase, Nonoverlapping Clocks

Switched capacitor circuits are often called analog sampled data circuits because the signals are continuous in amplitude and discrete in time. An arbitrary continuous time voltage waveform, *v(t)*, is shown on Fig. 9.1-5 by the gray line. At the time *t = 0, T/2, T, 3T/2, ...* this voltage has been sampled and held for a half-period (*T/2*). The sampled data waveform, *v*(t)*, of Fig. 9.1-5(a) is typical of a switched capacitor waveform assuming that the input signal to the switched capacitor circuit has been sampled and held. The

shaded and unshaded rectangles correspond to the ϕ_1 phase and the ϕ_2 phase, respectively, of the two-phase of the nonoverlapping clock of Fig. 9.1-2.

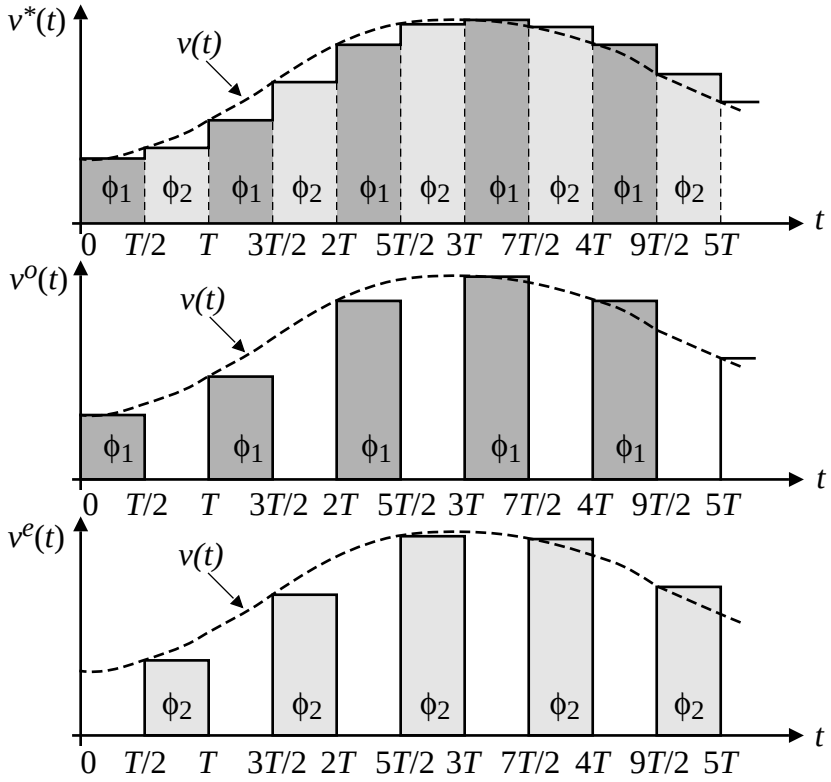


Figure 9.1-5 - (a.) A sampled data voltage waveform for a two-phase clock. (b.) Waveform for the odd clock (ϕ_1). (c.) Waveform for the even clock (ϕ_2).

It is clear from Fig. 9.1-5 that the Fig. 9.1-5(a) is equal to the sum of Figs. 9.1-5(b) and 9.1-5(c). This relationship can be expressed as

$$v^*(t) = v^o(t) + v^e(t) \tag{23}$$

where the superscript *o* denotes the odd phase (ϕ_1) and the superscript *e* denotes the even phase (ϕ_2). For any given sample point, $t = nT/2$, Eq. (23) may be expressed as

$$v^*(nT/2) = v^o\left((n\text{-}1)\frac{T}{2}\right) + v^e\left((n\text{-}1)\frac{T}{2}\right) \tag{24}$$

where for the odd phase, n = 1,3,5,⋯ and for the even phase, n = 2,4,6,⋯.

To examine switched capacitor circuits in the frequency domain, it is necessary to transform the sequence in the time domain to a z-domain equivalent expression. To illustrate, consider the one-sided z-transform of a sequence, $v(nT)$, defined as [5]

$$V(z) = \sum_{n=0}^{\infty} v(nT)z^{-n} = v(0) + v(T)z^{-1} + v(2T)z^{-2} + \cdots \tag{25}$$

for all z for which the series $V(z)$ converges. Now, Eq. (23) can be expressed in the z-domain as

$$V^*(z) = V^o(z) + V^e(z) \; . \tag{26}$$

The z-domain format for switched capacitor circuits allows one to analyze transfer functions.

A switched capacitor circuit viewed from a z-domain viewpoint is shown in Fig. 9.1-6. Both, the input voltage , $V_i(z)$, and output voltage, $V_o(z)$, can be decomposed into its odd and even component voltages. Depending on whether the odd or even voltages are selected, there are four possible transfer functions. In general they are expressed as

$$H^{ij}(z) = \frac{V_o^j(z)}{V_i^i(z)} \tag{27}$$

where i and j can be either e or o. For example, $H^{oe}(z)$ represents $V_o^e(z)/V_i^o(z)$. Also, a transfer function, H(z) can be defined as

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{V_o^e(z) + V_o^o(z)}{V_i^e(z) + V_i^o(z)} \; . \tag{28}$$

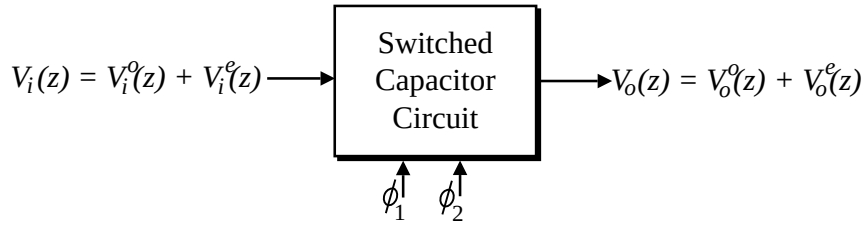


Figure 9.1-6 - Input-output voltages of a general switched capacitor circuit in the z-domain.

The analysis approach for switched capacitor circuits using a two-phase, nonoverlapping clock consists of analyzing the circuit in the time-domain during a selected phase period. Because the circuit consists of only capacitors (charged and uncharged) and voltage sources, the equations are easy to derive using simple algebraic methods. Once the selected phase period has been analyzed, then the following phase period is analyzed carrying over the initial conditions from the previous analysis. At this point, a time-domain equation can be found that relates the output voltage during the second period to the inputs during either of the phase periods. Next, the time-domain equation is converted to the z-domain using Eq. (25). The desired z-domain transfer function can be found from this expression. The following example will illustrate this approach.

It is convenient to associate a point in time with each clock phase. The obvious choices are at the beginning of the clock phase or the end of the clock phase. We will arbitrarily choose the beginning of the clock phase. However, one could equally well choose the end of the clock phase. The key is to be consistent thoughout a given analysis. In the following example, the time point is selected as the beginning of the phase period as indicated by the single parenthesis in Fig. 9.1-7b associating the beginning of the phase period with that phase period.

Example 9.1-3

Analysis of a Switched Capacitor, First-order, Lowpass Filter

Use the above approach to find the z-domain transfer function of the first-order, lowpass switched capacitor circuit shown in Fig. 9.1-7a. This circuit was developed by replacing the resistor, R_1, of Fig. 9.1-4 with the parallel switched capacitor resistor circuit of Table 9.1-1. Fig. 9.1-7b gives the timing of the clocks. This timing is arbitrary and is used to assist the analysis and does not change the result.

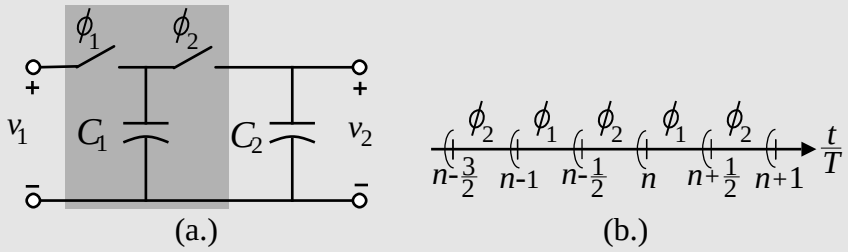


Figure 9.1-7 (a.) Switched capacitor, lowpass filter. (b.) Clock phasing.

Solution

Let us begin with the ϕ_1 phase during the time interval from $(n\text{-}1)T$ to $(n\text{-}1/2)T$. Fig. 9.1-8a is the equivalent of Fig. 9.1-7a during this time period. During this time period, C_1, is charged to $v_1^o\ (n\text{-}1)T$. However, C_2, remains at the voltage of the previous period, $v_2^e\ (n\text{-}3/2)T$. Fig. 9.1-8(b) show a useful simplification to Fig. 9.1-8a by replacing C_2 which has been charged to $v_2^e\ (n\text{-}3/2)T$ by an uncharged capacitor, C_2, in series with a voltage source of $v_2^e\ (n\text{-}3/2)T$. This voltage source is a step function that starts at $t = (n\text{-}3/2)$T. Because there is no voltage across C_2, then

$$v_2^o(n\text{-}1)T = v_2^e\ (n\text{-}3/2)T. \tag{29}$$

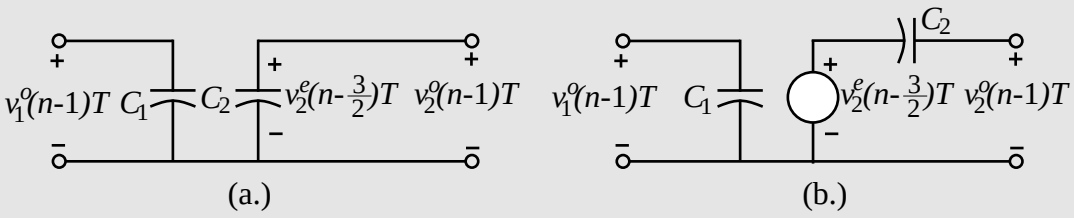


Figure 9.1-8 (a.) Equivalent circuit of Fig. 9.1-7(a.) during the period from $t = (n\text{-}1)T$ to $t = (n\text{-}3/2)T$. (b.) Simplified equivalent of Fig. 9.1-8(a.).

Now, let us consider the next clock period, ϕ_2, during the time from $t = (n\text{-}1/2)T$ to $t = nT$. The equivalent circuit of Fig. 9.1-7a during this period is shown in Fig. 9.1-9. We see that C_1 with its previous charge of $v_1^o\ (n\text{-}1)T$ is connected in parallel with C_2 which has the voltage given by Eq. (29). Thus, the output of Fig. 9.1-9 can

be expressed as the superposition of two voltage sources, $v_1^o\ (n\text{-}1)T$ and $v_2^o\ (n\text{-}1)T$ given as

$$v_2^e\ (n\text{-}1/2)T = \left(\frac{C_1}{C_1+C_2}\right)v_1^o\ (n\text{-}1)T + \left(\frac{C_2}{C_1+C_2}\right)v_2^o\ (n\text{-}1)T. \tag{30}$$

If we advance Eq. (29) by one full period, T, it can be rewritten as

$$v_2^o(n)T = v_2^e\ (n\text{-}1/2)T. \tag{31}$$

Substituting, Eq. (30) into Eq. (31) yields the desired result given as

$$v_2^o\ (nT) = \left(\frac{C_1}{C_1+C_2}\right)v_1^o\ (n\text{-}1)T + \left(\frac{C_2}{C_1+C_2}\right)v_2^o\ (n\text{-}1)T. \tag{32}$$

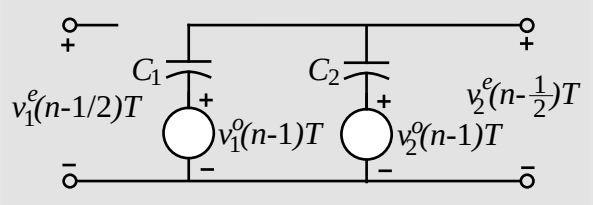


Figure 9.1-9 - Equivalent circuit of Fig. 9.1-7a during the time from $t = (n\text{-}1/2)T$ to $t = nT$.

The next step is to write the z-domain equivalent expression for Eq. (32). This can be done term by term using the sequence shifting property given as

$$v(n\text{-}n_1)T \leftrightarrow z^{n_1 T}V(z)\ . \tag{33}$$

The result is

$$z^{n\,T}\,V_2^o(z) = \left(\frac{C_1}{C_1+C_2}\right)z^{(n\text{-}1)T}\,V_1^o(z) + \left(\frac{C_2}{C_1+C_2}\right)z^{(n\text{-}1)T}\,V_2^o(z)\ . \tag{34}$$

Factoring out $z^{n\,T}$, gives

$$V_2^o(z) = \left(\frac{C_1}{C_1+C_2}\right)z^{-T}\,V_1^o(z) + \left(\frac{C_2}{C_1+C_2}\right)z^{-T}\,V_2^o(z). \tag{35}$$

Assume that $T = 1$ second so that Eq. (35) becomes,

$$V_2^o(z) = \left(\frac{C_1}{C_1+C_2}\right)z^{-1}\,V_1^o(z) + \left(\frac{C_2}{C_1+C_2}\right)z^{-1}\,V_2^o(z). \tag{36}$$

Finally, solving for $V_2^o(z)/V_1^o(z)$ gives the desired z-domain transfer function for the switched capacitor circuit of Fig. 9.1-7a as

$$H^{oo}(z) = \frac{V_2^o(z)}{V_1^o(z)} = \frac{z^{-1}\left(\frac{C_1}{C_1+C_2}\right)}{1 - z^{-1}\left(\frac{C_2}{C_1+C_2}\right)} = \frac{z^{-1}}{1 + \alpha - \alpha z^{-1}} \tag{37}$$

where

$$\alpha = \frac{C_2}{C_1}. \tag{38}$$

The above example illustrates the approach of finding the *z*-domain transfer function of switched capacitor circuits. In general, one tries to find the transfer function corresponding to even or odd phase at the output and input, i.e. $H^{oo}(z)$ or $H^{ee}(z)$. However, in some cases, $H^{oe}(z)$ or $H^{eo}(z)$ is used.

The frequency response of a continuous time circuit can be found from the complex frequency transfer function, H(s), given as

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} \tag{39}$$

where *s* is the familiar complex frequency variable defined as

$$s = \sigma + j\omega \tag{40}$$

where σ is the real part and ω is the imaginary part of the complex frequency variable *s*. The *s* domain is shown in Fig. 9.1-10a. The continuous time frequency response is found when $\sigma = 0$ or $s = j\omega$. The *z*-domain variable is also a complex variable expressed as

$$z = re^{j\omega T} \tag{41}$$

where *r* is the radius from the origin to a point, ω is the radian frequency variable in radians per second and *T* is the clock period in seconds. The z domain is shown in Fig. 9.1-10b. The discrete time frequency response is found by letting $r = 1$. We see that the continuous time frequency response corresponds to the vertical axis of Fig. 9.1-10a and the discrete time frequency response corresponds to the unit circle of Fig. 9.1-10b. Therefore, to find the frequency response of a discrete time or switched capacitor circuit, we replace the *z* variable with $e^{j\omega T}$ and evaluate the result as a function of ω. The following example will illustrate the method.

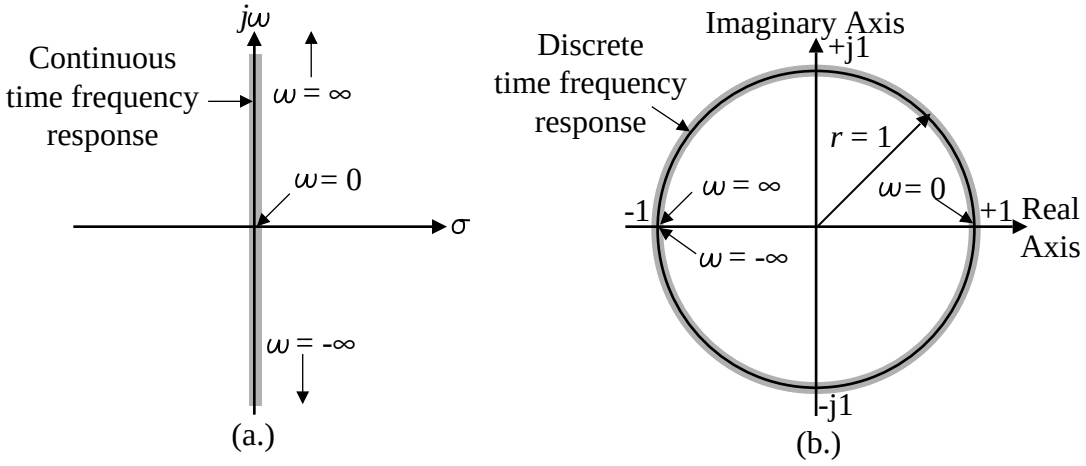


Figure 9.1-10 (a.) Continuous frequency domain. (b.) Discrete frequency domain.

Example 9.1-4

Frequency Response of Example 9.1-3

Use the results of the previous example to find the magnitude and phase of the discrete time frequency response for the switched capacitor circuit of Fig. 9.1-7a.

Solution

The first step is to replace z in Eq. (37) by $e^{j\omega T}$. The result is given below as

$$H^{oo}(e^{j\omega T}) = \frac{e^{-j\omega T}}{1+\alpha-\alpha\, e^{-j\omega T}} = \frac{1}{(1+\alpha)e^{j\omega T}-\alpha} = \frac{1}{(1+\alpha)cos(\omega T)-\alpha+j(1+\alpha)sin(\omega T)} \quad (42)$$

where we have used Eulers formula to replace $e^{j\omega T}$ by $cos(\omega T)+jsin(\omega T)$. The magnitude of Eq. (42) is found by taking the square root of the square of the real and imaginary components of the denominator to give

$$|H^{oo}| = \frac{1}{\sqrt{(1+\alpha)^2cos^2(\omega T) - 2\alpha(1+\alpha)cos(\omega T) + \alpha^2 + (1+\alpha)^2sin^2(\omega T)}}$$

$$= \frac{1}{\sqrt{(1+\alpha)^2[cos^2(\omega T)+sin^2(\omega T)]+\alpha^2-2\alpha(1+\alpha)cos(\omega T)}}$$

$$= \frac{1}{\sqrt{1+2\alpha + 2\alpha^2 -2\alpha(1+\alpha)cos(\omega T)}} = \frac{1}{\sqrt{1+2\alpha(1+\alpha)(1-cos(\omega T))}} . \quad (43)$$

The phase shift of Eq. (42) is expressed as

$$\text{Arg}[H^{oo}] = -\tan^{-1}\left[\frac{(1+\alpha)sin(\omega T)}{(1+\alpha)cos(\omega T)-\alpha}\right] = -\tan^{-1}\left[\frac{sin(\omega T)}{cos(\omega T) - \frac{\alpha}{1+\alpha}}\right] \quad (44)$$

Once the frequency response of the switched capacitor circuit has been found, it is necessary to design any of the circuit parameters. In the previous two examples, α which is the ratio of C_2 to C_1, is a circuit parameter. The design is typically done by assuming that the frequency of the signal applied to the switched capacitor circuit is much less than the clock frequency. This is called the *oversampling* assumption. It is expressed as

$$f_{signal} << f_{clock} . \quad (45)$$

If we let f_{signal} be represented as f, then we may rewrite the inequality of Eq. (45) as

$$f_{signal} = f << \frac{1}{T} . \quad (46)$$

Multiplying Eq. (46) by 2π gives

$$2\pi f = \omega << \frac{2\pi}{T} \quad (47)$$

or

$$\omega T << 2\pi. \tag{48}$$

If we use the oversampling assumption of Eq. (48), then ωT is much less than 2π and we can simplify the discrete time frequency response and equate it to the continuous time frequency response to find values for the circuit parameters. The following example illustrates this approach and completes the frequency analysis of Fig. 9.1-7a.

Example 9.1-5

Design of Switched Capacitor Circuit and Resulting Frequency Response

Design the first-order, lowpass, switched capacitor circuit of Fig. 9.1-7a to have a *-3dB* frequency at 1kHz. Assume that the clock frequency is 20kHz (The clock frequency should be higher but for illustration purposes we have chosen 20kHz.) Plot the frequency response for the resulting discrete time circuit and compare with a first-order, lowpass, continuous time filter.

Solution

If we assume that ωT is less than unity, then $cos(\omega T)$ approaches 1 and $sin(\omega T)$ approaches ωT. Substituting these approximations into the magnitude response of Eq. (42) results in

$$H^{oo}(e^{j\omega T}) \approx \frac{1}{(1+\alpha) - \alpha + j(1+\alpha)\omega T} = \frac{1}{1 + j(1+\alpha)\omega T}. \tag{49}$$

Comparing this equation to Eq. (18) results in the following relationship which permits the design of the circuit parameter α.

$$\omega\tau_1 = (1+\alpha)\omega T \tag{50}$$

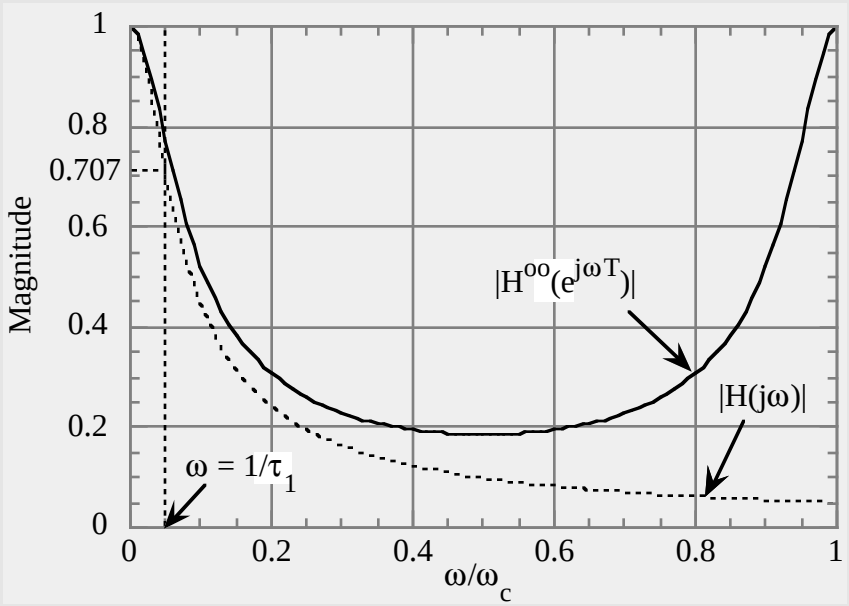
Solving for α gives

$$\alpha = \frac{\tau_1}{T} - 1 = f_c\tau_1 - 1 = \frac{f_c}{\omega_{-3dB}} - 1 = \frac{\omega_c}{2\pi\omega_{-3dB}} - 1 . \tag{51}$$

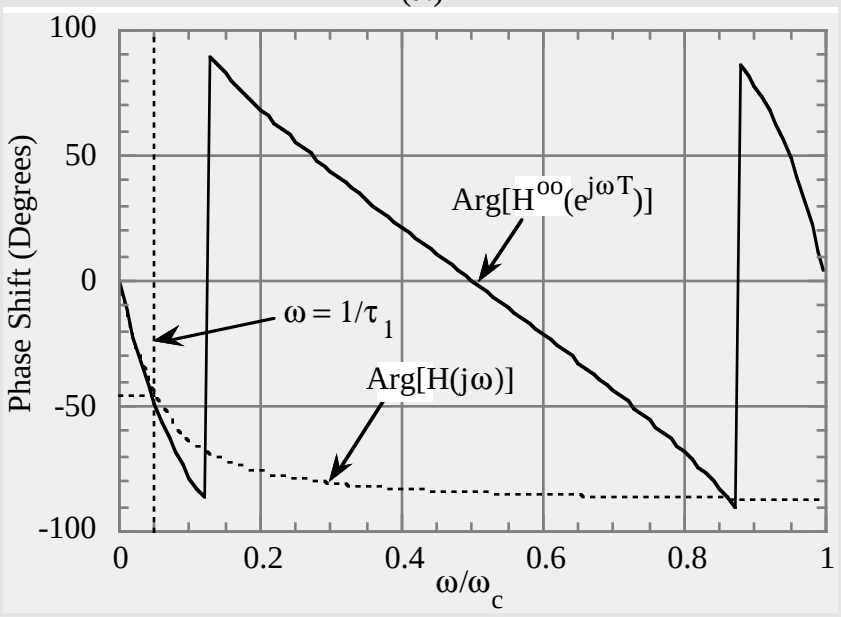
Using the values given in the example, we see that α = (20/6.28)-1 =2.1831. Therefore, $C_2 = 2.1831C_1$.

The magnitude and phase response of the continuous and discrete time, first-order, lowpass circuits are shown on Fig. 9.1-11. We note that for ω small, both the continuous time, $H(j\omega)$, and discrete time, $H^{oo}e^{j\omega T}$ frequency responses are almost identical. However, as ω increases, the discrete time frequency response deviates from the continuous time response. An important characteristic of a discrete time frequency magnitude response in Fig. 9.1-11a, is that it is repeated at the clock frequency and each harmonic of the clock frequency. Thus, we note that $\omega = 0.5\omega_c$, that the discrete time magnitude response reaches a minimum and increases back to

the value at ω_c that it had at $\omega = 0$. Because, ω_1 (= 2000π) is not much less than ω_c, the discrete time response deviates even at the *-3dB* frequency. This match could be improved by simply choosing a higher clock frequency such as 100kHz. The phase response shows good match between the two circuits at frequencies below $0.1\omega_c$. Above that frequency, the discrete time phase response becomes much larger than the continuous time phase response. The discrete time phase response at ω_c is similar to that at $\omega = 0$, however the phase shifted by an amount of -360° or -2π.



(a.)



(b.)

Figure 9.1-11 Frequency response of the continuous time low pass filter of Fig. 9.1-4 and the discrete time low pass filter of Fig. 9.1-7a. (a.) Magnitude response. (b.) Phase response.

The analysis of Fig. 9.1-7a illustrated through Examples 9.1-3, 9.1-4, and 9.1-5 show how to analyze a general discrete-time circuit. If the discrete time circuits become very complex, this method can be tedious and error-prone. Fortunately, most switched capacitor circuits are closely associated with op amps which reduces the complexity and results in circuits that are similar in complexity compared to the one illustrated above. The problems at the end of the chapter will provide other analysis opportunities.

9.2 Switched Capacitor Amplifiers

In this section, the use of switched capacitors for amplification will be presented. This class of circuits will use the op amp with negative feedback to achieve gains that are proportional to the ratios of capacitors. We will begin with amplifiers using resistor feedback. These amplifiers will serve as the basis for switched capacitor amplifiers. The influence of the op amp open-loop gain and unity-gainbandwidth on these amplifiers will be examined.

Continuous Time Amplifiers

Figure 9.2-1 shows the familiar noninverting and inverting amplifiers using resistors and op amps. The ideal gain of both circuits can be easily be found [6]. For the noninverting amplifier of Fig. 9.2-1a, the ideal gain is

$$\frac{v_{OUT}}{v_{IN}} = \frac{R_1+R_2}{R_1} \tag{1}$$

and for the inverting amplifier of Fig. 9.2-1b, the ideal gain is

$$\frac{v_{OUT}}{v_{IN}} = -\frac{R_2}{R_1}. \tag{2}$$

The results of Eqs. (1) and (2) assume that the differential gain of the op amps in Fig. 9.2-1 approach infinity.

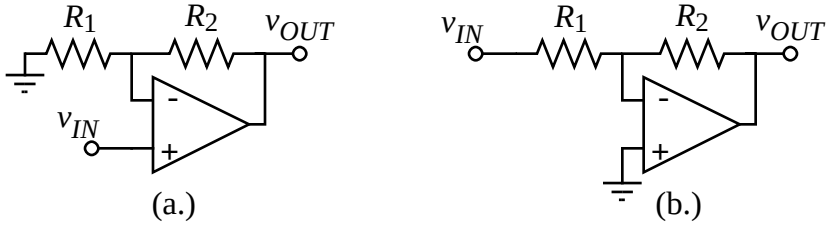


Figure 9.2-1 - (a.) Continuous time noninverting amplifier. (b.) Continous time inverting amplifier.

Figure 9.2-1 - (a.) Continuous time noninverting amplifier. (b.) Continuous time inverting amplifier.

The influence of a finite gain and finite unity-gainbandwidth can be seen by replacing the op amps of Fig. 9.2-1 with a the voltage-controlled, voltage source model shown in Fig. 9.2-2. The voltage gain, $A_{vd}(s)$ is a function of the complex frequency variable, s, and is given as

$$A_{vd}(s) = \frac{A_{vd}(0)\omega_a}{s+\omega_a} = \frac{GB}{s+\omega_a} \approx \frac{GB}{s} \quad \text{if } \omega >> \omega_a \tag{3}$$

where $A_{vd}(0)$ is the low-frequency differential voltage gain, GB is the *unity-gainbandwidth,* and ω_a is the *-3dB* frequency of the op amp. The influence of $A_{vd}(0)$ can be examined by letting s in Eq. (3) approach zero. Solving for the voltage gains of the op

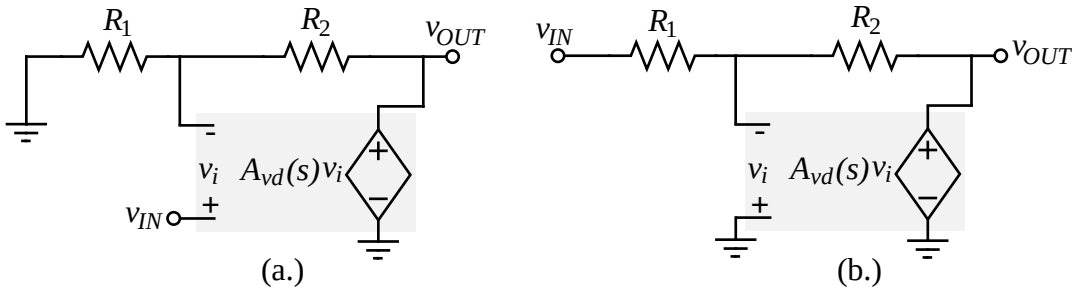


Figure 9.2-2 - Model for the (a.) noninverting and (b.) inverting voltage amplifiers that includes finite gain and finite unity-gainbandwidth.

amp configurations in Fig. 9.2-2 with $A_{vd}(s)$ equal $A_{vd}(0)$ gives the following results. For the noninverting amplifier we obtain,

$$\frac{V_{out}}{V_{in}} = \frac{A_{vd}(0)}{1+\frac{A_{vd}(0)R_1}{R_1+R_2}} = \left(\frac{R_1+R_2}{R_1}\right)\frac{\frac{A_{vd}(0)\,R_1}{R_1+R_2}}{1+\frac{A_{vd}(0)R_1}{R_1+R_2}} = \left(\frac{R_1+R_2}{R_1}\right)\frac{LG}{1+LG} \tag{4}$$

where the magnitude of the feedback loop gain, LG, is given as

$$LG = \frac{A_{vd}(0)R_1}{R_1+R_2}. \tag{5}$$

The result for the inverting amplifier is,

$$\frac{V_{out}}{V_{in}} = \frac{\frac{-R_2A_{vd}(0)}{R_1+R_2}}{1+\frac{A_{vd}(0)R_1}{R_1+R_2}} = -\left(\frac{R_2}{R_1}\right)\frac{\frac{R_1A_{vd}(0)}{R_1+R_2}}{1+\frac{A_{vd}(0)R_1}{R_1+R_2}} = -\left(\frac{R_2}{R_1}\right)\frac{LG}{1+LG}. \tag{6}$$

It is noted that as $A_{vd}(0)$ or LG becomes large, that Eqs. (4) and (6) approach Eqs. (1) and (2), respectively.

Example 9.2-1

Accuracy Limitation of Voltage Amplifiers due to a Finite Voltage Gain

Assume that the voltage amplifiers of Fig. 9.2-1 have been designed for a voltage gain of +10 and -10. If $A_{vd}(0)$ is 1000, find the actual voltage gains for each amplifier.

Solution

For the noninverting amplifier, the ratio of R_2/R_1 is 9. Therefore, from Eq. (5) the feedback loop gain becomes LG = 1000/(1+9) = 100. From Eq. (4), the actual gain is 10(100/101) = 9.901 rather than 10. For the inverting amplifier, the ratio of R_2/R_1 is 10. In this case, the feedback loop gain is LG = 1000/(1+10) = 90.909. Substituting this value in Eq. (6) gives an actual gain of -9.891 rather than -10.

A finite value of $A_{vd}(0)$ in Eq. (3) will influence the accuracy of the amplifiers gain at dc and low frequencies. As the frequency increases, a finite value of *GB* in Eq. (3) will influence the amplifier's frequency response. Before repeating the above analysis, let us assume that ω is much greater than ω_a so that we may use the approximation for $A_{vd}(s)$ given in Eq. (3), i.e. $A_{vd}(s) \approx GB/s$. Replacing $A_{vd}(0)$ in Eqs. (4) and (6) by GB/s results in the following expression for the noninverting amplifier

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{R_1+R_2}{R_1}\right)\frac{\frac{GB\cdot R_1}{R_1+R_2}}{s+\frac{GB\cdot R_1}{R_1+R_2}} = \left(\frac{R_1+R_2}{R_1}\right)\frac{\omega_H}{s+\omega_H} \tag{7}$$

where ω_H is the upper -3*dB* frequency and is given as

$$\omega_H = \frac{GB\cdot R_1}{R_1+R_2}. \tag{8}$$

The equivalent expression for the inverting amplifier is given below.

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(-\frac{R_2}{R_1}\right)\frac{\frac{GB\cdot R_1}{R_1+R_2}}{s+\frac{GB\cdot R_1}{R_1+R_2}} = \left(-\frac{R_2}{R_1}\right)\frac{\omega_H}{s+\omega_H} \tag{9}$$

Example 9.2-2

-3*dB* Frequency of Voltage Amplifiers due to Finite Unity-Gainbandwidth

Assume that the voltage amplifiers of Fig. 9.2-1 have been designed for a voltage gain of +1 and -1. If the unity-gainbandwidth, *GB*, of the op amps in Fig. 9.2-1 are 2πMrads/sec, find the upper -3*dB* frequency for each amplifier.

Solution

In both cases, the upper -3*dB* frequency is given by Eq. (8). However, for the noninverting amplifier with an ideal gain of +1, the value of R_2/R_1 is zero. Therefore, the upper -3*dB* frequency, ω_H, is equal to *GB* or 2πMrads/sec (1Mhz). For the inverting amplifier with an ideal gain of -1, the value of R_2/R_1 is one. Therefore, ω_H is equal to *GB*/2 or πMrads/sec (500kHz).

Charge Amplifiers

Before we consider switched capacitor amplifiers, let us examine a category of amplifiers called *charge amplifiers*. Charge amplifiers simply replace the resistors of Fig. 9.2-1 by capacitors resulting in Fig. 9-2-3. All the relationships summarized above hold if the resistor is replaced by the reciprocal capacitor. For example, the influence of the low-frequency, differential voltage gain, $A_{vd}(0)$, given in Eqs. (4), (5) and (6) become

$$\frac{V_{out}}{V_{in}} = \left(\frac{C_1+C_2}{C_2}\right)\frac{LG}{1+LG}, \tag{10}$$

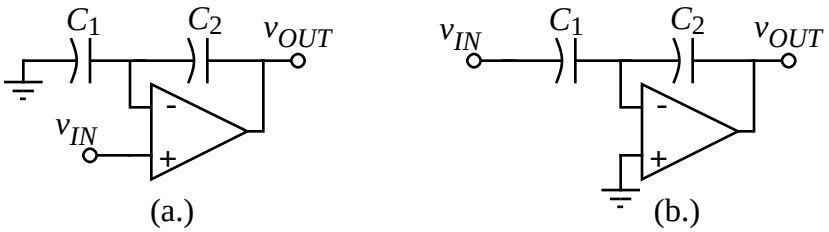


Figure 9.2-3 - (a.) Noninverting charge amplifier. (b.) Inverting charge amplifier.

$$LG = \frac{A_{vd}(0)C_2}{C_1+C_2}, \tag{11}$$

and

$$\frac{V_{out}}{V_{in}} = -\left(\frac{C_1}{C_2}\right)\frac{LG}{1+LG}, \tag{12}$$

respectively. The influence of the unity-gainbandwidth, *GB*, given in Eqs. (7), (8), and (9) becomes

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{C_1+C_2}{C_2}\right)\frac{\omega_H}{s+\omega_H}, \tag{13}$$

$$\omega_H = \frac{GB\cdot C_2}{C_1+C_2}, \tag{14}$$

and

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(-\frac{C_1}{C_2}\right)\frac{\omega_H}{s+\omega_H}. \tag{15}$$

The major difference between the charge amplifiers of Fig. 9.2-3 and the voltage amplifiers of Fig. 9.2-1 occurs as a function of time. If the inputs to the charge amplifiers remains constant, eventually the leakage currents will cause the voltage across the capacitors to change. This will result in the output voltage of the op amp becoming equal to either its plus or minus limit. At this point, the feedback loop around the op amp is no longer active and the above equations no longer hold. Thus, one of the requirements for charge amplifiers is that voltage across the capacitor is redefined often enough so that leakage currents have no influence. It turns out in switched capacitor circuits that the voltages are redefined at least once every clock cycle. Therefore, charge amplifiers find use in switched capacitor circuits as voltage amplifiers.

Switched Capacitor Amplifiers

At first thought, it may seem like the charge amplifiers above can serve as amplifiers for switched capacitor circuits. While this is true there are several reasons for examining a switched capacitor amplifier that uses op amps, switches, and capacitors. The first is that there is a difference between the performance of switched capacitor amplifiers and charge amplifiers. Secondly, switched capacitor amplifiers are a natural step in the development of switched capacitor integrators which are an important objective of this

chapter. For the present, we will consider only a switched capacitor implementation of the inverting voltage amplifier of Fig. 9.2-1b.

Figure 9.2-4 shows the evolution of an inverting switched capacitor amplifier. The resistors of the inverting voltage amplifier of Fig. 9.2-1b are replaced by the parallel switched capacitor resistor emulation of Fig. 9.1-1 or of Table 9.1-1 resulting in Fig. 9.2-4a. Unfortunately, during the ϕ_2 phase period, the feedback loop around the op amp is broken. This is undesirable and causes the output voltage of the op amp to needlessly fluctuate. It turns out that if we select the bilinear switched capacitor resistor emulation for R_2, that this problem is avoided. However, the bilinear switched capacitor resistor emulation requires four more switches. Instead, we chose a slight modification of the series switched capacitor resistor emulation as shown in Fig. 9.2-4b. In this case we have kept the ϕ_2 switch of the series switched capacitor resistor emulation closed during the clock cycle which means that this switch is not needed.

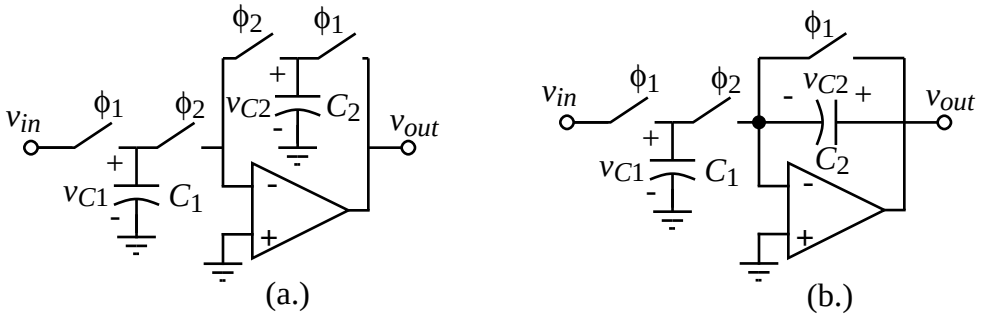


Figure 9.2-4 - (a.) Switched capacitor voltage amplifier using the parallel resistor emulation. (b.) Modification of Fig. 9.2-4(a.) to make the amplifier practical.

The switched capacitor voltage amplifier of Fig. 9.2-4b can be analyzed using the methods illustrated in the previous section. It turns out that the op amp will make the analysis simpler because it reduces the number of floating nodes to zero. Let us use the clock phasing shown in Fig. 9.1-7b to guide the analysis. We begin with the ϕ_1 phase period during the time interval from $(n\text{-}1)T$ to $(n\text{-}1/2)T$. We see that during this time, C_1 is charged to $v_{in}^{o}(n\text{-}1)T$ and C_2 is discharged. Now, let us consider the next clock period, ϕ_2, during the time from $t = (n\text{-}1/2)T$ to $t = nT$. The equivalent circuit of Fig. 9.2-4b just at the moment that the ϕ_2 switch closes is shown in Fig. 9.2-5a. (For simplicity, this moment is assumed to be t = 0.) A more useful form of this circuit is given in Fig. 9.2-5b. In Fig. 9.2-5b, a step voltage source of $v_{in}^{o}(n\text{-}1)T$ is effectively applied to an inverting charge amplifier to yield the output voltage during the ϕ_2 phase period of

$$v_{out}^{e}(n\text{-}1/2)T = -\left(\frac{C_1}{C_2}\right)v_{in}^{o}(n\text{-}1)T\,. \tag{16}$$

Converting Eq. (16) to its z-domain equivalent gives

$$z^{-1/2}V_{out}^{e}(z) = -\left(\frac{C_1}{C_2}\right)z^{-1}\,V_{in}^{o}(z)\,. \tag{17}$$

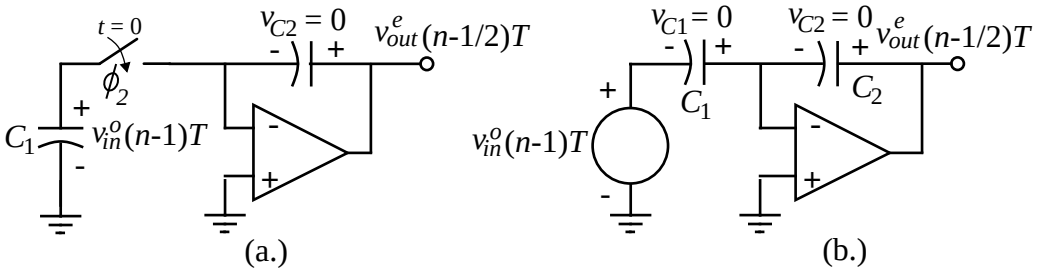


Figure 9.2-3 - (a.) Equivalent circuit of Fig. 9.2-4(b.) at the moment ϕ_2 switch closes. (b.) Simplified equivalent of Fig. 9.2-5(a.).

Multiplying Eq. (17) by $z^{1/2}$, gives

$$V^e_{out}(z) = -\left(\frac{C_1}{C_2}\right) z^{-1/2}\ V^o_{in}(z)\ . \tag{18}$$

Solving for the even-odd transfer function gives,

$$H^{oe}(z) = \frac{V^e_{out}(z)}{V^o_{in}(z)} = -\left(\frac{C_1}{C_2}\right) z^{-1/2}\ . \tag{19}$$

If we assume that applied input signal, $v^o_{in}(n\text{-}1)T$, was unchanged during the previous ϕ_2 phase period (from $t = (n\text{-}3/2)T$ to $t = (n\text{-}1)T$), then

$$v^o_{in}(n\text{-}1)T = v^e_{in}(n\text{-}3/2)T \tag{20}$$

which gives

$$V^o_{in}(z) = z^{-1/2} V^e_{in}(z)\ . \tag{21}$$

Substituting Eq. (21) into Eq. (18) gives

$$V^e_{out}(z) = -\left(\frac{C_1}{C_2}\right) z^{-1}\ V^e_{in}(z) \tag{22}$$

or

$$H^{ee}(z) = \frac{V^e_{out}(z)}{V^e_{in}(z)} = -\left(\frac{C_1}{C_2}\right) z^{-1}\ . \tag{23}$$

As before, it is useful to compare the continuous time inverting amplifier of Fig. 9.2-1b with the switched capacitor equivalent of Fig. 9.2-4b in the frequency domain. Let us first assume ideal op amps. The frequency response of Fig. 9.2-1b has a magnitude of R_2/R_1 and a phase shift of ±180°. Both the magnitude and phase shift are independent of frequency. The frequency response of Fig. 9.2-4b is found by substituting for z by $e^{j\omega T}$ in Eq. (19) or Eq. (23). The result is

$$H^{oe}(e^{j\omega T}) = \frac{V^e_{out}(\ e^{j\omega T})}{V^o_{in}(\ e^{j\omega T})} = -\left(\frac{C_1}{C_2}\right) e^{j\omega T/2} \tag{24}$$

for Eq. (19) and

$$H^{ee}(e^{j\omega T}) = \frac{V_{out}^{e}(e^{j\omega T})}{V_{in}^{e}(e^{j\omega T})} = -\left(\frac{C_1}{C_2}\right)e^{-j\omega T} \tag{25}$$

for Eq. (23). If C_1/C_2 is equal to R_2/R_1, then the magnitude response of Fig. 9.2-4b is identical to that of Fig. 9.2-1b. However, the phase shift of Eq. (24) is

$$\text{Arg}[H^{oe}(e^{j\omega T})] = \pm 180° - \omega T/2 \tag{26}$$

and the phase shift of Eq. (25) is

$$\text{Arg}[H^{ee}(e^{j\omega T})] = \pm 180° - \omega T. \tag{27}$$

We see that the phase shift of the switched capacitor inverting amplifier starts out equal to the continuous time inverting amplifier, but experiences a linear phase delay in addition to the ±180° phase shift. The excess negative phase shift of Eq. (27) is twice that of Eq. (26). The reader can confirm that when the signal frequency is one-half of the clock frequency that the excess negative phase shift from Eq. (26) is 90° and from Eq. (27) it is 180°. In most cases, the excess negative phase shift will not be important. However, if the switched capacitor inverting amplifier is placed in a feedback loop, the excess phase shift can become a critical factor in regard to stability.

In practice, the switched capacitor inverting amplifier of Fig. 9.2-4b is influenced by the parasitic capacitors shown in Fig. 2.4-3. The bottom plate parasitic is shorted out but the top plate parasitic adds directly to the value of C_1. We observe that the parasitics of C_2 do not effect it. This is because one of the parasitic capacitors (i.e. the bottom plate) is in shunt with the op amp input which is a virtual ground and always has zero voltage across it. The other parasitic capacitor (i.e. the top plate) is in shunt with the output of the op amp and only serves as a capacitive load for the op amp.

Switched capacitor circuits have been developed that are insensitive to the capacitor parasitics [7]. Figure 9.2-6a and 9.2-6b show a positive and negative, switched capacitor *transresistor* equivalent circuit that are independent of the capacitor parasitics. These transresistors are two-port networks that take the voltage applied at one-port and create a current in the other port which has been short-circuited in this case. In our application, the short-circuited port is the port connected to the differential input of the op amp which is a virtual ground.

We see that if the switched capacitor circuits of Fig. 9.2-6 are used as transresistances, then the parasitic capacitors of C do not influence the circuit. When the ϕ_1 switches in Fig. 9.2-6a are closed, the parasitic capacitors, C_P, are shorted out and can't be charged. During the ϕ_2 phase, the parasitic capacitors are either connected in parallel with v_1 or shorted out. Even though the left-hand parasitic capacitor is charged to a value of v_1, this charge is shorted out during the next phase period, ϕ_1.

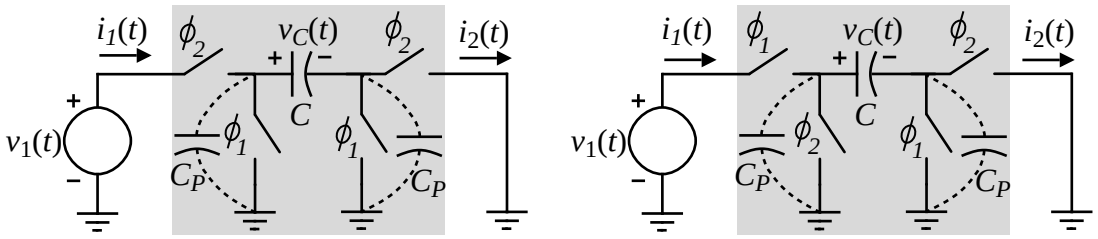


Figure 9.2-6 - (a.) Positive and (b.) negative switched capacitor transresistance equivalent circuits.

We now show that Fig. 9.2-6b is equivalent to a negative transresistance of T/C. The transresistance of Fig. 9.2-6 is defined as

$$R_T = \frac{v_1(t)}{i_2(t)} = \frac{v_1}{i_2(average)} \ . \tag{28}$$

In Eq. (28), we have assumed as before that $v_1(t)$ is approximately constant over one period of the clock frequency. Using the approach illustrated in Sec. 9.1, we can write

$$i_2(average) = \frac{1}{T}\int_{T/2}^{T} i_2(t)dt = \frac{-q_2(T) + q_2(T/2)}{T} = \frac{-Cv_C(T) + Cv_C(T/2)}{T} = \frac{-Cv_1}{T}. \tag{29}$$

Substituting Eq. (28) into Eq. (29) shows that $R_T = -T/C$. Similarly, it can be shown that the transresistance of Fig. 9.2-6a is T/C. These results are only valid when $f_c >> f$.

Using the switched capacitor transresistances of Fig. 9.2-6 in the switched capacitor inverting amplifier of Fig. 9.2-4b, we can achieve both a noninverting and an inverting switched capacitor voltage amplifier that is independent of the parasitic capacitances of the capacitors. The resulting circuits are shown in Fig. 9.2-7. We should take careful notice of the fact that the only difference between Figs. 9.2-7a and 9.2-7b are the phasing of the left-most set of switches. Note we still use the ϕ_1-C_2 circuit of Fig. 9.2-4b because the transresistance circuits of Fig. 9.2-6 would cause the feedback loop to be open during one of the clock phases. Although the circuits of Fig. 9.2-6 achieve the desired realization of switched capacitor voltage amplifiers, we must examine their performance more closely because they are slightly different from the previous circuit of Fig. 9.2-4b.

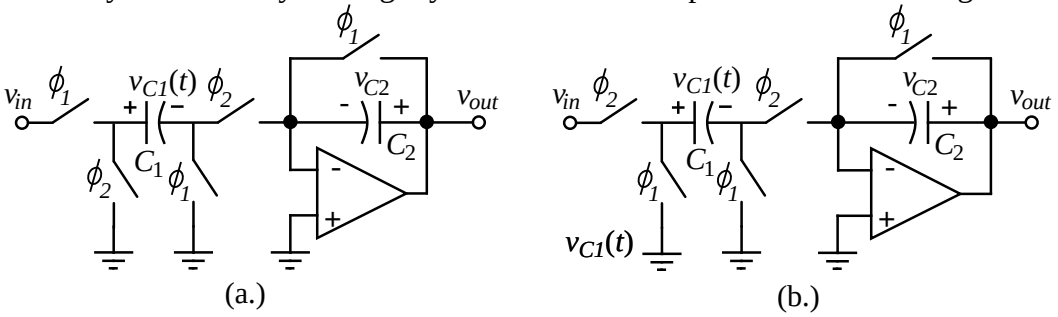


Figure 9.2-7 - (a.) Noninverting and (b.) inverting switched capacitor voltage amplifiers that are insensitive to parasitic capacitors.

Let us first examine the noninverting voltage amplifier of Fig. 9.2-7a. Using the phasing of Fig. 9.1-7b, we begin with the ϕ_1 phase during the time from $t = (n\text{-}1)T$ to $t = (n\text{-}1/2)T$. The voltages across each capacitor can be written as

$$v_{C1}^{o}(n\text{-}1)T = v_{in}^{o}(n\text{-}1)T \tag{30}$$

and

$$v_{C2}^{o}(n\text{-}1)T = v_{out}^{o}(n\text{-}1)T = 0\ . \tag{31}$$

During the ϕ_2 phase, the circuit is equivalent to the inverting charge amplifier of Fig. 9.2-3b with a negative input of $v_{in}^{o}(n\text{-}1)T$ applied. As a consequence, the output voltage can be written as

$$v_{out}^{e}(n\text{-}1/2)T = \left(\frac{C_1}{C_2}\right)v_{in}^{o}(n\text{-}1)T\ . \tag{32}$$

The z-domain equivalent of Eq. (32) is

$$V_{out}^{e}(z) = \left(\frac{C_1}{C_2}\right)z^{-1/2}\,V_{in}^{o}(z) \tag{33}$$

which is equivalent to Eq. (18) except for the sign. If the applied input signal, $v_{in}^{o}(n\text{-}1)T$, was unchanged during the previous ϕ_2 phase period, then Eq. (33) becomes

$$V_{out}^{e}(z) = \left(\frac{C_1}{C_2}\right)z^{-1}\,V_{in}^{e}(z) \tag{34}$$

which also is similar to Eq. (22) except for the sign. To summarize the comparison between Fig. 9.2-4b and Fig. 9.2-7a, we see that the magnitude is identical and the phase of Eqs. (26) and (27) is simply $-\omega T/2$ and $-\omega T$, respectively.

Next, let us examine Fig. 9.2-7b which is the inverting, voltage amplifier realization. We note that during the ϕ_1 phase, that both C_1 and C_2 are discharged. Consequently, there is no charged transferred between the ϕ_1 and ϕ_2 phase periods. During the ϕ_2 phase period, Fig. 9.2-7b is simply an inverting charge amplifier, similar to Fig. 9.2-3b. The output voltage during this phase period is written as

$$v_{out}^{e}(n\text{-}1/2)T = -\left(\frac{C_1}{C_2}\right)v_{in}^{e}(n\text{-}1/2)T\ . \tag{35}$$

We note that the output voltage has no delay with respect to the input voltage. The z-domain equivalent expression is

$$V_{out}^{e}(z) = -\left(\frac{C_1}{C_2}\right)V_{in}^{e}(z)\ . \tag{36}$$

Thus, the parasitic insensitive, inverting voltage amplifier is equivalent to an inverting charge amplifier during the phase where C_1 is connected between the input and the inverting input terminal of the op amp. Compared with Fig. 9.2-4b which is characterized by Eqs. (19) or (23), Fig. 9.2-7b has the same magnitude response but has no excess phase delay.

Example 9.2-3

Design of a Switched Capacitor Summing Amplifier

Design a switched capacitor summing amplifier using the circuits in Fig. 9.2-7 to which gives the output voltage during the ϕ_2 phase period that is equal to $10v_1$ - $5v_2$, where v_1 and v_2 are held constant during a ϕ_2-ϕ_1 period and then resampled for the next period.

Solution

Because the inverting input of the op amps in Fig. 9.2-7 is at a virtual ground, more than one capacitor can be connected to that point to transfer charge to the feedback capacitor. Therefore, a possible circuit solution is shown in Fig. 9.2-8 a positive and negative transresistance circuit has been connected to the inverting input of a single op amp.

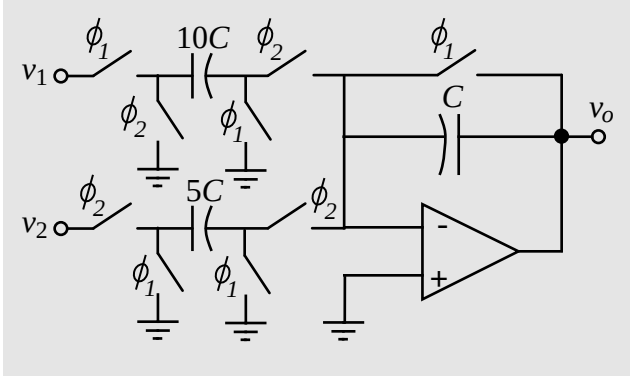


Figure 9.2-8 - A switched capacitor, voltage summing amplifier.

Considering each of the inputs separately, we can write that

$$v_{o1}^{e}(n\text{-}1/2)T = 10v_1^{o}(n\text{-}1)T \tag{37}$$

and

$$v_{o2}^{e}(n\text{-}1/2)T = -5v_2^{e}(n\text{-}1/2)T\ . \tag{38}$$

Because $v_1^{o}(n\text{-}1)T = v_1^{e}(n\text{-}3/2)T$, Eq. (37) can be rewritten as

$$v_{o1}^{e}(n\text{-}1/2)T = 10v_1^{e}(n\text{-}3/2)T\ . \tag{39}$$

Combining Eqs. (38) and (39) gives

$$v_o^{e}(n\text{-}1/2)T = v_{o1}^{e}(n\text{-}1/2)T + v_{o2}^{e}(n\text{-}1/2)T = 10v_1^{e}(n\text{-}3/2)T - 5v_2^{e}(n\text{-}1/2)T\ . \tag{40}$$

or

$$V_o^{e}(z) = 10z^{-1}V_1^{e}(z) - 5V_2^{e}(z)\ . \tag{41}$$

Eqs. (40) and (41) verifies that Fig. 9.2-8 satisfies the specifications of the example.

Nonidealities of Switched Capacitor Circuits

In Section 5.1, we noted that the MOSFET switches of the switched capacitor circuits can cause a feedthrough that results in a dc offset that can be input dependent. We next show how to analyze this influence by considering the noninverting, switched capacitor voltage amplifier of Fig. 9.2-7a. This circuit is redrawn in Fig. 9.2-9 emphasizing the overlap capacitors, C_{OL}. To simplify this consideration, we will assume that the overlap capacitances of all MOSFET switches are identical and that the threshold voltages of all MOSFET switches are equal to a value, V_T. Furthermore, we assume that the MOSFETs are n-channel with no bulk effects. The normal symbol for an n-channel MOSFET is not used because the source terminal is not defined in a switch application.

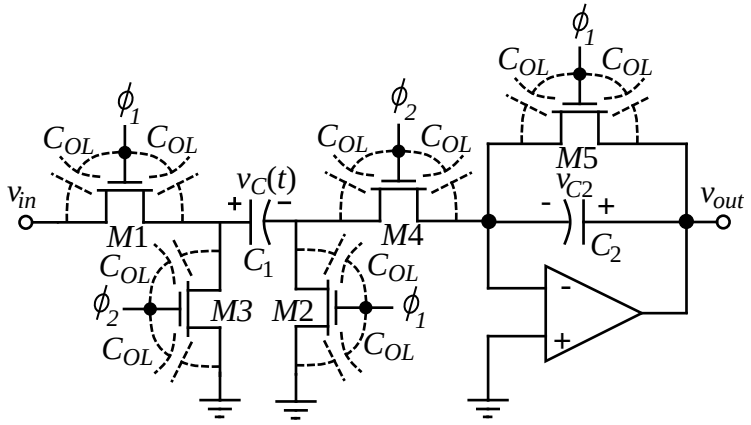


Figure 9.2-9 - Noninverting, switched capacitor voltage amplifier showing MOSFET switch overlap capacitors.

Let us consider a sequence of ϕ_1 switches closing and then opening followed by a closing and opening of the ϕ_2 switches. The first feedthrough occurs as the ϕ_1 switch turns off. Figure 9.2-10 shows an equivalent circuit that allows us to calculate the effects of feedthrough for the circuit of Fig. 9.2-9 for a complete clock period. First, let us assume that v_{in} is positive. As ϕ_1 turns off, feedthrough from C_1 (which has been charged to v_{in}) will occur via the overlap capacitors, C_{OL}, when the ϕ_1 clock is falling from the value of $v_{in}+V_T$ to 0 for M1 and the value of V_T to 0 for M2. In addition, feedthrough from C_2 will occur when the ϕ_1 clock is falling from the value of V_T to 0 for M5. The models for these two cases are shown in the second and third columns of the first row of Fig. 9.2-10. From these models we can write that

$$v_{C1}(\phi_{1off}) \approx v_{in} - \left(\frac{C_{OL}}{2C_1}\right)v_{in} \tag{42}$$

and

$$v_{C2}(\phi_{1off}) = \left(\frac{C_{OL}}{C_2}\right)V_T\,. \tag{43}$$

This analysis ignores the influence of the bulk-drain and bulk-source capacitances (see Problem 9.2-9).

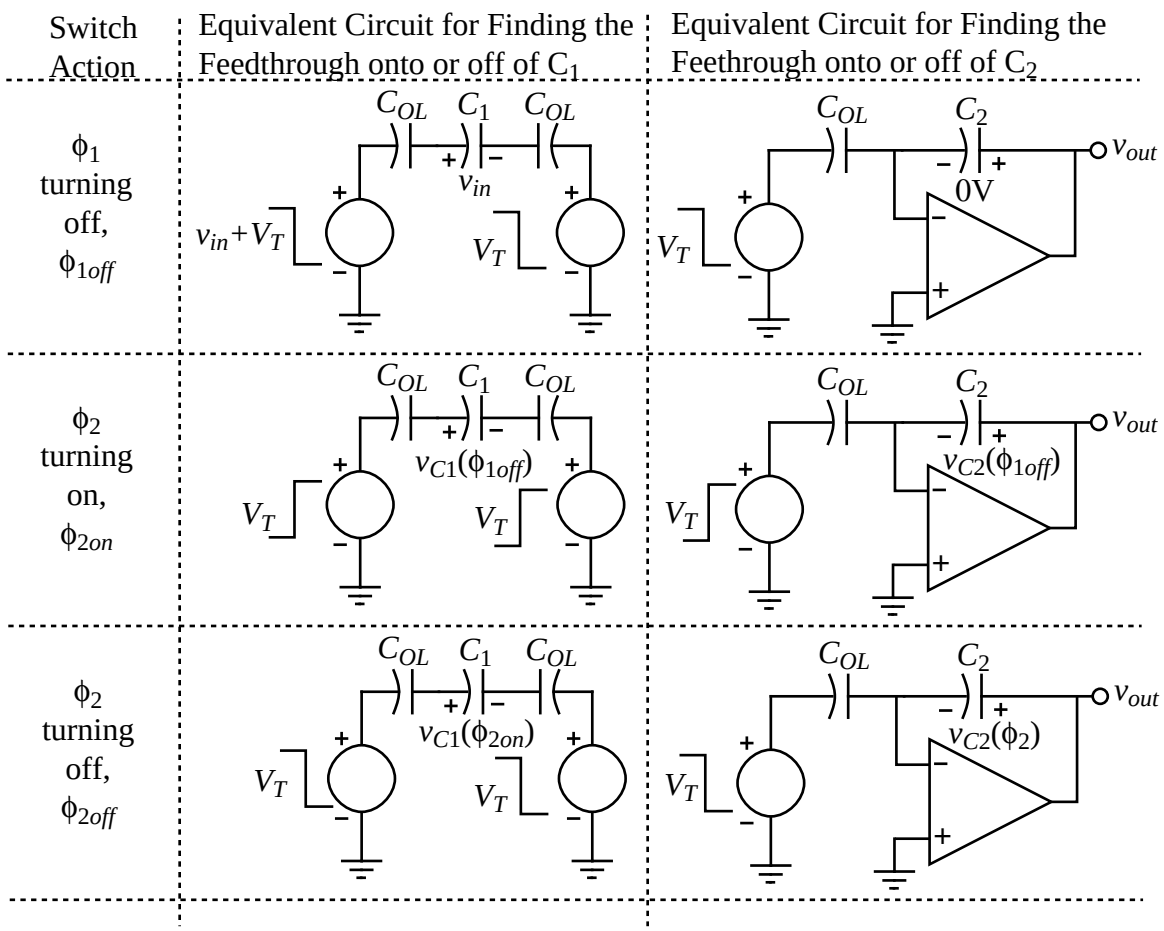


Figure 9.2-10 - Models that permit the calculation of the effects of feedthrough for a clock period.

Ideally, $v_{C1}(\phi_{1off})$ should be equal to v_{in} and $v_{C2}(\phi_{2off})$ should be zero. We see that the effects of the feedthrough due to ϕ_1 turning off is to introduce an *input dependent voltage offset* on C_1 and a dc voltage offset on C_2.

The next occurrence of feedthrough happens when the ϕ_2 switches (M3 and M4) turn on. From the value of ϕ_2 from 0 to V_T, feedthrough on to C_1 and C_2 will occur. This is modeled in the second row of Fig. 9.2-10. From these models we can write

$$v_{C1}(\phi_{2on}) \approx v_{C1}(\phi_{1off}) + \left(\frac{C_{OL}}{2C_1}\right)V_T - \left(\frac{C_{OL}}{2C_1}\right)V_T = v_{C1}(\phi_{1off}) \tag{44}$$

and

$$v_{C2}(\phi_{2on}) \approx v_{C2}(\phi_{1off}) - \left(\frac{C_{OL}}{C_2}\right)V_T\,. \tag{45}$$

After the ϕ_2 switches (M3 and M4) turn on, the voltage across C_2, $v_{C2}(\phi_2)$, will be

$$v_{C2}(\phi_2) \approx \left(\frac{C_1}{C_2}\right)v_{C1}(\phi_{2on}) + v_{C2}(\phi_{2on}) = \left(\frac{C_1}{C_2}\right)v_{C1}(\phi_{1off}) + v_{C2}(\phi_{2on})\ . \tag{46}$$

The final occurrence of feedthrough happens when the ϕ_2 switches (M3 and M4) turn off. When ϕ_2 makes the transition from V_T to 0, feedthrough from C_1 and C_2 will occur.

This is modeled in the third row of Fig. 9.2-10. However, at this point we are only interested in the capacitor, C_2. From the right-hand model in the third row, we can write

$$v_{out} = v_{C2}(\phi_{2off}) \approx v_{C2}(\phi_2) + \left(\frac{C_{OL}}{C_2}\right)V_T \,. \tag{47}$$

Substituting Eq. (46) into Eq. (47) gives

$$v_{out} \approx \left(\frac{C_1}{C_2}\right)v_{C1}(\phi_{1off}) + v_{C2}(\phi_{2on}) + \left(\frac{C_{OL}}{C_2}\right)V_T \,. \tag{48}$$

Substituting Eq. (45) into Eq. (48) gives

$$v_{out} \approx \left(\frac{C_1}{C_2}\right)v_{C1}(\phi_{1off}) + v_{C2}(\phi_{1off}) - \left(\frac{C_{OL}}{C_2}\right)V_T + \left(\frac{C_{OL}}{C_2}\right)V_T \,. \tag{49}$$

Finally, substituting Eqs. (42) and (43) into Eq. (49) gives desired result which is

$$v_{out} \approx \frac{C_1}{C_2}\left(v_{in} - \frac{C_{OL}}{2C_1}v_{in}\right) + \left(\frac{C_{OL}}{C_2}\right)V_T = \left(\frac{C_1}{C_2}\right)v_{in} - \left(\frac{C_{OL}}{2C_2}\right)v_{in} + \left(\frac{C_{OL}}{C_2}\right)V_T \,. \tag{50}$$

Eq. (50) is a general result for switched capacitor circuits. The output voltage will consist of three terms. These terms are the ideal output, an output that is proportional to the input, and an output that is constant. The input independent or constant term can be eliminated using the concept of autozeroing, discussed in Chap. 8. The most annoying term is the one that is proportional to the input because this introduces distortion into the signal being processed by the switched capacitor circuit. We will show in the next section, how to eliminate the input dependent term of Eq. (50) by modifying the clocks slightly. Consequently, circuit techniques can eliminate both undesired terms.

Example 9.2-4

Clock Feedthrough Effects on a Switched Capacitor Voltage Amplifier

For the noninverting, voltage amplifier of Fig. 9.2-9, find the ideal output voltage and the input dependent and independent terms due to feedthrough if C_1 = 10pF, C_2 = 1pF, and C_{OL} = 100fF. Assume that v_{in} = 0.1V and V_T = 1V.

Solution

From Eq. (50) we get

$$v_{out} = 10\, v_{in} - 0.05\, v_{in} - 0.1V = 1V - 0.005V + 0.1V.$$

Therefore, the ideal output is 1V, the input dependent output is -5mV, and the input independent output is 100mV.

The next nonideality of the switched capacitor voltage amplifiers we will examine is that of a finite, differential voltage gain of the op amp, $A_{vd}(0)$. The influence of $A_{vd}(0)$ on the noninverting voltage amplifier of Fig. 9.2-7a can be characterized from the model given in Fig. 9.2-11 for the amplifier during the ϕ_2 phase period. Eqs. (30) and (31) for the ϕ_2 phase period are still valid. Because $A_{vd}(0)$ is not infinite, there is a voltage that

exists in series with the op amp input to model this result. The value of this voltage source is $v_{out}/A_{vd}(0)$ where v_{out} is the output voltage of the op amp. The result, as shown in Fig. 9.2-11 is that a virtual ground no longer exists at the inverting input terminal of the op amp. Therefore, the output voltage during the ϕ_2 phase period can be written as

$$v_{out}^{e}(n\text{-}1/2)T = \left(\frac{C_1}{C_2}\right)v_{in}^{o}(n\text{-}1)T - \left(\frac{C_1+C_2}{C_2}\right)\frac{v_{out}^{e}(n\text{-}1/2)T}{A_{vd}(0)}. \qquad (51)$$

Note that if $A_{vd}(0)$ becomes infinity that Eq. (51) reduces to Eq. (32). Converting Eq. (51) to the z-domain and solving for the $H^{oe}(z)$ transfer function gives

$$H^{oe}(z) = \frac{V_{out}^{e}(z)}{V_{in}^{o}(z)} = \left(\frac{C_1}{C_2}\right)z^{-1/2}\left[\frac{1}{1+\dfrac{C_1+C_2}{A_{vd}(0)C_2}}\right]. \qquad (52)$$

Eq. (52) shows that the influence of a finite value of $A_{vd}(0)$ is on the magnitude response only. The phase response is unaffected by a finite value of $A_{vd}(0)$. For example, if $A_{vd}(0)$ is 1000V/V then for Ex. 9.2-4, the bracket term which is the error term has a value of 0.9891 instead of the ideal value of 1.0. This error is a gain error which can influence the signal processing function of the switched capacitor circuit.

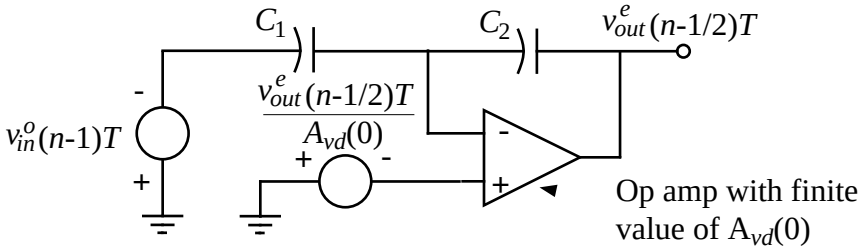


Figure 9.2-11 - Circuit model for the Fig. 9.2-7a during the ϕ_2 phase when the op amp has a finite value of $A_{vd}(0)$.

Lastly, let us consider the influence of a finite value of the unity-gainbandwidth, *GB*, and the slew rate of the op amp. The quantitative analysis of the influence of *GB* on switched capacitor circuits is not simple and is best done using simulation methods. In general, if clock period, *T*, becomes less than $10/GB$, the *GB* will influence the performance. The influence manifests itself in an incomplete transfer of charge causing both magnitude and phase errors. The *GB* of the op amp must be large enough so that the transient response, called the *settling time*, is completed before the circuit is ready for the next phase. For further detail, the reader is referred to reference [7].

In addition to a finite value of *GB*, another nonideality of the op amp that can influence the switched capacitor circuit performance is the *slew rate*. The slew rate is the maximum rate of the rise or fall of the output voltage of the op amp. If the output voltage of the op amp must make large changes, such as when the feedback switch (M5) in Fig. 9.2-9 closes, the slew rate requires a period of time for the output voltage to change. For example, suppose the output voltage of Fig. 9.2-9 is 5V and the slew rate of the op amp is $1V/\mu s$. To change the output by 5V requires $5\mu s$. This means a period of at least $10\mu s$ is required which corresponds to a maximum clock frequency of 100kHz.

9.3 Switched Capacitor Integrators

The switched capacitor integrator is a key building block in analog signal processing circuits. All filter design can be reduced to noninverting and inverting integrators. In this section, we will first examine continuous time integrators to understand the desired performance of switched capacitor integrators. The remainder of the section will discuss switched capacitor integrators and illustrate their frequency response characteristics. The nonideal characteristics of the op amp and switches upon the performance will be presented. Lastly, we will look at damped, switched capacitor integrators or first-order circuits, lowpass circuits.

Continuous Time Integrators

A noninverting and inverting, continuous time integrator using op amps is shown in Fig. 9.3-1. While it is possible to find a noninverting integrator configuration using one op amp, Fig. 9.3-1a is used because it is the simplest form of a noninverting integrator. We will characterize the integrators in this section in the frequency domain although we could equally well use the time domain. The ideal transfer function for the noninverting integrator of Fig. 9.3-1a is

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{1}{j\omega R_1 C_2} = \frac{\omega_I}{j\omega} = \frac{-j\omega_I}{\omega} \tag{1}$$

where ω_I is the called the *integrator frequency*. τ_I is equal to $1/\omega_I$ and is called the *integrator time constant*. ω_I is the frequency where the magnitude of the integrator gain is unity. For the inverting integrator, the ideal transfer function is

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{-1}{j\omega R_1 C_2} = \frac{-\omega_I}{j\omega} = \frac{j\omega_I}{\omega}. \tag{2}$$

Fig. 9.3-2 gives the ideal magnitude and phase response of the noninverting and inverting integrators. The magnitude response is the same but the phase response is different by 180°.

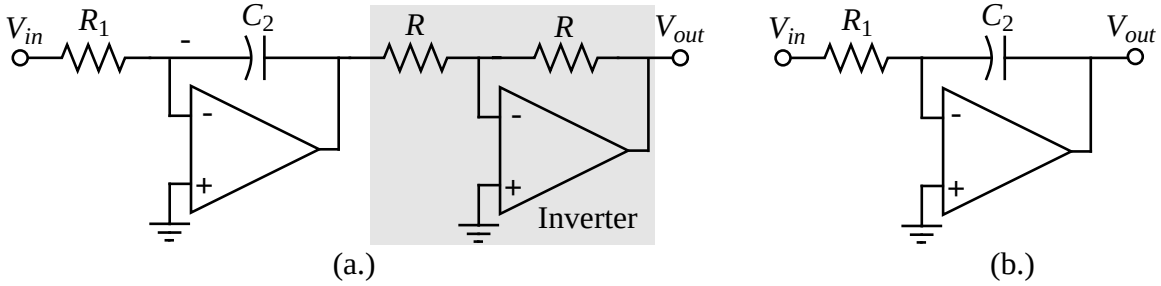


Figure 9.3-1 - (a.) Noninverting and (b.) inverting continuous time integrators.

Let us now investigate the influence of a finite value of the differential voltage gain, $A_{vd}(0)$, and a finite unity-gainbandwidth, *GB*, of the op amp. We will focus only on Fig. 9.3-1b because the switched capacitor realizations will use this structure and not Fig.

9.3-1a. Substituting the resistance, R_2, in Fig. 9.2-2 with a capacitance, C_2 and solving for the closed transfer function gives,

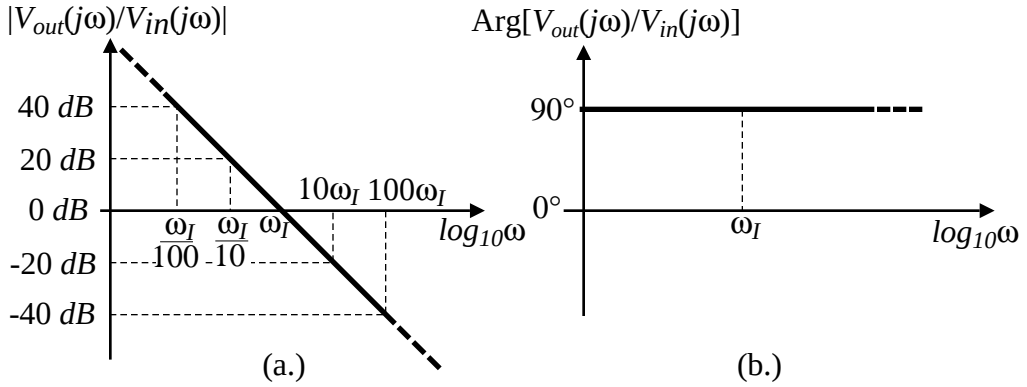


Figure 9.3-2 - (a.) Ideal magnitude and (b.) phase response for an inverting, continuous time integrator.

$$\frac{V_{out}}{V_{in}} = -\left(\frac{1}{sR_1C_2}\right)\frac{\dfrac{A_{vd}(s)\,sR_1C_2}{sR_1C_2+1}}{1+\dfrac{A_{vd}(s)\,sR_1C_2}{sR_1C_2+1}} = \left(-\frac{\omega_I}{s}\right)\frac{\dfrac{A_{vd}(s)\,(s/\omega_I)}{(s/\omega_I)+1}}{1+\dfrac{A_{vd}(s)\,(s/\omega_I)}{(s/\omega_I)+1}} \tag{3}$$

where the loop gain, LG, is given as

$$LG = \frac{A_{vd}(s)\,(s/\omega_I)}{(s/\omega_I)+1}. \tag{4}$$

As we examine the magnitude of the loop gain frequency response, we see that for low frequencies ($s\rightarrow 0$) that LG becomes much less than unity. Also, at high frequencies LG is much less than unity. In the middle frequency range, the magnitude of LG is much greater than unity and Eq. (3) becomes

$$\frac{V_{out}}{V_{in}} = -\frac{\omega_I}{s}. \tag{5}$$

At low frequencies ($s\rightarrow 0$), $A_{vd}(s)$ is approximately $A_{vd}(0)$ and Eq. (3) becomes

$$\frac{V_{out}}{V_{in}} = -A_{vd}(0). \tag{6}$$

At high frequencies ($s\rightarrow\infty$), $A_{vd}(s)$ is approximately GB/s and Eq. (3) becomes

$$\frac{V_{out}}{V_{in}} = -\left(\frac{GB}{s}\right)\left(\frac{\omega_I}{s}\right). \tag{7}$$

Eqs. (5), (6), and (7) represent Eq. (3) for various ranges of frequency. We can identify these ranges by finding the frequency where the magnitude of the loop gain goes to unity. However, it is simpler just to equate the magnitude of Eq. (5) to Eq. (6) and solve for the frequency, ω_{x1}, where they cross. The result is

$$\omega_{x1} = \frac{\omega_I}{A_{vd}(0)}. \tag{8}$$

The transition frequency between Eqs. (5) and (7), ω_{x2}, is similarly found by equating the magnitude of Eq. (5) to the magnitude of Eq. (7) resulting in

$$\omega_{x2} = GB. \tag{9}$$

Fig. 9.3-3 shows the resulting magnitude and phase response of the inverting integrator when $A_{vd}(0)$ and GB are finite.

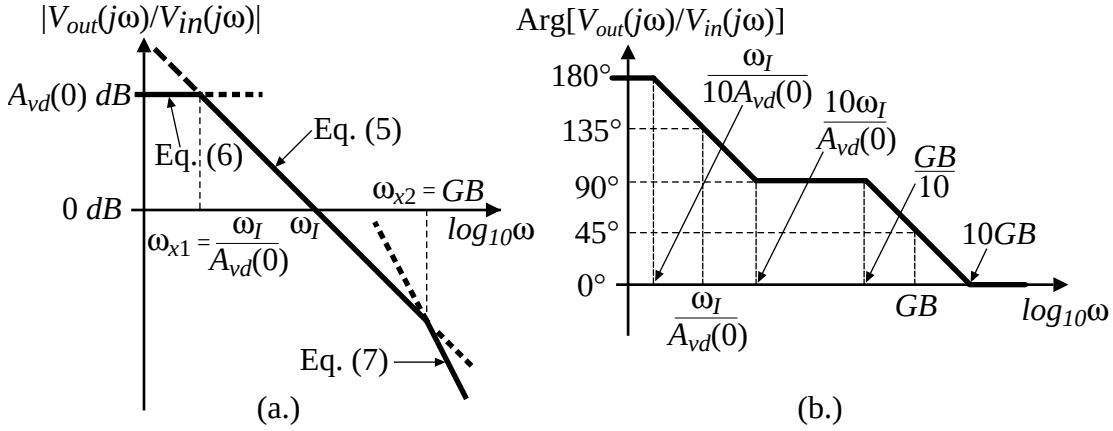


Figure 9.3-3 - (a.) Magnitude and (b.) phase response of a continuous time, inverting integrator when $A_{vd}(0)$ and GB are finite.

Example 9.3-1

Frequency Range over which the Continuous Time Integrator is Ideal

Find the range of frequencies over which the continuous time integrator approximates ideal behavior if $A_{vd}(0)$ and GB of the op amp are 1000 and 1MHz, respectively. Assume that ω_I is 2000π radians/sec.

Solution

The "idealness" of an integrator is determined by how close the phase shift is to ±90° (+90° for an inverting integrator and -90° for a noninverting integrator). The actual phase shift in the asymptotic plot of Fig. 9.3-3b is approximately 6° above 90° at the frequency $10\omega_I/A_{vd}(0)$ and approximately 6° below 90° at GB /10. Let us assume for this example that a ±6° tolerance is satisfactory. The frequency range can be found by evaluating $10\omega_I/A_{vd}(0)$ and $GB/10$. We find this range to be from 10Hz to 100kHz.

Switched Capacitor Integrators

The implementation of switched capacitor integrators is straight-forward based on the previous considerations of this chapter. Let us choose the continuous time, inverting integrator of Fig. 9.3-1b as the prototype. If we replace the resistor, R_1, with the negative

transresistance equivalent circuit of Fig. 9.2-6b we obtain the noninverting, switched capacitor integrator shown in Fig. 9.3-4a. Note that the negative transresistance circuit in effect realizes the inverter of Fig. 9.3-1a. Next, if we replace R_1 by the positive transresistance equivalent circuit of Fig. 9.2-6a we obtain the noninverting, switched capacitor integrator shown in Fig. 9.3-4b. Alternately, we could simply remove the ϕ_1 feedback switch from circuits in Fig. 9.2-7 to obtain the circuits in Fig. 9.3-4.

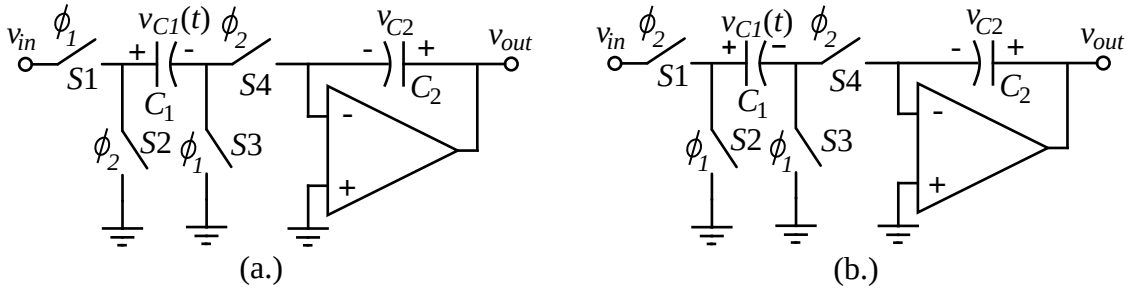


Figure 9.3-4 - (a.) Noninverting and (b.) inverting switched-capacitor integrators that are independent of parasitic capacitors.

Next, we will develop the frequency response for each of the integrators in Fig. 9.3-4. Starting with the noninverting integrator of Fig. 9.3-4a, let us again use the phasing of Fig. 9.1-7b. Beginning with the phase, ϕ_1, during the time from $t = (n\text{-}1)T$ to $t = (n\text{-}1/2)T$, we may write the voltage across each capacitor as

$$v_{c1}^{o}(n\text{-}1)T = v_{in}^{o}(n\text{-}1)T \tag{10}$$

and

$$v_{c2}^{o}(n\text{-}1)T = v_{out}^{o}(n\text{-}1)T\,. \tag{11}$$

During the ϕ_2 phase, the circuit is equivalent to the circuit shown in Fig. 9.3-5. Note that each capacitor has a previous charge that is now represented by voltage sources in series with the capacitances. From Fig. 9.3-5b, we can write

$$v_{out}^{e}(n\text{-}1/2)T = \left(\frac{C_1}{C_2}\right)v_{in}^{o}(n\text{-}1)T + v_{out}^{o}(n\text{-}1)T\,. \tag{12}$$

If we advance one more phase period, i.e. t = (n)T to t = (n-1/2)T, we see that the voltage at the output is unchanged. Thus, we may write

$$v_{out}^{o}(n)T = v_{out}^{e}(n\text{-}1/2)T\,. \tag{13}$$

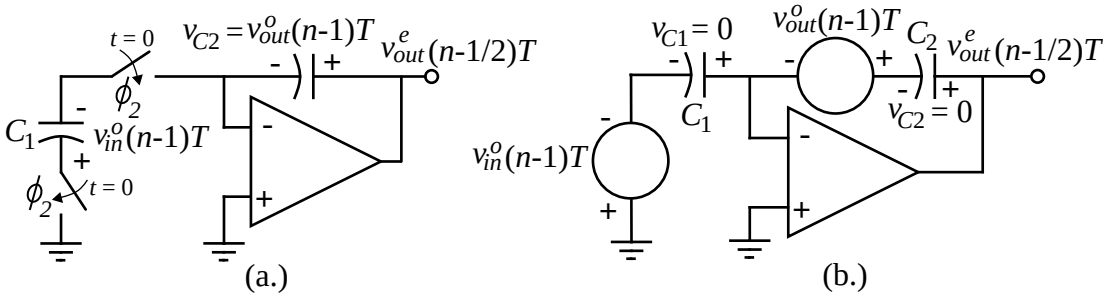


Figure 9.3-5 - (a.) Equivalent circuit of Fig. 9.3-4a at the moment the ϕ_2 switches close. (b.) Simplified equivalent circuit of Fig. 9.3-5a.

Substituting Eq. (12) into Eq. (13) gives the desired time relationship expressed as

$$v_{out}^{o}(n)T = \left(\frac{C_1}{C_2}\right)v_{in}^{o}(n\text{-}1)T + v_{out}^{o}(n\text{-}1)T\,. \tag{14}$$

We can write Eq. (14) in the z-domain as

$$V_{out}^{o}(z) = \left(\frac{C_1}{C_2}\right)z^{-1}V_{in}^{o}(z) + z^{-1}V_{out}^{o}(z)\,. \tag{15}$$

Solving for the transfer function, $H^{oo}(z)$, gives

$$H^{oo}(z) = \frac{V_{out}^{o}(z)}{V_{in}^{o}(z)} = \left(\frac{C_1}{C_2}\right)\frac{z^{-1}}{1\text{-}z^{-1}} = \left(\frac{C_1}{C_2}\right)\frac{1}{z\text{-}1}\,. \tag{16}$$

To get the frequency response, we replace z by $e^{j\omega T}$. The result is,

$$H^{oo}(e^{j\omega T}) = \frac{V_{out}^{o}(e^{j\omega T})}{V_{in}^{o}(e^{j\omega T})} = \left(\frac{C_1}{C_2}\right)\frac{1}{e^{j\omega T}\text{-}1} = \left(\frac{C_1}{C_2}\right)\frac{e^{-j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}\,. \tag{17}$$

Replacing $e^{j\omega T/2} - e^{-j\omega T/2}$ by its equivalent trigonometric identity, Eq. (17) becomes

$$H^{oo}(e^{j\omega T}) = \frac{V_{out}^{o}(e^{j\omega T})}{V_{in}^{o}(e^{j\omega T})} = \left(\frac{C_1}{C_2}\right)\frac{e^{-j\omega T/2}}{j2\,\sin(\omega T/2)}\left(\frac{\omega T}{\omega T}\right) = \left(\frac{C_1}{j\omega TC_2}\right)\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)(e^{-j\omega T/2}). \tag{18}$$

The interpretation of the results of Equation (18) is found by letting ωT becomes small so that the last two terms approach unity. Therefore, we can equate Eq. (18) with Eq. (1). We see that the result is that R_1 is equivalent to T/C_1 which is consistent with the results transresistance of Fig. 9.2-6. The integrator frequency, ω_I, can be expressed as,

$$\omega_I = \frac{C_1}{TC_2}\,. \tag{19}$$

Note that the integrator frequency, ω_I, of the switched capacitor integrator will be well defined because it is proportional to the ratio of capacitors.

The second and third terms in Eq. (18) represent the magnitude error and phase error respectively. As the signal frequency, ω, increases the magnitude term increases from a value of unity and approaches infinity when $\omega = 2\pi/T$. The phase error is zero at low frequencies and subtracts linearly from the ideal phase shift of -90 degrees. The following example illustrates the influence of these errors and the difference between a continuous time and switched capacitor integrator.

Example 9.3-2

Comparison of a Continuous Time and Switched Capacitor Integrator

Assume that ω_I is equal to $0.1\omega_c$ and plot the magnitude and phase response of the noninverting continuous time and switched capacitor integrator from 0 to ω_I.

Solution

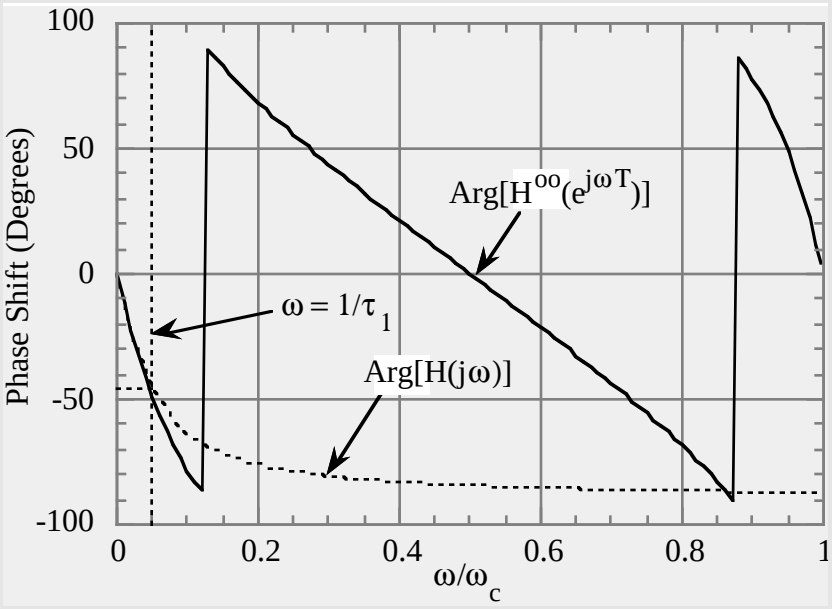
Letting ω_I be $0.1\omega_c$ gives

$$H(j\omega) = \frac{1}{10j\omega/\omega_c}$$

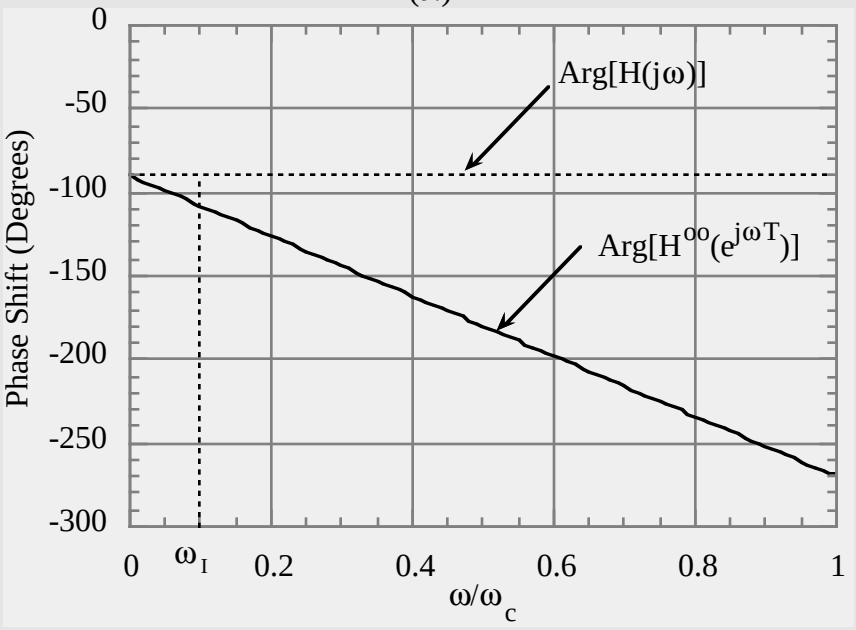
and

$$H^{oo}(e^{j\omega T}) = \left(\frac{1}{10j\omega/\omega_c}\right)\left(\frac{\pi\omega/\omega_c}{sin(\pi\omega/\omega_c)}\right)(e^{-\pi\omega/\omega_c})$$

Figure 9.3-6 shows the results of this example.



(a.)



(b.)

Figure 9.3-6 - (a.) Magnitude and (b.) phase response of a continuous time, $H(j\omega)$, and a switched capacitor, $H^{oo}(e^{j\omega T})$, noninverting integrator.

The inverting, stray-insensitive, switched capacitor integrator is shown in Fig. 9.3-4b. The frequency response for this circuit will be developed in a manner similar to the noninverting integrator illustrated above. If we continue to use the switch phasing of Fig. 9.1-7b, the conditions during the ϕ_1 phase period during the time from $t = (n\text{-}1)T$ to $t = (n\text{-}1/2)T$ can be written as

$$v_{C1}^{o}(n\text{-}1)T = 0 \tag{20}$$

and

$$v_{C2}^{o}(n\text{-}1)T = v_{out}^{o}(n\text{-}1)T = v_{out}^{e}(n\text{-}3/2)T\,. \tag{21}$$

We note from Eq. (21) that the capacitor, C_2, holds the voltage from the previous phase period, ϕ_2, during the present phase period, ϕ_1.

During the next phase period, ϕ_2, which occurs during the time from $t = (n\text{-}1/2)T$ to $t = (n)T$, the inverting integrator of Fig. 9.3-4b can be represented as shown in Fig. 9.3-7a. Using the simplified equivalent circuit of Fig. 9.3-7b, we easily write the output voltage during this phase period as

$$v_{out}^{e}(n\text{-}1/2)T = v_{out}^{e}(n\text{-}3/2)T - \left(\frac{C_1}{C_2}\right)v_{in}^{e}(n\text{-}1/2)T\,. \tag{22}$$

Expressing Eq. (22) in terms of the z-domain equivalent gives

$$V_{out}^{e}(z) = z^{-1}V_{out}^{e}(z) - \left(\frac{C_1}{C_2}\right)V_{in}^{e}(z)\,. \tag{23}$$

Solving for the transfer function, $H^{ee}(z)$, gives

$$H^{ee}(z) = \frac{V_{out}^{e}(z)}{V_{in}^{e}(z)} = -\left(\frac{C_1}{C_2}\right)\frac{1}{1\text{-}z^{-1}} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z\text{-}1}\,. \tag{24}$$

To get the frequency response, we replace z by $e^{j\omega T}$. The result is,

$$H^{ee}(e^{j\omega T}) = \frac{V_{out}^{e}(e^{j\omega T})}{V_{in}^{e}(e^{j\omega T})} = -\left(\frac{C_1}{C_2}\right)\frac{e^{j\omega T}}{e^{j\omega T}\text{-}1} = -\left(\frac{C_1}{C_2}\right)\frac{e^{j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}\,. \tag{25}$$

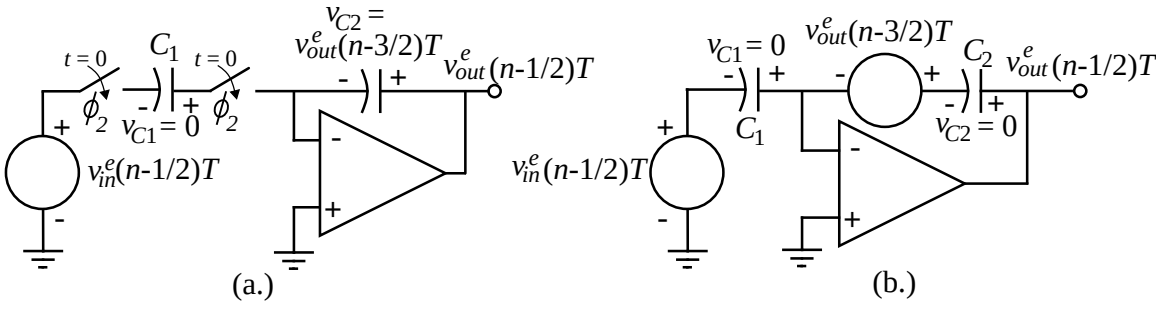


Figure 9.3-7 - (a.) Equivalent circuit of Fig. 9.3-4b at the moment the ϕ_2 switches close. (b.) Simplified equivalent circuit of Fig. 9.3-7a.

Replacing $e^{j\omega T/2} - e^{-j\omega T/2}$ in Eq. (25) by $2j\ sin(\omega T/2)$ and simplifying gives,

$$H^{ee}(e^{j\omega T}) = \frac{V_{out}^{e}(e^{j\omega T})}{V_{in}^{e}(e^{j\omega T})} = -\left(\frac{C_1}{j\omega TC_2}\right)\left(\frac{\omega T/2}{sin(\omega T/2)}\right)(e^{j\omega T/2}) \ . \tag{26}$$

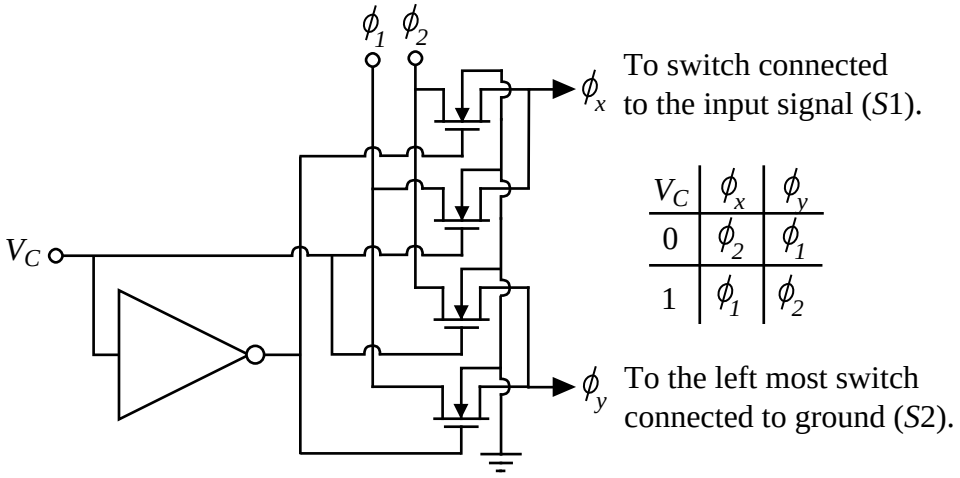
Eq. (26) is nearly identical with Eq. (18) for the noninverting integrator. The only difference is the minus sign multiplying the entire function and in the argument of the exponential term. Consequently, the magnitude response is identical but the phase response is given as

$$\text{Arg}[H^{ee}(e^{j\omega T})] = \frac{\pi}{2} + \frac{\omega T}{2}. \tag{27}$$

We see that the phase error is positive for the case of the inverting integrator. Other transfer functions can be developed for the inverting (and noninverting) integrator depending upon when the output is taken (see Problem 9.3-xx).

In many applications, a noninverting and inverting integrator are in series in a feedback loop. It should be noted using the configurations of Fig. 9.3-4 that *the phase errors of each integrator cancel* resulting in no phase error. Consequently, these integrators would be ideal from a phase response viewpoint.

In addition, we note that the inverting, stray insensitive, switched capacitor integrator of Fig. 9.3-4b differs from the noninverting, stray insensitive, switched capacitor integrator of Fig. 9.3-4a only by the phasing of the two left-most switches. In many applications, the phasing of these switches can be controlled by a circuit such as Fig. 9.3-8 which steers the ϕ_1 and ϕ_2 clocks according to the binary value of the voltage, v_C. ϕ_x is applied to the switch connected to the input ($S1$) and ϕ_y is applied to the leftmost switch connected to ground ($S2$). This circuit is particularly useful in waveform generators [8].



V_C	ϕ_x	ϕ_y
0	ϕ_2	ϕ_1
1	ϕ_1	ϕ_2

Figure 9.3-8 - A circuit that changes the ϕ_1 and ϕ_2 clocks of the leftmost switches of Fig. 9.3-4.

Nonideal Characteristics of Switched Capacitor Integrators

The nonideal behavior of switched capacitor integrators includes clock feedthrough, finite differential voltage gain of the op amp, finite unity gainbandwidth of the op amp, and the slew rate of the op amp. We will briefly consider the effects of each of these characteristics.

The influence of the clock feedthrough has been illustrated for when switched capacitor amplifiers were discussed. Recall that the offset appeared at the output in two forms. One that was independent of the input signal and one that was dependent on the input signal. The signal dependent input offset can be removed by delaying the ϕ_1 clock and the ϕ_2 clock applied to leftmost switches of Fig. 9.3-4. Fig. 9.3-9 illustrates how the clocks are delayed. Consider the results of applying the clocks of Fig. 9.3-9 to the noninverting integrator of Fig. 9.3-4a. As $S3$ opens when ϕ_1 falls, clock feedthrough occurs but since the switch terminals are at ground potential, this feedthrough is independent of the signal level. After a clock delay, $S1$ opens because the clock ϕ_{1d} falls. However, no feedthrough can occur because $S3$ is open and there is no current path. Similarily, as $S4$ opens because the clock ϕ_{2d} falls, no input dependent feedthrough can occur because the switch terminals are at ground potential. Finally, as $S2$ opens because the clock ϕ_{2d} falls, there can be no feedthrough because $S4$ is open and there is no current path. The delayed clock for switches $S1$ and $S2$ result in the removal of input dependent feedthrough.

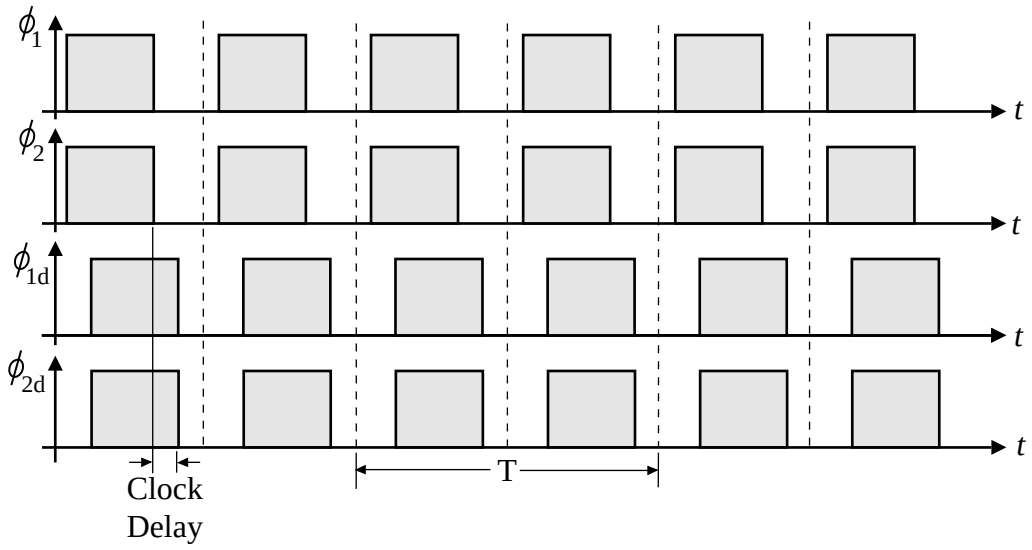


Figure 9.3-9 - Delayed clock scheme to remove input dependent offset voltage.

The influence of a finite value of $A_{vd}(0)$ can be developed by using the model for the op amp shown in Fig. 9.2-11 for one of the switched capacitor integrators of Fig. 9.3-4. Consider the circuit in Fig. 9.3-10 which is an equivalent for the noninverting integrator at the beginning of the ϕ_2 phase period. Compared with Fig. 9.3-5b, we note two important changes. First, is the presence of an independent source, v_{out}^{e} $(n\text{-}1/2)T/A_{vd}(0)$, that models the finite value of $A_{vd}(0)$ and the second is that the independent source in

series with C_2 has been increased by the amount of $v_{out}^{o}(n\text{-}1)T/A_{vd}(0)$. The time domain expression for $v_{out}^{e}(n\text{-}1/2)T$ can be written as

$$v_{out}^{e}(n\text{-}1/2)T = \left(\frac{C_1}{C_2}\right)v_{in}^{o}(n\text{-}1)T + v_{out}^{o}(n\text{-}1)T + \frac{v_{out}^{o}(n\text{-}1)T}{A_{vd}(0)} - \frac{v_{out}^{e}(n\text{-}1/2)T}{A_{vd}(0)}\left(\frac{C_1+C_2}{C_2}\right). \quad (28)$$

Substituting Eq. (13) into Eq. (28) gives

$$v_{out}^{o}(n)T = \left(\frac{C_1}{C_2}\right)v_{in}^{o}(n\text{-}1)T + v_{out}^{o}(n\text{-}1)T + \frac{v_{out}^{o}(n\text{-}1)T}{A_{vd}(0)} - \frac{v_{out}^{o}(n)T}{A_{vd}(0)}\left(\frac{C_1+C_2}{C_2}\right) \quad (29)$$

Using the previous procedures to solve for the z-domain transfer function results in,

$$H^{oo}(z) = \frac{V_{out}^{o}(z)}{V_{in}^{o}(z)} = \frac{\frac{C_1}{C_2}z^{-1}}{1 - z^{-1} - \frac{z^{-1}}{A_{vd}(0)} + \frac{C_1}{A_{vd}(0)C_2} + \frac{1}{A_{vd}(0)}}. \quad (30)$$

Eq. (30) can be rewritten as

$$H^{oo}(z) = \frac{V_{out}^{o}(z)}{V_{in}^{o}(z)} = \left(\frac{(C_1/C_2)\,z^{-1}}{1 - z^{-1}}\right)\left(\frac{1}{1 + \frac{1}{A_{vd}(0)} + \frac{C_1}{A_{vd}(0)C_2(1\text{-}z^{-1})}}\right) \quad (31)$$

or

$$H^{oo}(z) = \frac{V_{out}^{o}(z)}{V_{in}^{o}(z)} = \frac{H_I(z)}{1 + \frac{1}{A_{vd}(0)} + \frac{C_1}{A_{vd}(0)C_2(1\text{-}z^{-1})}} \quad (32)$$

where $H_I(z)$ is given by Eq. (16). The similar development for the inverting integrator of Fig. 9.3-4b results in Eq. (32) if $H_I(z)$ is given by Eq. (24).

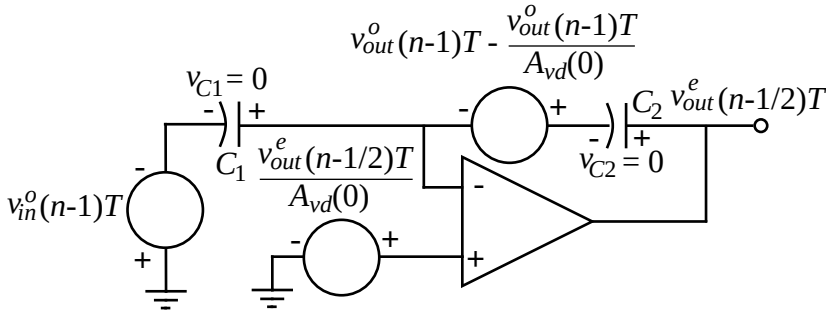


Figure 9.3-10 - Equivalent circuit for the noninverting integrator at the beginning of the ϕ_2 phase period.

The denominator of Eq. (32) represents the error due to a finite value of $A_{vd}(0)$. If we substitute in Eq. (32) for the z-domain variable, z, by $e^{j\omega T}$, we can get the following expression

$$H^{oo}(e^{j\omega T}) = \frac{H_I(e^{j\omega T})}{1 + \frac{1}{A_{vd}(0)}\left[1 + \frac{C_1}{2C_2}\right] - j\frac{C_1/C_2}{2A_{vd}(0)\ tan\left(\frac{\omega T}{2}\right)}} \tag{33}$$

where now $H_I(e^{j\omega T})$ is given by Eq. (18) for the noninverting integrator and Eq. (26) for the inverting integrator. The error of an integrator can be expressed by the following [7]

$$H(j\omega) = \frac{H_I(j\omega)}{[1-m(\omega)]\ e^{-j\theta(\omega)}} \tag{34}$$

where $m(\omega)$ is the magnitude error and $\theta(\omega)$ is the phase error and $H_I(j\omega)$ is the ideal integrator transfer function. Note that in the case of switched capacitor circuits, $H_I(j\omega)$, includes a magnitude and phase error due to sampling. If $\theta(\omega)$ is much less than unity, Eq. (34) can be approximated by

$$H(j\omega) \approx \frac{H_I(j\omega)}{1 - m(\omega) - j\theta(\omega)}. \tag{35}$$

Comparing Eq. (33) with Eq. (35) gives the magnitude and phase error due to a finite value of $A_{vd}(0)$ as

$$m(j\omega) = -\frac{1}{A_{vd}(0)}\left[1 + \frac{C_1}{2C_2}\right] \tag{36}$$

and

$$\theta(j\omega) = \frac{C_1/C_2}{2A_{vd}(0)\ tan\left(\frac{\omega T}{2}\right)}. \tag{37}$$

Eqs. (36) and (37) characterize the magnitude and phase error due to a finite value of $A_{vd}(0)$ for the switched capacitor integrators of Fig. 9.3-4.

Example 9.3-3

Evaluation of the Integrator Errors due to a finite value of $A_{vd}(0)$

Assume that the clock frequency and integrator frequency of a switch capacitor integrator is 100kHz and 10kHz, respectively. If the value of $A_{vd}(0)$ is 100, find the value of $m(j\omega)$ and $\theta(j\omega)$ at 10kHz.

Solution

The ratio of C_1 to C_2 is found from Eq. (19) as

$$\frac{C_1}{C_2} = \omega_I T = \frac{2\pi \cdot 10{,}000}{100{,}000} = 0.6283\ .$$

Substituting this value along with that for $A_{vd}(0)$ into Eq. (36) and Eq. (37) gives

$$m(j\omega) = -\left[1 + \frac{0.6283}{2}\right] = -1.0131$$

and

$$\theta(j\omega) = \frac{0.6283}{2 \cdot 100 \cdot \tan(18°)} = 0.554° \ .$$

The interpretation of these results are best seen in Eq. (34). The "ideal" switched capacitor transfer function, $H_I(j\omega)$, will be multiplied by a value of approximately 1/1.0131 = 0.987 and will have an additional phase lag of approximately 0.554°. In general, the phase shift error is more serious than the magnitude error.

Finally, let us examine the influence of a finite value of the unity-gainbandwidth, *GB*. The calculations necessary to develop the results require a time domain model for the op amp that incorporates the frequency effects of *GB*. The model and calculations are beyond the scope of this presentation but can be found in the appendix of [7]. The results are summarized in Table 9.3-1. If ωT is much less than unity, the expressions in Table 9.3-1 reduce to

$$m(\omega) \approx -2\pi \left(\frac{f}{f_c}\right) e^{-\pi(GB/f_c)} \tag{38}$$

for both the noninverting and inverting integrators. For the noninverting integrator, $\theta(j\omega)$ is still approximately zero but for the inverting integrator, $\theta(\omega) \approx m(\omega)$. These results should allow one to estimate the influence of a finite value of *GB* on the performance of the switched capacitor integrators of Fig. 9.3-4.

Table 9.3-1

Summary of the Influence of a Finite Value of *GB* on Switched Capacitor Integrators.

Noninverting Integrator	Inverting Integrator
$m(\omega) \approx -e^{-k_1}\left(\frac{C_2}{C_1+C_2}\right)$	$m(\omega) \approx -e^{-k_1}\left[1 - \left(\frac{C_2}{C_1+C_2}\right)\cos(\omega T)\right]$
$\theta(\omega) \approx 0$	$\theta(\omega) \approx -e^{-k_1}\left(\frac{C_2}{C_1+C_2}\right)\cos(\omega T)$
$k_1 \approx \pi\left(\frac{C_2}{C_1+C_2}\right)\left(\frac{GB}{f_c}\right)$	

The remaining nonideal characteristic of the op amp to consider is the slew rate of the op amp. The integrators are fortunate in being less sensitive to slew rate limits than the amplifiers of the last section. This is because the feedback capacitor, C_2, holds the output voltage of the op amp constant when no capacitors are being connected to the

inverting input of the op amp. Slew rate limitations occur only when the output of the op amp is changing due to a change of charge on C_2. During this time, slew rate limitation may occur. To avoid this limitation, it necessary that the following inequality be satisfied

$$\frac{\Delta V_o(max)}{SR} < \frac{T}{2} \tag{39}$$

where $\Delta v_o(max)$ is the maximum output swing of the integrator. For example, if $\Delta v_o(max)$ is 5V and the clock frequency is 100kHz, the slew rate of the op amp must be greater than 1V/μs. To allow for the other nonidealities of the op amp, a slew rate of 10V/μs would be preferable in this case.

The noise of switched capacitor circuits includes normal sources plus a noise source that is a thermal equivalent noise source of the switches. This noise voltage spectral density is called kT/C noise and has units of volts^2/Hz. Assume that the switched capacitor or Fig. 9.3-11a can be represented by the continuous time circuit of Fig. 9.3-11b. Next, we find the rms noise voltage of Fig. 9.3-11b and assume that it approximates that of Fig. 9.3-11a.

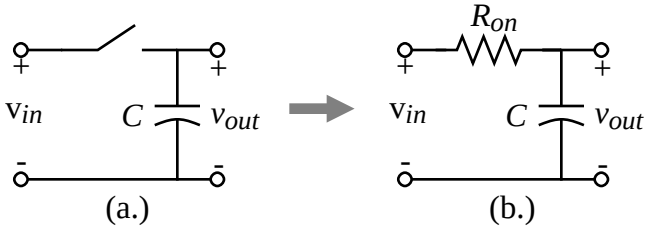


Figure 9.3-11 - (a.) Simple switched capacitor circuit. (b.) Approximation of (a.).

The noise voltage spectral density of Fig. 9.3-11b is given as

$$\overline{e_{R_{on}}^2} = 4kTR_{on} \text{ Volts}^2/\text{Hz} = \frac{2kTR_{on}}{\pi} \text{ Volt}^2/\text{Rad./sec.} \tag{40}$$

The rms noise voltage is found by integrating this spectral density from 0 to ∞. This is given as

$$v_{R_{on}}^2 = \frac{2kTR_{on}}{\pi} \int_0^\infty \frac{\omega_1^2 d\omega}{\omega_1^2+\omega^2} = \frac{2kTR_{on}}{\pi}\left(\frac{\pi\omega_1}{2}\right) = \frac{kT}{C} \text{ Volts(rms)}^2 \tag{41}$$

where $\omega_1 = 1/(R_{on}C)$. Note that the switch has an effective noise bandwidth of

$$f_{sw} = \frac{1}{4R_{on}C} \text{ Hz} \tag{42}$$

which is found by dividing Eq. (41) by Eq. (40).

Other nonidealities that we have not examined include noise coupled directly or capacitively from the power, clock and ground lines and from the substrate into the circuit. In addition, the noise of the MOSFETs must be considered.

9.4 - z-domain Models of Two-Phase, Switched Capacitor Circuits

Although the switched capacitor circuits considered so far can be analyzed with reasonable effort, more complex switched capacitor circuits will become a challenge. To provide a way to meet this challenge and to confirm the hand analysis results, we examine z-domain models of switched capacitor circuits in this section. These models will allow us to both analyze more complex switched capacitor circuits and to perform frequency domain simulation using SPICE-type simulators. Other specialized simulation programs are available that simulate the frequency response of switched capacitor circuits [9,10,11].

The development of z-domain models for switched capacitor circuits using a two-phase, nonoverlapping clock is based on decomposing time-varient circuits into time-invarient circuits. This can be done by considering a generic switched capacitor circuit such as that shown in Fig. 9.4-1. Here we see a two-port characterization of a switched capacitor circuit. It consists of an independent voltage source, a switched capacitor, an unswitched capacitor, and an op amp or dependent voltage source. There are actually four different versions of the unswitched capacitor that we will consider. They are the parallel or toggle switched capacitor of Fig. 9.1-1, the positive and negative switched capacitors of Fig. 9.2-6, and a capacitor in series with a switch which we have not used yet. The z-domain models for each of these two-ports and their respective versions are presented below followed with examples. It is important to note that all switched and unswitched capacitor two-port networks are connected between a voltage source and the virtual ground of an op amp.

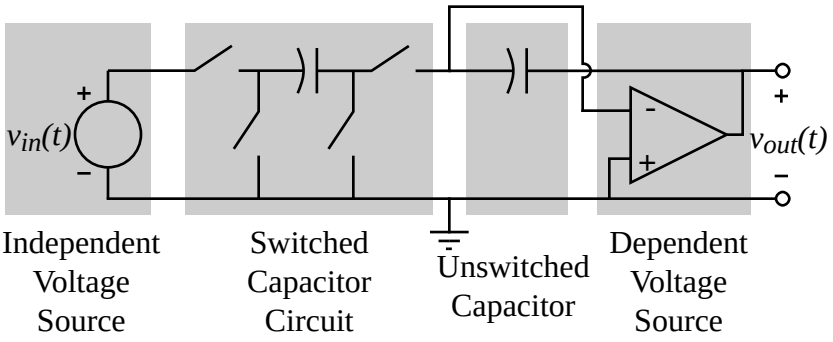


Figure 9.4-1 - Two-port characterization of a general switched capacitor circuit.

Independent Voltage Sources

A possible waveform of an independent voltage source in a two-phase switched capacitor circuit was shown in Fig. 9.1-5. A z-domain, phase-dependent model of this voltage source is shown in Fig. 9.4-2a along with the values of voltages during each phase. The values of $V^e(z)$ and $V^o(z)$ are shown in Fig. 9.1-5. The values of this independent source depends on the phase of the clock. A z-domain, phase-independent model of this voltage source for the odd and even phases are shown in Fig. 9.4-2b and 9.4-2c, respectively along with their waveforms. Note that the phase-independent voltage sources change value every clock period, T, so that $V^e(z) = z^{-1/2}V^o(z)$ and $V^o(z) = z^{-1/2}V^e(z)$ for Figs. 9.4-2b and 9.4-2c, respectively.

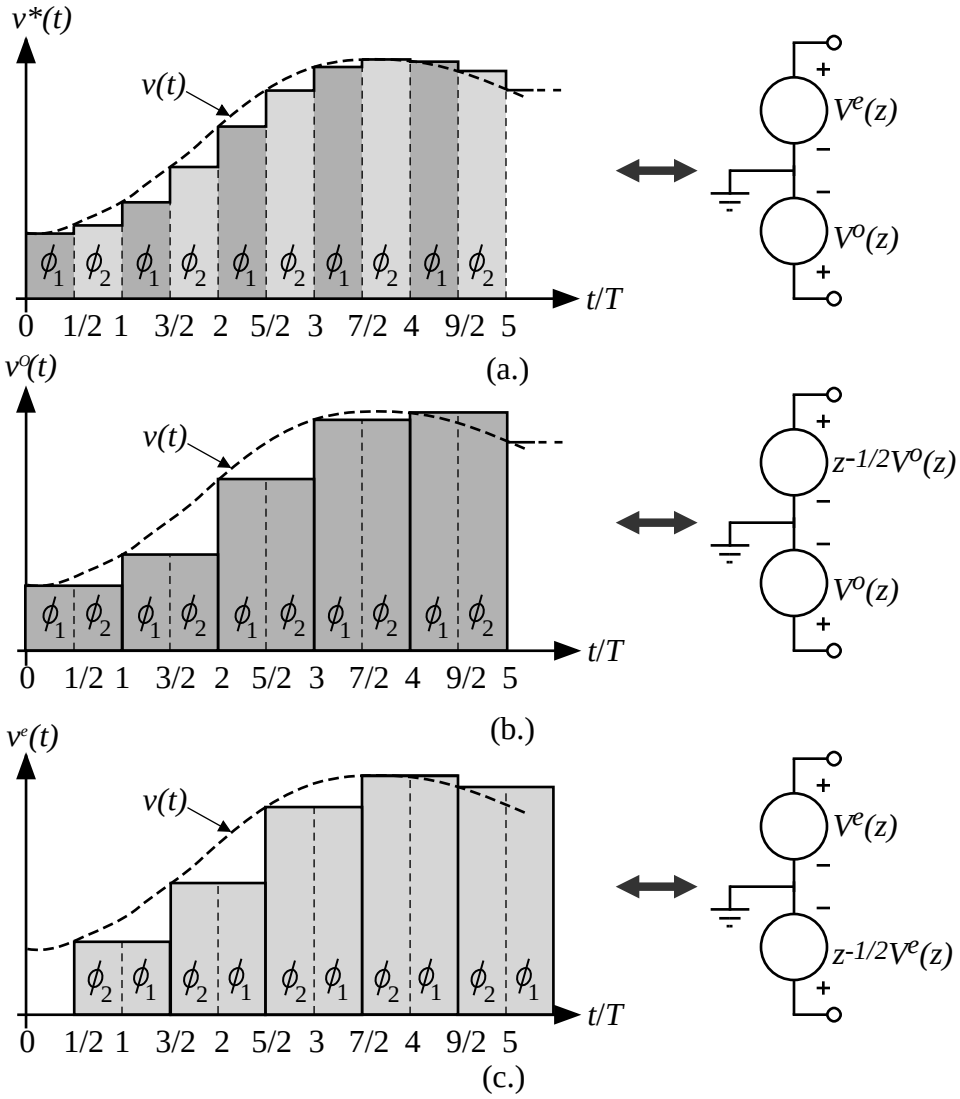


Figure 9.4-2 - z-domain equivalent circuits for a independent voltage source. (a.) A phase dependent source. (b.) A phase independent voltage source for the odd phase. (c.) A phase independent voltage source for the even phase.

Switched Capacitor Two-Port Circuits

Let us now consider the z-domain equivalent circuits for four different types of switched capacitor two-port circuits. The z-domain models will contain three types of admittances. We remember that the voltage across the admittance is the stimulus and the current through the admittance is the response. The first type of admittance is expressed as

$$I(z) = Y \cdot z^{0} V(z) = Y \cdot V(z) \tag{1}$$

which is interpreted as a current $I(z)$ of value $YV(z)$ occurs with no delay when a voltage $V(z)$ is applied. The second type of admittance is given as

$$I(z) = Y \cdot z^{-1/2} V(z) \tag{2}$$

which is interpreted as a current $I(z)$ of value $YV(z)$ occuring a half-period after the voltage $V(z)$ is applied. Finally, the third type of admittance is

$$I(z) = (1\text{-}z^{-1})Y \cdot V(z) \qquad (3)$$

which is interpreted as a current which first appears as a value of $YV(z)$ and at a period later this current is zero. The admittance factor, Y, is equal to the value of the capacitor, C, that is being switched in all three cases.

The four switched capacitor two-port circuits are shown in Fig. 9.4-3 in the first column. The second column gives a four-port, z-domain equivalent model. The third column shows the reduced equivalent circuit when the switched capacitor circuit is imbedded between a voltage source and the virtual ground of an op amp. The synthesis of these circuits is more complex that we wish to consider here. More detail on the model development can be found elsewhere [12].

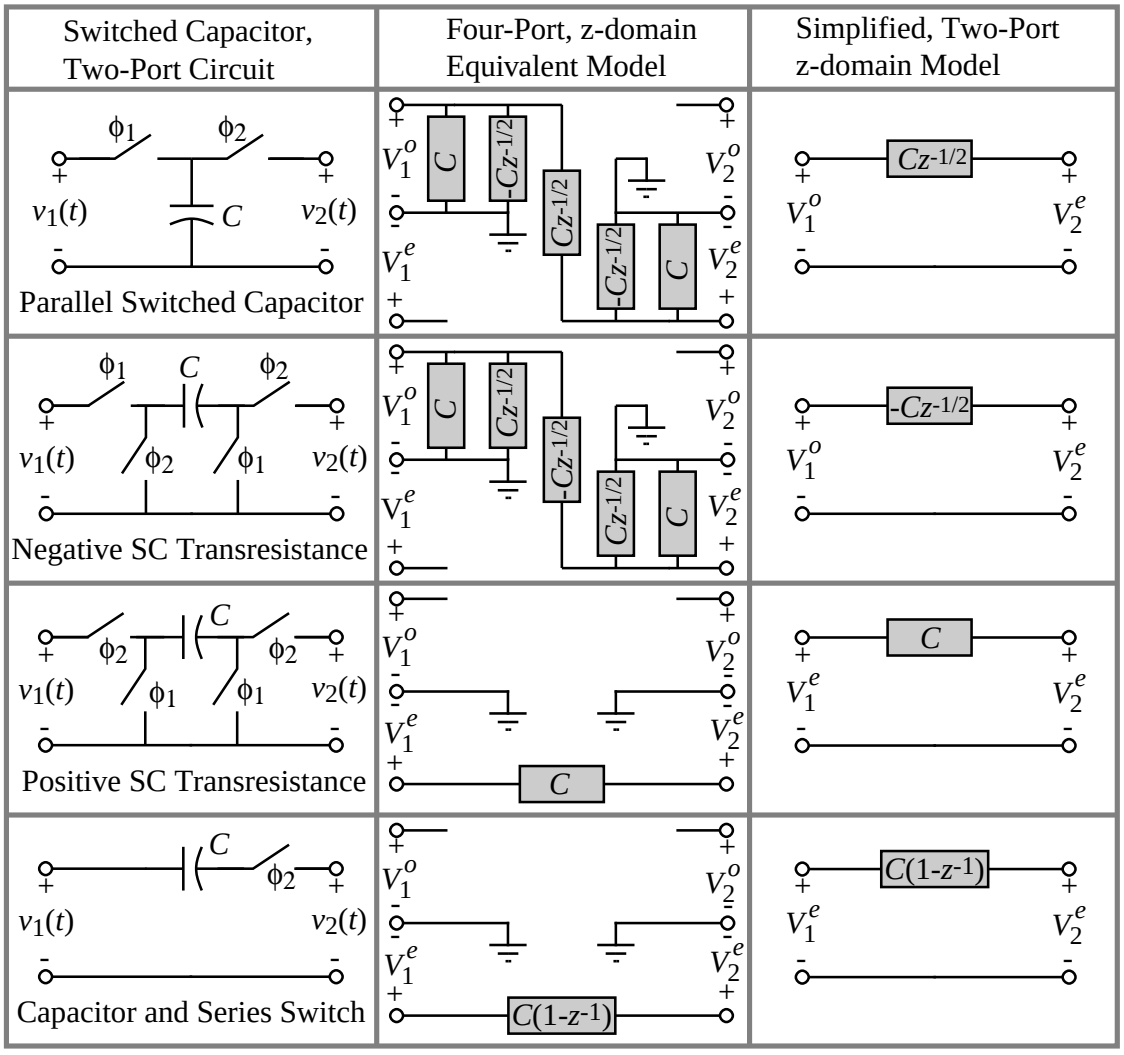


Figure9.4-3 - z-domain models for some of the more widely used switched capacitor circuits.

Unswitched Capacitors and Op Amps

In addition to switched capacitors of Fig 9.4-3, there two other configurations of importance. One is the unswitched capacitance shown in the first row of Fig. 9.4-4 and the other is a capacitor and shunt switch shown in the bottom row of Fig. 9.4-4. Neither of the z-domain models for these circuits can be reduced to a two-port model. The derivation of these models is given in [12].

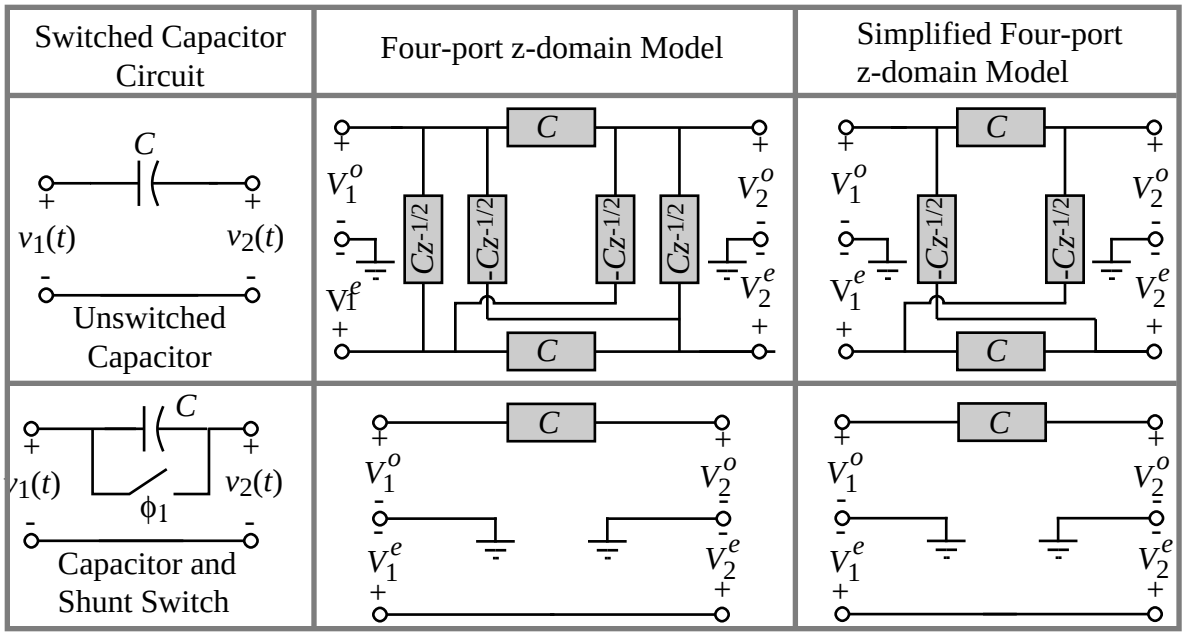


Figure 9.4-4 - z-domain models for switched capacitor circuits that cannot be reduced to two-port models.

Finally, Fig. 9.4-5 shows the z-domain model of an op amp having a low-frequency gain of A_v. Figs. 9.4-3 through 9.4-5 constitute a sufficient set of models for the switched capacitor circuits that are normally encountered.

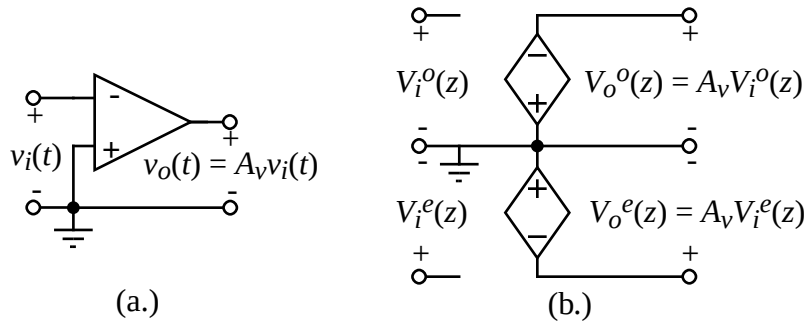


Figure 9.4-5 - (a.) Time domain op amp model. (b.) z-domain op amp model.

Example 9.4-1

Illustration of the Validity of the z-domain Models of Fig. 9.4-3

Show that the z-domain four-port model for the negative switched capacitor transresistance circuit of Fig. 9.4-3 is equivalent to the two-port switched capacitor circuit.

Solution

For the two-port switched capacitor circuit, we observe that during the ϕ_1 phase, the capacitor C is charged to $v_1(t)$. Let us assume that the time reference for this phase is t - T/2 so that the capacitor voltage is

$$v_C = v_1(t - T/2).$$

During the next phase, ϕ_2, the capacitor is inverted and v_2 can be expressed as

$$v_2(t) = -v_C = -v_1(t - T/2).$$

Next, let us sum the currents flowing away from the positive V_2^e node of the four-port z-domain model in Fig. 9.4-3. This equation is,

$$-Cz^{-1/2}(V_2^e - V_1^o) + Cz^{-1/2}V_2^e + CV_2^e = 0.$$

This equation can be simplified as

$$V_2^e = -z^{-1/2}V_1^o$$

which when translated to the time domain gives

$$v_2(t) = -v_C = -v_1(t - T/2).$$

Thus, we have shown that the four-port z-domain model is equivalent to the time domain circuit for the above consideration.

z-domain Analysis of Switched Capacitor Circuits

Many of the switched capacitor circuits that we shall use have the same form so that the z-domain analysis is very useful for analyzing switched capacitor circuits. In the most general case, the circuit is time varying so that it is necessary to take the two-port switched capacitor circuit such as that in Fig. 9.4-1 and expand it to a four-port switched capacitor. This is illustrated in Fig. 9.4-6. In Fig. 9.4-6b, we have chosen the upper terminals as the odd terminals (ϕ_1 phase) and the lower terminals as the even terminals (ϕ_2 phase).

Fig. 9.4-6b corresponds to circuits which are time-variant. These types of circuits process and transfer charge during both phases of the clock. The four-port z-domain models of the middle column of Fig. 9.4-3 are used in Fig. 9.4-6b. However, if the switched capacitor circuit only processes and transfers charge during one phase of the clock and is not used during the other phase, then it can be treated as a time-invarient circuit. This allows the four-port model to be reduced to the two-port model of Fig. 9.4-7. Most of the cases considered in this study will be time-invarient which permits

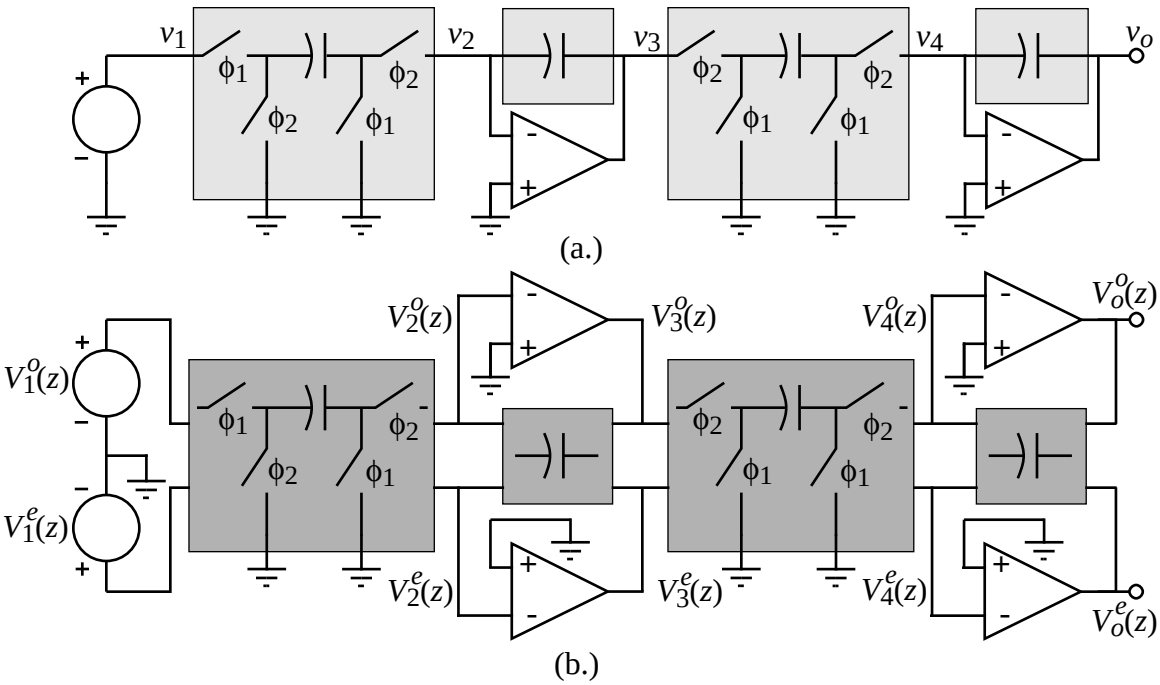


Figure 9.4-6 - (a.) General, two-port (lightly shaded blocks), switched capacitor circuit. (b.) Four-port (darker shaded blocks) z-domain model of (a.)

appreciable simplification in the z-domain model (i.e. the two-port models in the right-hand column of Fig. 9.4-3).

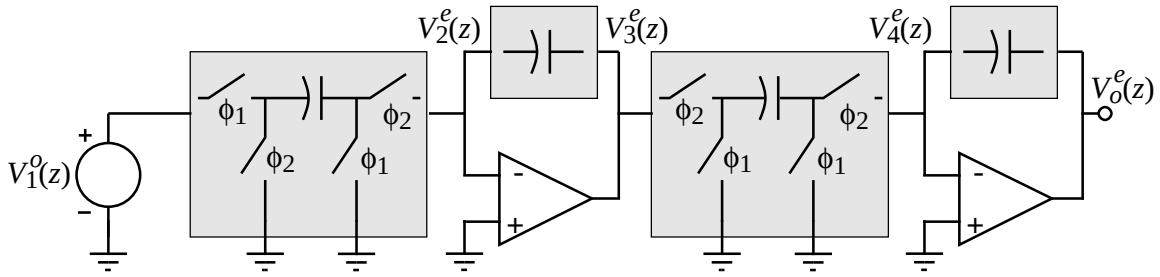


Figure 9.4-7 - Simplification of Fig. 9.4-6b to a two-port z-domain model if the switched capacitor circuits are time-invarient.

Let us now apply the above z-domain modeling in several examples of switched capacitor circuits that will serve to illustrate the approach to apply these models.

Example 9.4-2

z-domain Analysis of the Noninverting Switched Capacitor Integrator of Fig. 9.3-4a

Find the z-domain transfer function $V_o^e(z)/V_i^o(z)$ and $V_o^o(z)/V_i^o(z)$ of Fig. 9.3-4a using the above methods.

Solution

First redraw Fig. 9.3-4a as shown in Fig. 9.4-8a. We have added an additional ϕ_2 switch to help in using Fig. 9.4-3. Because this circuit is time-invarient, we may use the two-port modeling approach of Fig. 9.4-7. We have grouped the switched capacitors as indicated by the shaded boxes in Fig. 9.4-8a. Note that C_2 and the indicated ϕ_2 switch are modeled by the bottom row, right column of Fig 9.4-3. The fact that the point between C_2 and the ϕ_2 switch is at virtual ground has no influence on the modeling. The resulting z-domain model for Fig. 9.4-8a is shown in Fig. 9.4-8b. In Fig. 9.4-8b we have also shown how to calculate the transfer function for the odd phase by using a voltage-controlled voltage source with a half-period delay.

Recalling that the z-domain models are of admittance form, it is easy to write

$$-C_1 z^{-1/2} V_i^o(z) + C_2(1-z^{-1}) V_o^e(z) = 0$$

which can be rearanged to give

$$H^{oe}(z) = \frac{V_o^e(z)}{V_i^o(z)} = \frac{C_1 z^{-1/2}}{C_2(1-z^{-1})} \ .$$

$H^{oo}(z)$ is found by using the relationship that $V_o^o(z) = z^{-1/2} V_o^e(z)$ to get

$$H^{oo}(z) = \frac{V_o^o(z)}{V_i^o(z)} = \frac{C_1 z^{-1}}{C_2(1-z^{-1})}$$

which is equal to Eq. (16) of Sec. 9.3.

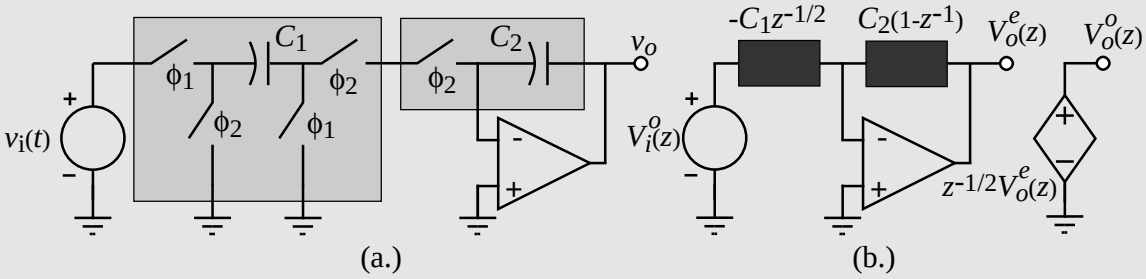


Figure 9.4-8 - (a.) Modified equivalent circuit of Fig. 9.3-4a. (b.) Two-port, z-domain model for Fig. 9.4-8a.

Example 9.4-3

z-domain Analysis of the Inverting Switched Capacitor Integrator of Fig. 9.3-4b.

Find the z-domain transfer function $V_o^e(z)/V_i^e(z)$ and $V_o^o(z)/V_i^e(z)$of Fig. 9.3-4a using the above methods.

Solution

Fig. 9.4-9a shows the modified equivalent circuit of Fig. 9.3-4b. The two-port, z-domain model for Fig. 9.4-9a is shown in Fig. 9.4-9b. Suming the currents flowing to the inverting node of the op amp gives

$$C_1 V_i^e(z) + C_2(1-z^{-1})V_o^e(z) = 0$$

which can be rearanged to give

$$H^{ee}(z) = \frac{V_o^e(z)}{V_i^e(z)} = \frac{-C_1}{C_2(1-z^{-1})} .$$

which is equal to Eq. (24) of Sec. 9.3.

$H^{eo}(z)$ is found by using the relationship that $V_o^o(z) = z^{-1/2}V_o^e(z)$ to get

$$H^{eo}(z) = \frac{V_o^o(z)}{V_i^e(z)} = \frac{C_1 z^{-1/2}}{C_2(1-z^{-1})} .$$

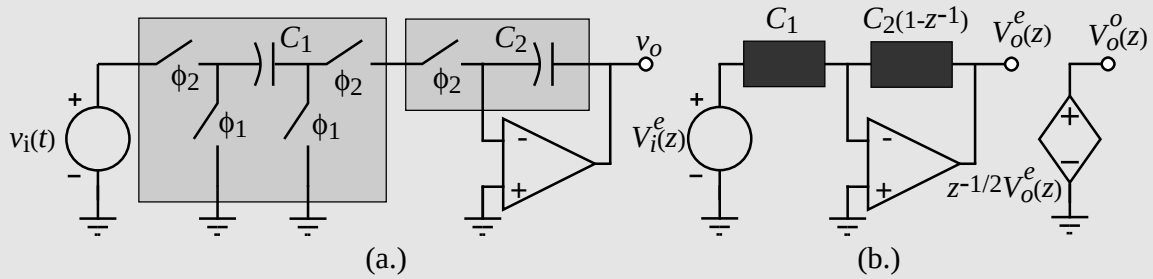


Figure 9.4-9 - (a.) Modified equivalent circuit of Fig. 9.3-4b. (b.) Two-port, z-domain model for Fig. 9.4-9a.

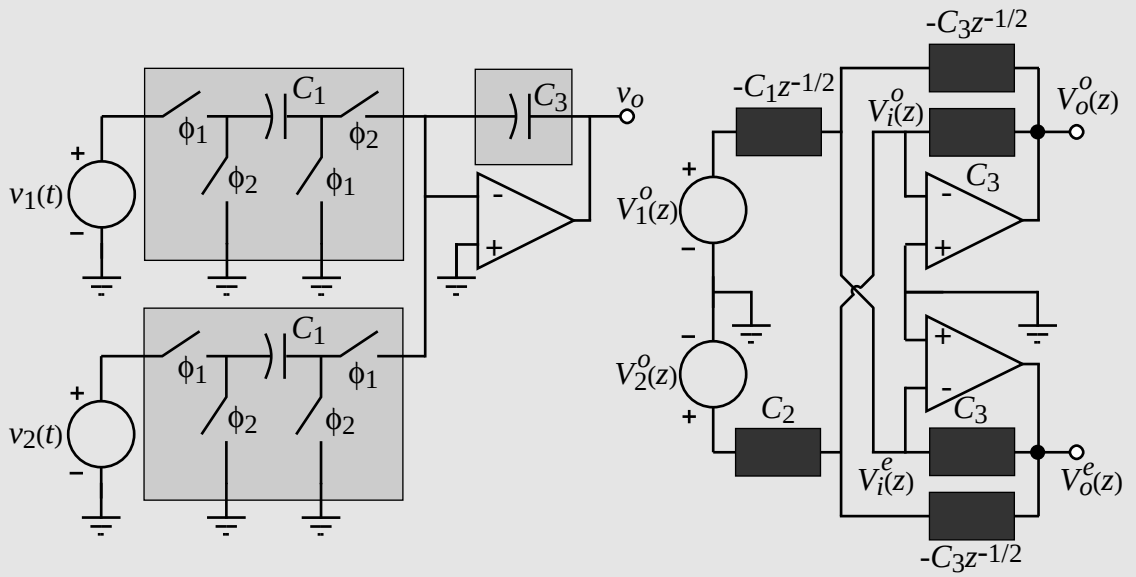
Example 9.4-4

z-domain Analysis a Time-Varient Switched Capacitor Circuit

Find $V_o^o(z)$ and $V_o^e(z)$ as function of $V_1^o(z)$ and $V_2^o(z)$ for the summing, switched capacitor integrator of Fig. 9.4-10a.

Solution

It is important to note that the circuit is time varient. This can be seen in that C_3 is charged from a different circuit for each phase. Therefore, we cannot use the model for C_3 from the bottom row of Fig. 9.4-3. Rather we must use the model in the top row of Fig. 9.4-4. The resulting z-domain model for Fig. 9.4-10a is shown in Fig. 9.4-10b.



(a.) (b.)

Figure 9.4-10 - (a.) Summing, switched capacitor integrator. (b.) Four-port, z-domain model for Fig. 9.4-10a.

Summing the currents flowing away from the $V_i^o(z)$ node gives

$$C_2V_2^e(z) + C_3V_o^o(z) - C_3z^{-1/2}V_o^e(z) = 0 \tag{4}$$

Summing the currents flowing away from the $V_i^e(z)$ nodes gives

$$-C_1z^{-1/2}V_1^o(z) - C_3z^{-1/2}V_o^e(z) + C_3V_o^e(z) = 0 \tag{5}$$

Multiplying Eq. (5) by $z^{-1/2}$ and adding it to Eq. (4) gives

$$C_2V_2^o(z) + C_3V_o^o(z) - C_1z^{-1}V_1^o(z) - C_3z^{-1}V_o^o(z) = 0 \tag{6}$$

Solving for $V_o^o(z)$ gives,

$$V_o^o(z) = \frac{C_1z^{-1}V_1^o(z)}{C_3(1-z^{-1})} - \frac{C_2V_2^o(z)}{C_3(1-z^{-1})} \tag{7}$$

Multiplying Eq. (4) by $z^{-1/2}$ and adding it to Eq. (5) gives

$$C_2z^{-1/2}V_2^o(z) - C_1z^{-1}V_1^o(z) - C_3z^{-1}V_o^e(z) + C_3V_o^e(z) = 0 \tag{8}$$

Solving for $V_o^e(z)$ gives,

$$V_o^e(z) = \frac{C_1z^{-1/2}V_1^o(z)}{C_3(1-z^{-1})} - \frac{C_2z^{-1/2}V_2^o(z)}{C_3(1-z^{-1})} \ . \tag{9}$$

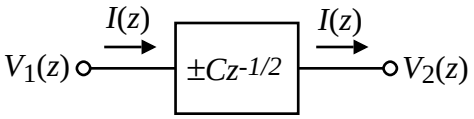
Frequency Domain Simulation of Switched Capacitor Circuits using SPICE

The z-domain analysis methods illustrated above can be used to achieve frequency domain simulation of switched capacitor circuits using SPICE. We note that the z-domain models of switched capacitor circuits consist of positive conductances and positive and negative delayed conductances and dependent and independent voltage sources. All but the delayed conductances can easily be modeled in SPICE. The delayed conductances can be modeled as *storistors* [13]. A storistor is a two-terminal element and is shown in Fig. 9.4-11. Fig. 9.4-11a shows the storistor in the z-domain. It can be written as

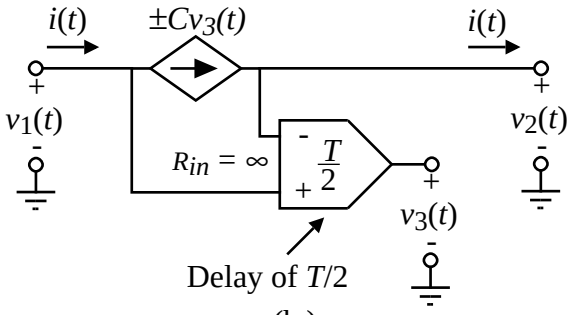
$$I(z) = \pm Cz^{-1/2}\,[V_1(z) - V_2(z)] \tag{10}$$

Figure 9.4-11b shows a time-domain version of the storistor. The symbol that contains T/2 is a delay of T/2 seconds. It can be written as

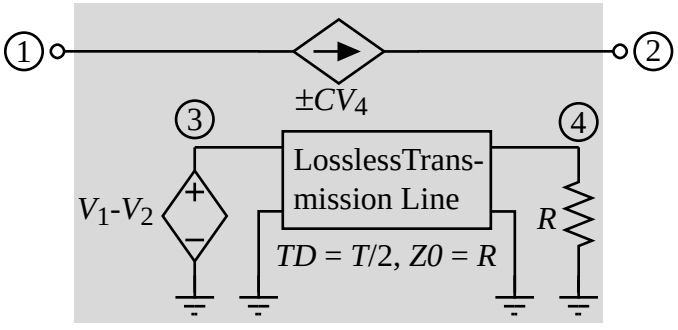
$$i(t) = \pm C\left[v_1\left(t - \frac{T}{2}\right) - v_2\left(t - \frac{T}{2}\right)\right] \tag{11}$$



(a.)



(b.)



(c.)

Figure 9.4-11 - (a.) z-domain model for a storistor. (b.) Time-domain model of a storistor. (c.) Storistor model using SPICE primitives.

Figure 9.4-11c shows the time-domain version of the storistor in SPICE primitives which includes a lossless transmission line. Thus, the voltages applied across the $\pm Cv_4(t)$ controlled source are applied to the input of a lossless transmission line of characteristic impedance Z_o, with a delay of $T/2$ terminated in a resistance equal to Z_o. At $T/2$ seconds after the application of the voltages across the $\pm Cv_4(t)$ controlled source, a current of $\pm$C times the difference between these voltages results. The storistor can easily be made a subcircuit to make its use in simulation as simple as possible. We will illustrate these concepts with an example.

Example 9.4-5

SPICE Simulation of Example 9.4-2

Use SPICE to obtain a frequency domain simulation of the noninverting, switched capacitor integrator in Fig. 9.3-4a. Assume that the clock frequency is 100kHz and design the ratio of C_1 and C_2 to give an integration frequency of 10kHz.

Solution

Eq. (19) of Sec. 9.3 allows the design of C_1/C_2. From this equation we get

$$\frac{C_1}{C_2} = \omega_I T = \frac{2\pi f_I}{f_c} = 0.6283$$

Let us assume that C_2 = 1F which makes C_1 = 0.6283F. Next we replace the switched capacitor C_1 and the unswitched capacitor of Fig. 9.3-4a by the z-domain model of the second row of Fig. 9.4-3 and the first row of Fig. 9.4-4 to obtain Fig. 9.4-12. Note that in addition we used Fig. 9.4-5 for the op amp and assumed that the op amp had a differential voltage gain of 10^6.

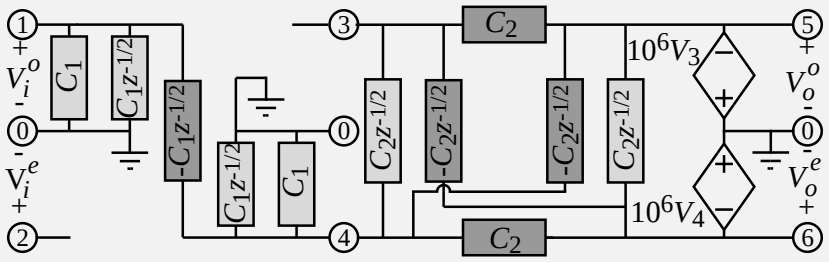


Figure 9.4-12 - z-domain model for noninverting switched capacitor integrator of Fig. 9.3-4a.

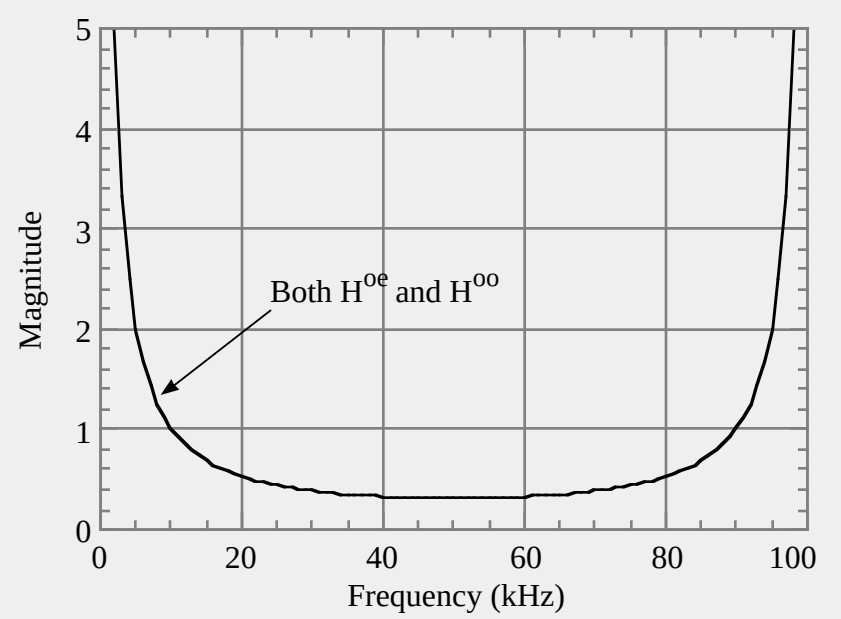
If the differential voltage gain of the op amp approaches infinity, we can simplify Fig. 9.4-12 to that includes only the darker components. This is because nodes 3 and 4 become virtual grounds.

The SPICE input file to perform a frequency domain simulation of Fig. 9.3-4a is shown below.

```
VIN 1 0 DC 0 AC 1
R10C1 1 0 1.592
X10PC1 1 0 10 DELAY
G10 1 0 10 0 1
```

```
X14NC1 1 4 14 DELAY
G14 4 1 14 0 1
R40C1 4 0 1.592
X40PC1 4 0 40 DELAY
G40 4 0 40 0 1
X43PC2 4 3 43 DELAY
G43 4 3 43 0 1
R35 3 5 1.0
X56PC2 5 6 56 DELAY
G56 5 6 56 0 1
R46 4 6 1.0
X36NC2 3 6 36 DELAY
G36 6 3 36 0 1
X45NC2 4 5 45 DELAY
G45 5 4 45 0 1
EODD 6 0 4 0 1E6
EVEN 5 0 3 0 1E6
**********
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5U
RDO 3 0 1K
.ENDS DELAY
**********
.AC LIN 99 1K 99K
.PRINT AC V(6) VP(6) V(5) VP(5)
.PROBE
.END
```

This SPICE input file uses a subcircuit based on the storistor model in Fig. 9.4-11c using the same node numbering here as in that model. The results of this simulation are shown in Fig. 9.4-13. They should be compared with Fig. 9.3-6. It is interesting



Figur 9.4-13(a.) - SPICE magnitude simulation results for Fig. 9.3-4(a.).

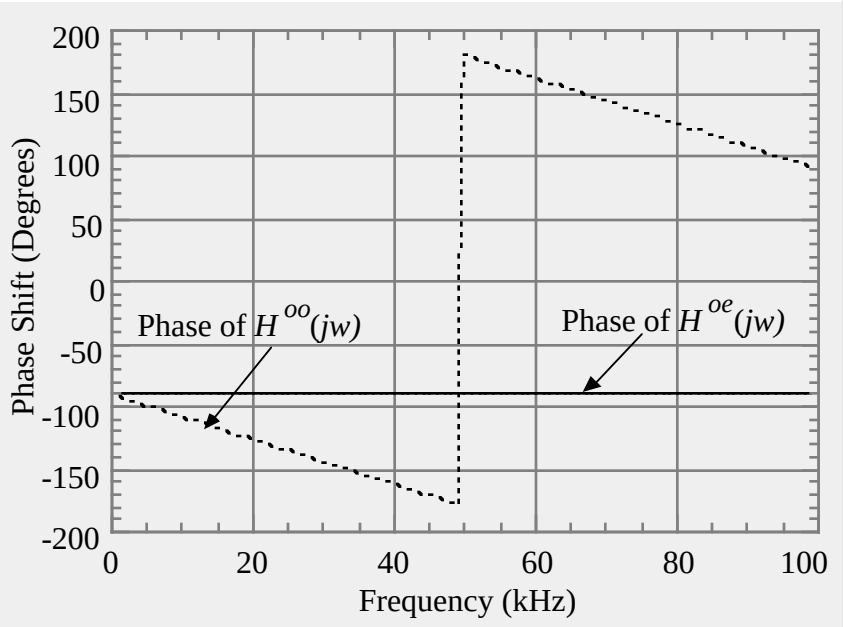


Figure 9.4-13 (b.) - SPICE phase shift simulation results for Fig. 9.3-4a

to note that the $H^{oe}(j\omega)$ phase shift is constant at -90° which is consistent with the previous z-domain analysis.

The above simulation approach can be used examine most of the switched capacitor circuits that will be discussed in this chapter. One should note that the approach cannot be extended to switched capacitor circuits containing resistors because both the switched and unswitched capacitors use conductances (reciprocal resistors) in the model. If the op amp is assumed to be ideal, then z-domain models can be simplified. The advantage of the above approach is that the gain of the op amp could be lowered to simulate its influence on the switched capacitor circuit.

Unfortunately, computer simulation cannot use the z-domain models using unit delays. This prevents the four-port models used above for computer simulation from being simplified to the simpler form of the models used for hand calculations

Methods of analyzing switched capacitor circuits in the z-domain have been illustrated in this section. This method extended naturally to permitting the simulation of switched capacitor circuits in the frequency domain using SPICE. Most of the switched capacitor circuits that we will develop can be reduced to blocks consisting of multiple-input integrators. Consequently, the above analysis methods are applicable to most of the circuits we will study in the remainder of this chapter.

9.5 - First-Order Switched Capacitor Circuits

There are two approaches to switched capacitor filter design. One uses integrators coupled together and the other uses cascades of first-order and second-order switched capacitor building blocks. This section will introduce some of the more well known first-building blocks.

First-Order Switched Capacitor Circuits

A general first-order transfer function in the s-domain is given as

$$H(s) = \frac{sa_1 \pm a_0}{s + b_0} \tag{1}$$

We see that a first-order transfer function has one pole and one zero. If $a_1 = 0$, then the transfer function is lowpass. If $a_0 = 0$, the transfer function is highpass. If neither a_1 or a_0 are zero, the transfer function is all pass. Note that the zero can be in the RHP or LHP of the complex frequency domain.

The equivalent expression of (1) in the z-domain is given as

$$H(z) = \frac{zA_1 \pm A_0}{z + B_0} = \frac{A_1 \pm A_0 z^{-1}}{1 - B_0 z^{-1}} \tag{2}$$

Low Pass Circuit

Figure 9.5-1a shows a switched capacitor low pass circuit. We note that this circuit is identical to Fig. 9.3-4a except a switched capacitor, $\alpha_2 C$, has been placed in parallel with the integrating capacitor, C. An easy way to understand and analyze this and similar circuits is to disconnect the $\alpha_2 C$ switched capacitor from the output and redraw it as shown in Fig. 9.5-1b. This circuit is simply a summing integrator and we can use previous methods to analyze it. The switches in the shaded boxes can be combined into a single pair of switches in the actual realization to minimize the number of switches.

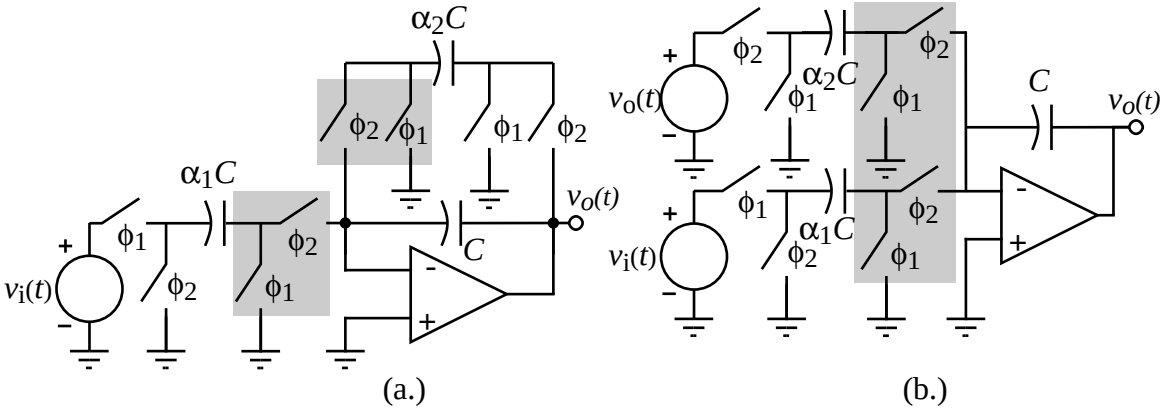


Figure 9.5-1 - (a.) Noninverting, first-order low pass circuit. (b.) Equivalent circuit of Fig. 9.5-1a.

From the results of the last section, it is easy to construct a z-domain model of Fig. 9.5-1b. This model is shown in Fig. 9.5-2. Summing currents flowing toward the inverting op amp terminal gives

$$\alpha_2 C_1 V_o^e(z) - \alpha_1 C_1 z^{-1/2} V_i^o(z) + C_1(1-z^{-1}) V_o^e(z) = 0 \tag{3}$$

Solving for $V_o^o(z)/V_i^o(z)$ gives

$$\frac{V_o^o(z)}{V_i^o(z)} = \frac{\alpha_1 z^{-1}}{1 + \alpha_2 - z^{-1}} = \frac{\dfrac{\alpha_1 z^{-1}}{1+\alpha_2}}{1 - \dfrac{z^{-1}}{1+\alpha_2}} \tag{4}$$

Equating Eq. (4) to Eq. (2) gives the design equations for Fig. 9.5-2 as

$$\alpha_1 = \frac{A_0}{B_0} \qquad \text{and} \qquad \alpha_2 = \left(\frac{1-B_0}{B_0}\right) \tag{5}$$

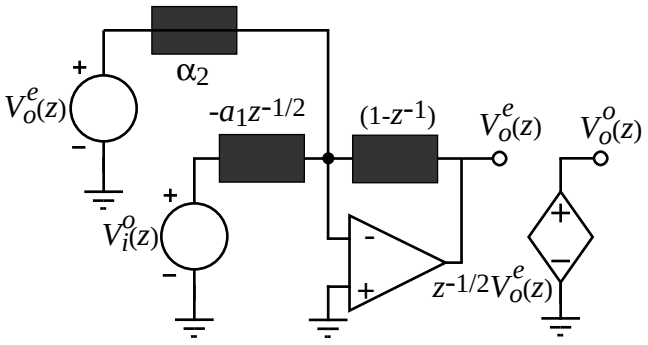


Figure 9.5-2 - z-domain model of Fig. 9.5-1b.

An inverting low pass circuit can be obtained by reversing the phases of the leftmost two switches in Fig. 9.5-1a. It is easy to show that (see Problem 9.5-1)

$$\frac{V_o^e(z)}{V_i^e(z)} = \frac{-\alpha_1}{1 + \alpha_2 - z^{-1}} = \frac{\dfrac{-\alpha_1}{1+\alpha_2}}{1 - \dfrac{z^{-1}}{1+\alpha_2}} \tag{6}$$

Equating Eq. (6) to Eq. (1) gives the design equations for the inverting low pass circuit as

$$\alpha_1 = \frac{-A_1}{B_0} \qquad \text{and} \qquad \alpha_2 = \left(\frac{1-B_0}{B_0}\right) \tag{7}$$

Example 9.5-1

Design of a Switched Capacitor First-Order Circuit

Design a switched capacitor first-order circuit that has a low frequency gain of +10 and a -3dB frequency of 1kHz. Give the value of the capacitor ratios α_1 and α_2. Use a clock frequency of 100kHz.

Solution

This design is complicated in that the specifications are in the s-domain. One way to approach this problem is to assume that the clock frequency, f_c, is much larger than the -3dB frequency. In this example, the clock frequency is 100 times

larger so this assumption should be valid. Based on this assumption, we approximate z^{-1} as

$$z^{-1} = e^{-sT} \approx 1 - sT + \cdots \tag{8}$$

Let us rewrite Eq. (4) as

$$\frac{V_o^o(z)}{V_i^o(z)} = \frac{\alpha_1 z^{-1}}{\alpha_2 + 1 - z^{-1}} \tag{9}$$

Next, we note from Eq. (8) that $1-z^{-1} \approx sT$. Furthermore, if $sT<<1$, then $z^{-1} \approx 1$. Note that $sT<<1$ is equivalent to $\omega << f_c$ which is valid. Making these substitutions in Eq. (9), we get

$$\frac{V_o^o(z)}{V_i^o(z)} \approx \frac{\alpha_1}{\alpha_2 + sT} = \frac{\alpha_1/\alpha_2}{1 + s(T/\alpha_2)} \tag{10}$$

Equating Eq. (10) to the specifications gives

$$\alpha_1 = 10\alpha_2 \qquad \text{and} \qquad \alpha_2 = \frac{\omega_{-3dB}}{f_c} \tag{11}$$

Therefore, we see that $\alpha_2 = 6283/100{,}000 = 0.0628$ and $\alpha_1 = 0.6283$.

High Pass Circuit

A high pass, first-order switched capacitor circuit is shown in Fig. 9.5-3a. The equivalent circuit in the s-domain is a capacitor from the input to the inverting op amp terminal and a parallel resistor and capacitor connected from the output back to the inverting op amp terminal. The switched capacitor, $\alpha_2 C$, implements the resistor in this realization. Fig. 9.5-3b gives a more useful realization that only allows the charge to change on α_1ˆC during the ϕ_2 phase.

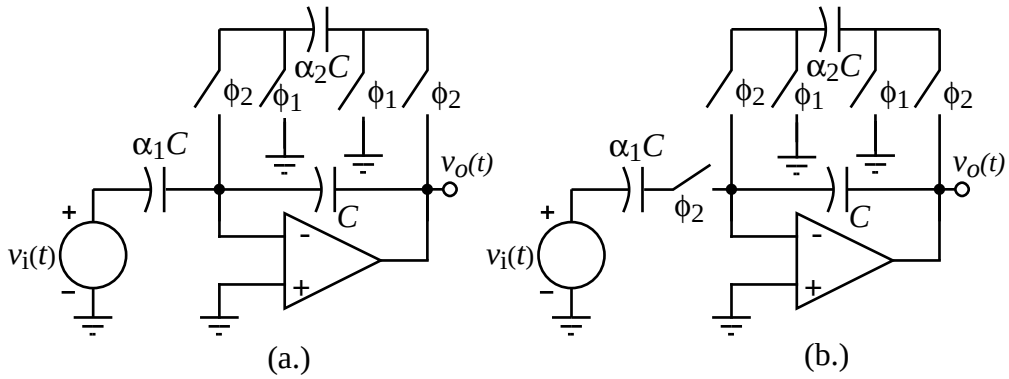


Figure 9.5-3 - (a.) Switched-capacitor, high pass circuit. (b.) Version of Fig. 9.5-3a that constrains the charging of C_1 to the ϕ_2 phase.

The z-domain model for Fig. 9.5-3 is shown in Fig. 9.5-4. We have not bothered to disconnect $\alpha_2 C$ from the output because the circuit is straight-forward to analyze. Summing currents at the inverting input node of the op amp gives

$$\alpha_1(1\text{-}z^{-1})V_i^e(z) + \alpha_2 V_o^e(z) + (1\text{-}z^{-1})V_o^e(z) = 0 \tag{12}$$

Solving for the $H^{ee}(z)$ transfer function gives

$$H^{ee}(z) = \frac{V_o^e(z)}{V_i^e(z)} = \frac{\text{-}\alpha_1(1\text{-}z^{-1})}{\alpha_2\text{+}1\text{-}z^{-1}} = \frac{\dfrac{\alpha_1}{\alpha_2+1}(1\text{-}z^{-1})}{1 - \dfrac{1}{\alpha_2+1}z^{-1}} \tag{13}$$

Equating Eq. (13) to Eq. (1) gives

$$\alpha_1 = \frac{\text{-}A_1}{B_0} \qquad \text{and} \qquad \alpha_2 = 1 - \frac{1}{B_0} \tag{14}$$

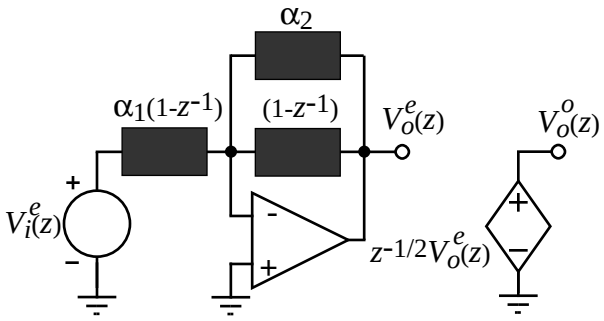


Figure 9.5-4 - z-domain model for Fig. 9.5-3.

Allpass Circuit

Lastly, we consider a first-order realization that can boost either the high or low frequency range. This circuit can also realize an allpass circuit where the magnitude is constant as a function of frequency. Fig. 9.5-5 shows this circuit and its modification in Fig. 9.5-5b that permits easier z-domain modeling.

The z-domain model for Fig. 9.5-5b is shown in Fig. 9.5-6. Summing the currents flowing into the inverting input of the op amp gives

$$\text{-}\alpha_1 z^{-1/2} V_i^o(z) + \alpha_3(1\text{-}z^{-1})V_i^e(z) + \alpha_2 V_o^e(z) + (1\text{-}z^{-1})V_o^e(z) = 0 \tag{15}$$

Since $V_i^o(z) = z^{-1/2}V_i^e(z)$, Eq. (15) can be written as,

$$V_o^e(z)\,[\,\alpha_2\text{+}1\text{-}z^{-1}] = \alpha_1 z^{-1} V_i^e(z) - \alpha_3(1\text{-}z^{-1})V_i^e(z) \tag{16}$$

Solving for $H^{ee}(z)$ gives

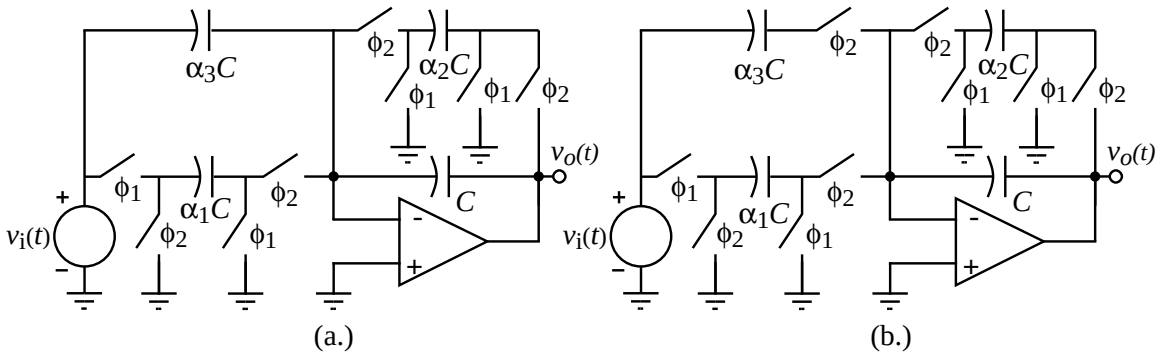


Figure 9.5-5 - (a.) High or low frequency boost circuit. (b.) Modification of (a.) to simplify the z-domain modeling

$$H^{ee}(z) = \frac{\alpha_1 z^{-1} - \alpha_3(1-z^{-1})}{\alpha_2 + (1-z^{-1})} = \left(\frac{-\alpha_3}{\alpha_2+1}\right)\frac{1 - \dfrac{\alpha_1+\alpha_3}{\alpha_3}z^{-1}}{1 - \dfrac{z^{-1}}{\alpha_2+1}} \qquad (17)$$

Equating Eq. (16) to Eq. (1) gives

$$\alpha_1 = \frac{A_1+A_0}{B_0}, \qquad \alpha_2 = 1 - \frac{1}{B_0} \qquad \text{and} \qquad \alpha_3 = \frac{-A_0}{B_0} \qquad (18)$$

The following example demonstrates the use of Fig. 9.5-5 to design a bass boost circuit.

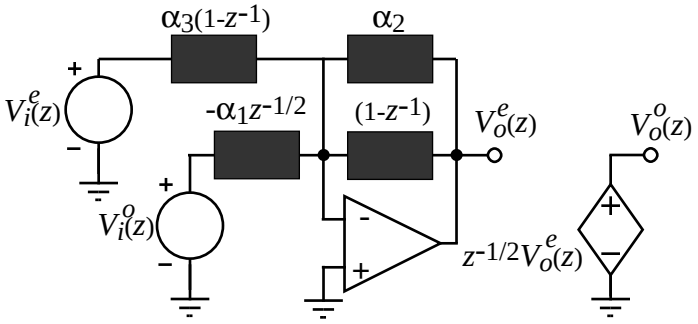


Figure 9.5-6 - z-domain model for Fig. 9.5-5b.

Example 9.5-2

Design of a Switched Capacitor Bass Boost Circuit

Find the values of the capacitor ratios α_1, α_2, and α_3 using a 100kHz clock for Fig. 9.5-5 that will realize the asymptotic frequency response shown in Fig. 9.5-7.

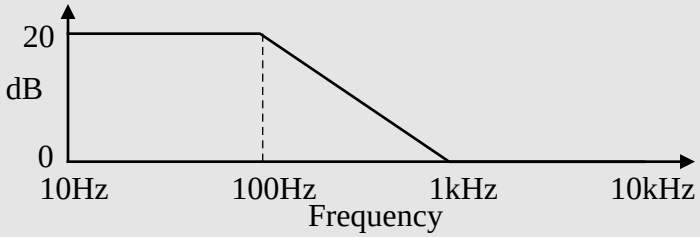


Figure 9.5-7 - Bass boost response for Ex. 9.5-2.

Solution

Since the specification for the example is given in the continuous time frequency domain, let us use the approximation that $z^{-1} \approx 1$ and $1\text{-}z^{-1} \approx sT$, where T is the period of the clock frequency. Therefore, Eq. (16) can be written as

$$H^{ee}(s) \approx \frac{-sT\alpha_3 + \alpha_1}{sT + \alpha_2} = -\frac{\alpha_1}{\alpha_2}\left(\frac{sT\alpha_3/\alpha_1 - 1}{sT/\alpha_2 + 1}\right) \tag{19}$$

From Fig. 9.5-7, we see that the desired response has a dc gain of 10, a right-half plane zero at 2π kHz and a pole at -200π Hz. Thus, we see that the following relationships must hold.

$$\frac{\alpha_1}{\alpha_2} = 10\,, \quad \frac{\alpha_1}{T\alpha_3} = 2000\pi\,, \quad \text{and} \quad \frac{\alpha_2}{T} = 200\pi \tag{20}$$

From the relationships in Eq. (20) we get the desired values as

$$\alpha_1 = \frac{2000\pi}{f_c}\,, \quad \alpha_2 = \frac{200\pi}{f_c}\,, \quad \text{and} \quad \alpha_3 = 1 \tag{20}$$

The circuit of Fig. 9.5-5 becomes an all pass if the magnitude of the pole and zero of Eq. (17) are equal. In this case, α_3/α_1 should equal $1/\alpha_2$. An all pass circuit is useful for contributing a phase shift without influencing the magnitude response of a system.

The three first-order circuits of Fig. 9.5-1, 9.5-3 and 9.5-5 are representative of most siwtched capacitor, first-order circuits. In practice, differential versions of these circuits are used to reduce clock feedthrough, common mode noise sources and enhance the signal swing. Fig. 9.5-8 shows one possible differential version of Fig. 9.5-1, 9.5-3, and 9.5-5. Differential operation of switched capacitor circuits requires op amps or OTAs with differential outputs. Differential output amplifiers require that some means of stabilizing the common mode output voltage is present. This can be done internally in the op amp or externally using switches and capacitors to sample the common mode output voltage and feed it back to the biasing circuitry of the amplifier. Although, differential operation increases the component count and the amplifier complexity, the signal swing is increased by a factor of two and the even harmonics are diminished.

First-order building blocks of this section will be useful for general signal processing as well as for higher-order switched capacitor filter applications. We should recall that the performance of the first-order blocks in the z-domain will approximate that in the time-domain only if the clock frequency is greater than the largest signal frequency.

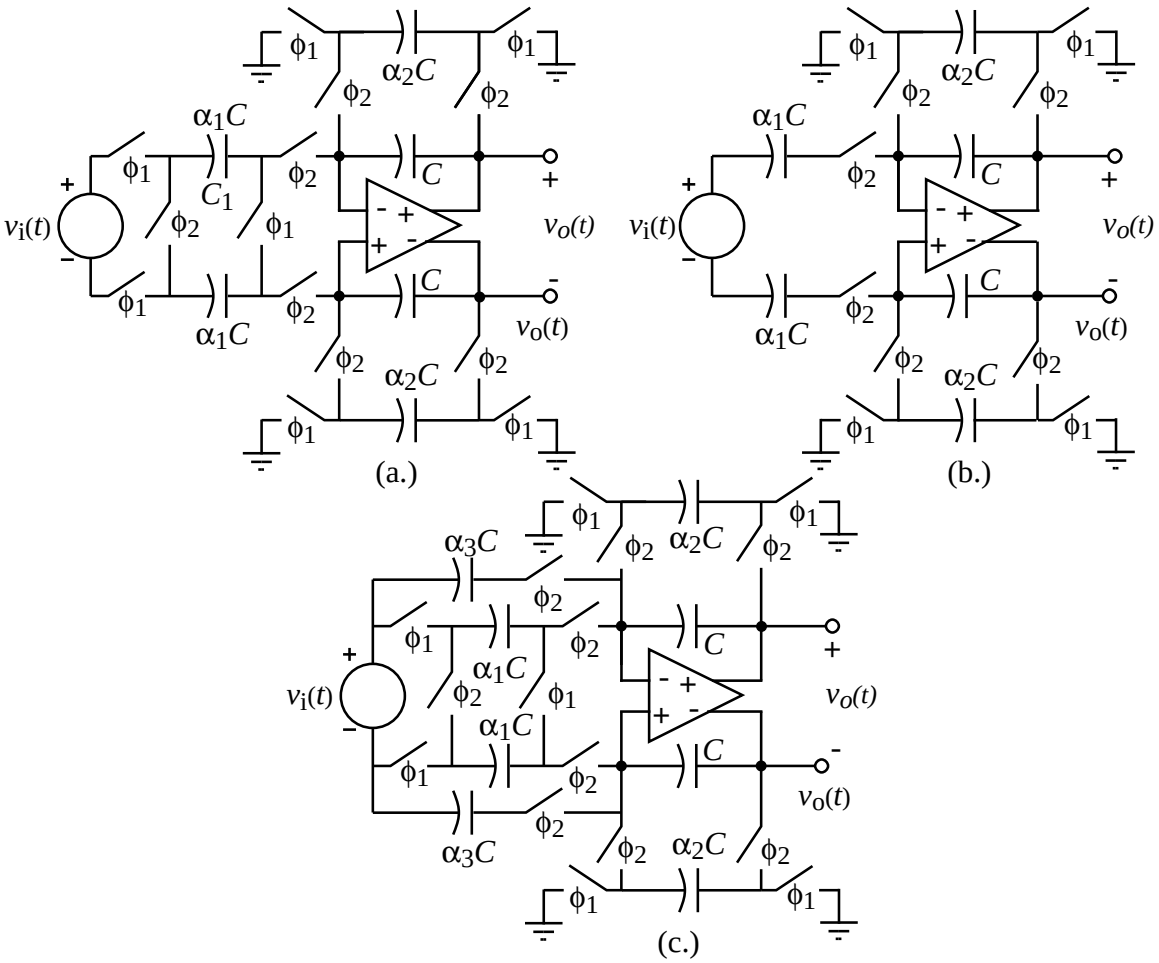


Figure 9.5-8 - Differential implementations of (a.) Fig. 9.5-1, (b.) Fig. 9.5-3, and (c.) Fig. 9.5-5.

9.6 - Second-Order Switched Capacitor Circuits

Second-order circuits have the advantage of potentially realizing complex poles and zeros which can be more efficient in designing frequency domain filters. One approach to designing higher order filters is to take the design in polynomial form and break it into products of second-order products. If the filter order is odd, then one first-order product will result. The implementation of each product can then be accomplished by a cascade of second-order circuits that each individually realize a pair of complex conjugate poles and two zeros (which may be at infinity or zero or in between). If the filter order is odd, then one of the products will be first-order requiring a realization from the last section. Fig. 9.6-1 illustrates the concept of cascade filter design.

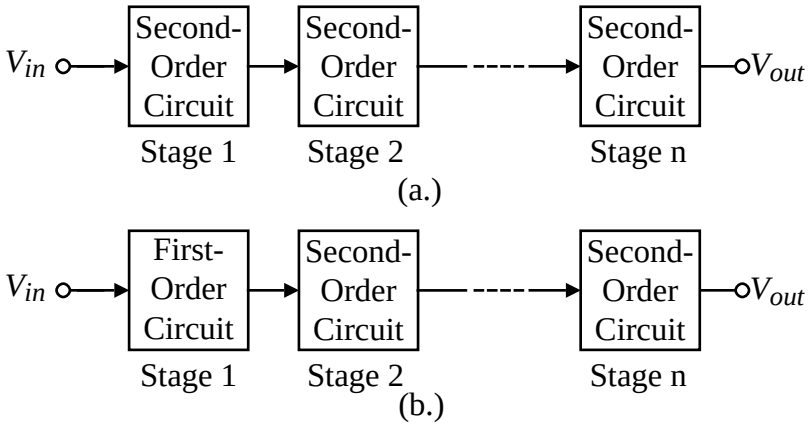


Figure 9.6-1 - (a.) Cascade design when n is even. (b.) Cascade designwhen n is odd.

In this section, we will focus on the second-order circuits implemented as switched capacitors. We will introduce several second-order, biquad circuits which provide general flexibility in cascade design. The biquad circuit has the ability to realize both complex poles and complex zeros. The poles are generated by the primary feedback path which generally consists of a noninverting integrator and an inverting integrator. One of the integrators is damped to avoid oscillation. The zeros are generated by how the input signal is applied to circuit. If there is more than one parallel signal path from the input to the output, zeros will result. The zero locations will determine the global frequency behavior of the biquad (i.e. lowpass, bandpass, highpass, all pass, notch, etc.). The poles influence the transition regions more strongly.

Low-Q, Switched Capacitor Biquad

We will develop two, switched capacitor biquad realizations in the following material. These two realizations are identical with those used in MicroSim's Filter Designer program[14] and therefore will be of further use to those with access to this program.

A biquad circuit in the continuous time domain can be written in general as

$$H_a(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{-(K_2 s^2 + K_1 s + K_0)}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad (1)$$

where ω_o is the pole frequency and Q the pole Q. K_0, K_1, and K_2 are arbitrary coefficients that determine the zero locations of the biquad. We can rewrite Eq. (1) as

$$s^2V_{out}(s) + \frac{\omega_o s}{Q}V_{out}(s) + \omega_o{}^2V_{out}(s) = -(K_2s^2 + K_1s + K_0)V_{in}(s) \qquad (2)$$

Dividing through by s^2 and solving for $V_{out}(s)$, gives

$$V_{out}(s) = \frac{-1}{s}\left[(K_1 + K_2s)V_{in}(s) + \frac{\omega_o}{Q}V_{out}(s) + \frac{1}{s}\left(K_0V_{in}(s) + \omega_o{}^2V_{out}(s)\right)\right] \qquad (3)$$

If we define the voltage $V_1(s)$ as

$$V_1(s) = \frac{-1}{s}\left[\frac{K_0}{\omega_o}V_{in}(s) + \omega_oV_{out}(s)\right] \qquad (4)$$

then Eq. (4) can be expressed as

$$V_{out}(s) = \frac{-1}{s}\left[(K_1 + K_2s)\,V_{in}(s) + \frac{\omega_o}{Q}V_{out}(s) - \omega_oV_1(s)\right] \qquad (5)$$

Equations (4) and (5) are both in the form of a voltage expressed as the sum of integrated inputs, including the voltage itself. Therefore it is easy to synthesize a two-integrator realization of these equations. The result is shown in Fig. 9.6-2. Note that the K_2s term is simply a charge amplifier similar to that found in Sec. 9.2. We are taking the liberty of using negative resistors because the next step will be a switched capacitor implementation which can realize negative transresistances.

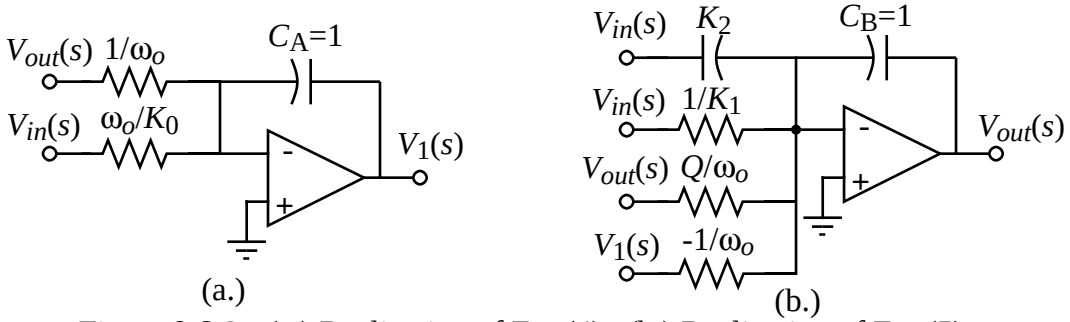


Figure 9.6-2 - (a.) Realization of Eq. (4). (b.) Realization of Eq. (5).

The circuits of Fig. 9.6-2 can be connected to form a continuous time biquad circuit (see Problem 9.6-1). However, let us use the previous switched capacitor circuits we have developed and implement Fig. 9.6-2 as two switched capacitor integrators where the output integrator has a non-integrated input. The result is shown in Fig. 9.6-3a and b. Fig. 9.6-4 shows the final switched capacitor biquad realization that we are seeking. Note that parallel switches with the same phasing have been combined in Fig. 9.6-4.

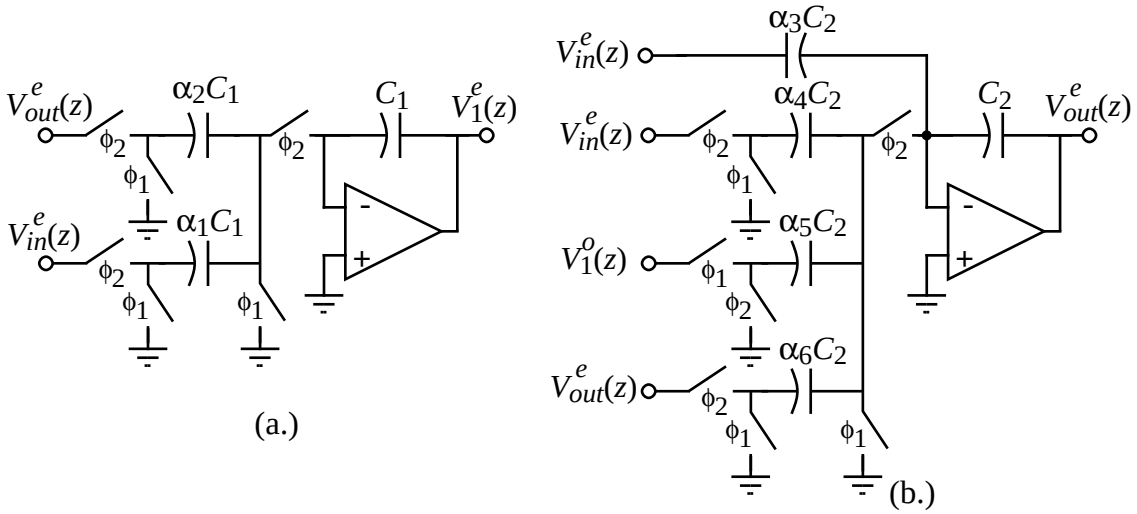


Figure 9.6-3 - (a.) Switched capacitor realization of Fig. 9.6-2a. (b.) Switched capacitor realization of Fig. 9.6-2b.

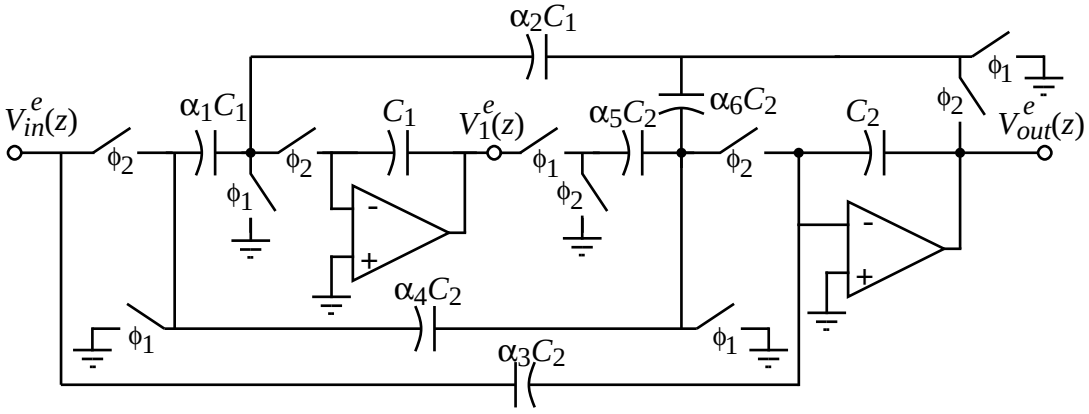


Figure 9.6-4 - Low Q, switched capacitor, biquad realization.

The outputs of Figs. 9.6-3a and 9.6-3b can be written as follows using the methods illustrated in Sec. 9.4.

$$V_1^e(z) = -\frac{\alpha_1}{1-z^{-1}} V_{in}^e(z) - \frac{\alpha_2}{1-z^{-1}} V_{out}^e(z) \tag{6}$$

and

$$V_{out}^e(z) = -\alpha_3 V_{in}^e(z) - \frac{\alpha_4}{1-z^{-1}} V_{in}^e(z) + \frac{\alpha_5 z^{-1}}{1-z^{-1}} V_1^e(z) - \frac{\alpha_6}{1-z^{-1}} V_{out}^e(z) . \tag{7}$$

Note that we multiplied the $V_1^o(z)$ input of Fig. 9.6-3b by $z^{-1/2}$ to convert it to $V_1^e(z)$. If we assume that $\omega T << 1$, then $1-z^{-1} \approx sT$ and Eqs. (6) and (7) can be approximated as

$$V_1^e(s) \approx -\frac{\alpha_1}{sT} V_{in}^e(s) - \frac{\alpha_2}{sT} V_{out}^e(s) = \frac{-1}{s}\left[\frac{\alpha_1}{T} V_{in}^e(s) + \frac{\alpha_2}{T} V_{out}^e(s)\right] \tag{8}$$

and

$$V_{out}^{e}(s) \approx \frac{-1}{s}\left[\left(\frac{\alpha_4}{T} + s\alpha_3\right)V_{in}^{e}(s) - \frac{\alpha_5}{T}V_1^{e}(s)\right] - \frac{\alpha_6}{T}V_{out}^{e}(s)\,. \qquad (9)$$

Eqs. (8) and (9) can be combined to give the transfer function, $H^{ee}(s)$ as follows.

$$H^{ee}(s) \approx \frac{-\left[\alpha_3 s^2 + \frac{s\alpha_4}{T} + \frac{\alpha_1\alpha_5}{T^2}\right]}{s^2 + \frac{s\alpha_6}{T} + \frac{\alpha_2\alpha_5}{T^2}} \qquad (10)$$

Comparing Eqs. (8) and (9) with Eqs. (4) and (5) gives

$$\alpha_1 = \frac{K_0 T}{\omega_o}, \quad \alpha_2 = |\alpha_5| = \omega_o T, \quad \alpha_3 = K_2, \quad \alpha_4 = K_1 T, \text{ and } \quad \alpha_6 = \frac{\omega_o T}{Q}\,. \qquad (11)$$

The relationships in Eq. (11) allow the design of a switched capacitor biquad given the coefficients of Eq. (1). Furthermore, they allow us to investigate the largest-to-smallest capacitor ratio of the biquad. If we focus only on the poles, it is obvious that if Q>1 and $\omega_o T$ <<1, the largest capacitor ratio (α) is α_5. If Q becomes too large, i.e. greater than 5, α_5 becomes too small which causes the biquad of Fig. 9.6-4 to be suitable for low-Q applications. If Q<1, the largest capacitor ratio is α_2 or α_5.

An additional property of the biquad is the *sum of the capacitances*. To find this value, normalize all of the capacitors connected or switched into the inverting terminal of each op amp by the smallest capacitor, $\alpha_{min}C$. The sum of the normalized capacitors associated with each op amp will be the sum of the capacitance connected to that op amp. This sum of the capacitors is given as

$$\Sigma C = \frac{1}{\alpha_{min}}\sum_{i=1}^{n}\alpha_i \qquad (12)$$

where there are n capacitors connected to the op amp inverting terminal, including the integrating capacitor.

Example 9.6-1

Design of a Switched Capacitor, Low-Q, Biquad

Assume that the specifications of a biquad are f_o = 1kHz, Q = 2, $K_0 = K_2 = 0$, and $K_1 = 2\pi f_o/Q$ (a bandpass filter). The clock frequency is 100kHz. Design the capacitor ratios of Fig. 9.6-4 and determine the maximum capacitor ratio and the total capacitance assuming that C_1 and C_2 have unit values.

Solution

From Eq. (11) we get $\alpha_1 = \alpha_3 = 0$, $\alpha_2 = \alpha_5 = 0.0628$, and $\alpha_4 = \alpha_6 = 0.0314$. The largest capacitor ratio is α_4 or α_6 and is 1/31.83. The sum of the capacitors connected to the input op amp of Fig. 9.6-4 is 1/0.0628 + 1 = 16.916. The sum of

capacitors connected to the second op amp is 0.0628/0.0314 + 2 + 1/0.0314 = 35.85. Therefore, the total biquad capacitance is 52.76 units of capacitance. Note that this number will decrease as the clock frequency becomes closer to the signal frequencies.

The switched capacitor, low-Q, biquad of Fig. 9.6-4 can also be designed in the z-domain. We can combine Eqs. (6) and (7) to get the following z-domain transfer function for Fig. 9.6-4.

$$\frac{V_{out}^{e}(z)}{V_{in}^{e}(z)} = H^{ee}(z) = -\frac{(\alpha_3 + \alpha_4)z^2 + (\alpha_1\alpha_5 - \alpha_4 - 2\alpha_3)z + \alpha_3}{(1 + \alpha_6)z^2 + (\alpha_2\alpha_5 - \alpha_6 - 2)z + 1} \tag{13}$$

A general *z*-domain specification for a biquad can be written as

$$H(z) = -\frac{a_2z^2 + a_1z + a_0}{b_2z^2 + b_1 z + 1} \tag{14}$$

Equating coefficients of Eqs. (13) and (14) gives

$$\alpha_3 = a_0,\ \alpha_4 = a_2\text{-}a_0,\ \alpha_1\alpha_5 = a_2\text{+}a_1\text{+}a_0,\ \alpha_6 = b_2\text{-}1, \text{ and } \alpha_2\alpha_5 = b_2\text{+}b_1\text{+}1 \tag{15}$$

Because there are 5 equations and 6 unknowns, an additional relationship can be introduced. One approach would be to select $\alpha_5 = 1$ and solve for the remaining capacitor ratios. Alternately, one could let $\alpha_2 = \alpha_5$ which makes the integrator frequency of both integrators in the feedback loop equal.

After designing the values of the capacitor ratios, one should also examine the voltages at V_1 and V_{out} to make sure that they have approximately the same magnitude of the frequency range of interest. If this is not the case, then a dynamic scaling can be employed to equalize the dynamic range seen by each op amp output. This dynamic range scaling can be accomplished by the following rule. *If the voltage at the output node of an op amp in a switched capacitor circuit is to be scaled by a factor of k, then all switched and unswitched capacitors connected to that output node must be scaled by a factor of 1/k.* This scaling is based on keep the total charge associated with a node constant. The choice above of $\alpha_2 = \alpha_5$ results in a near-optimally scaled dynamic range realization.

High-Q, Switched Capacitor Biquad

The switched capacitor biquad of Fig. 9.6-4 was seen to be limited to values of *Q* equal to 5 or less in order to avoid large element spreads. A biquad capable of realizing higher values of *Q* without suffering large element spreads is obtained by simply reformulating Eqs. (4) and (5). Starting with Eq. (3) let us reformulate equations for $V_1(s)$ and $V_{out}(s)$ as

$$V_{out}(s) = -\frac{1}{s}\ [K_2sV_{in} - \omega_oV_1(s)] \tag{16}$$

and

$$V_1(s) = -\frac{1}{s}\left[\left(\frac{K_0}{\omega_o} + \frac{K_1}{\omega_o}s\right)V_{in}(s) + \left(\omega_o + \frac{s}{Q}\right)V_{out}(s)\right] \qquad (17)$$

As before, we can synthesize these two equations as shown in Fig. 9.6-5. The next step is to realize the continuous time circuits of Fig. 9.6-5 as switched capacitor circuits. This is shown in Fig. 9.6-6.

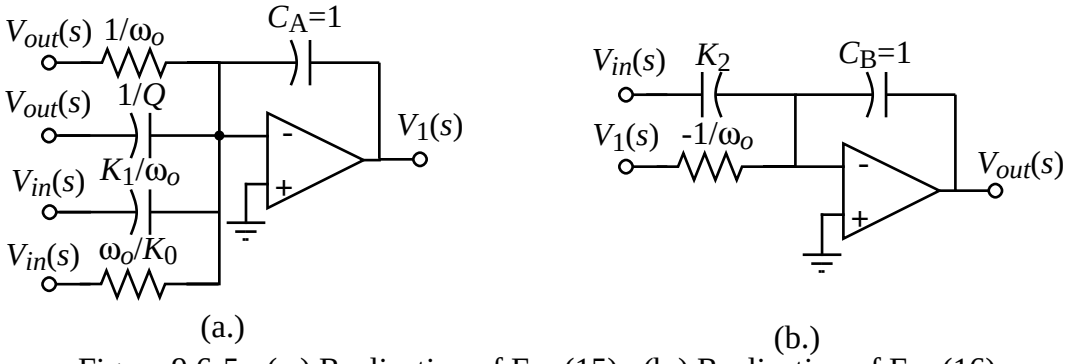


Figure 9.6-5 - (a.) Realization of Eq. (15). (b.) Realization of Eq. (16).

The outputs of Fig. 9.6-6 can be written as follows using the methods illustrated in Sec. 9.4.

$$V_{out}^{e}(z) = -\alpha_6 V_{in}^{e}(z) + \frac{\alpha_5 z^{-1}}{1-z^{-1}} V_1^{e}(z)\,. \qquad (17)$$

and

$$V_1^{e}(z) = -\frac{\alpha_1}{1-z^{-1}} V_{in}^{e}(z) - \frac{\alpha_2}{1-z^{-1}} V_{out}^{e}(z) - \alpha_3 V_{in}^{e}(z) - \alpha_4 V_{out}^{e}(z) \qquad (18)$$

Note that we multiplied the $V_1^{o}(z)$ input of Fig. 9.6-6b by $z^{-1/2}$ to convert it to $V_1^{e}(z)$, as was done previously. If we assume that $\omega T << 1$, then $1-z^{-1} \approx sT$ and Eqs. (17) and (18) can be approximated as

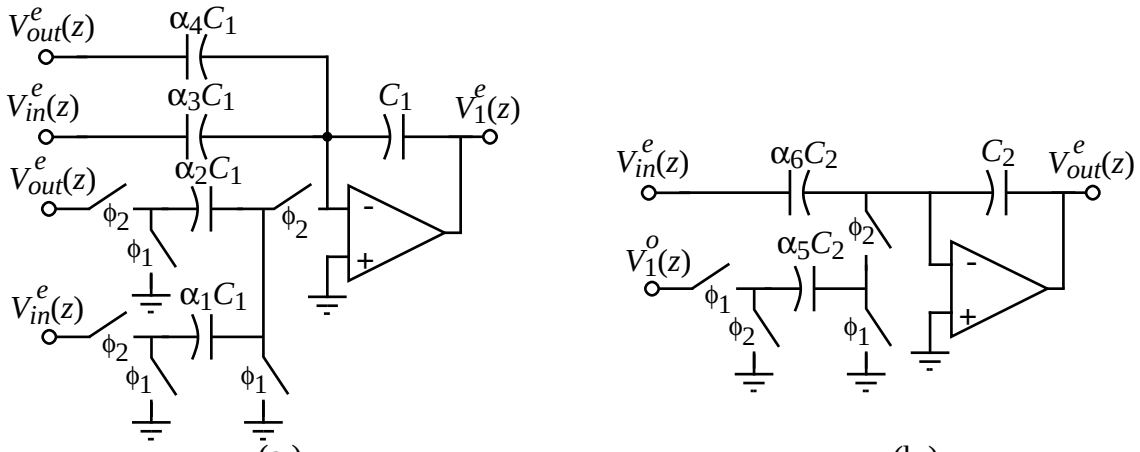


Figure 9.6-6 - (a.) Switched capacitor realization of Fig. 9.6-5a. (b.) Switched capacitor realization of Fig. 9.6-5b.

$$V_{out}^{e}(s) \approx \frac{-1}{s}\left[(s\alpha_6)V_{in}^{e}(s) - \frac{\alpha_5}{T}V_1^{e}(s)\right]. \tag{20}$$

and

$$V_1^{e}(s) \approx -\frac{1}{s}\left(\frac{\alpha_1}{T} + s\alpha_3\right)V_{in}^{e}(s) - \frac{1}{s}\left(\frac{\alpha_2}{T} + s\alpha_4\right)V_{out}^{e}(s) \tag{21}$$

The high Q biquad can be realized by making the connections implied in Fig. 9.6-6 to result in Fig. 9.6-7. Eqs. (20) and (21) can be combined to give the transfer function, $H^{ee}(s)$ of Fig. 9.6-7 as follows.

$$H^{ee}(s) \approx \frac{-\left[\alpha_6 s^2 + \frac{s\alpha_3\alpha_5}{T} + \frac{\alpha_1\alpha_5}{T^2}\right]}{s^2 + \frac{s\alpha_4\alpha_5}{T} + \frac{\alpha_2\alpha_5}{T^2}} \tag{21}$$

Comparing Eqs. (19) and (20) with Eqs. (15) and (16) gives

$$\alpha_1 = \frac{K_0 T}{\omega_o}, \quad \alpha_2 = |\alpha_5| = \omega_o T, \quad \alpha_3 = \frac{K_1}{\omega_o}, \quad \alpha_4 = \frac{1}{Q}, \text{ and } \quad \alpha_6 = K_2 . \tag{22}$$

The relationships in Eq. (22) allow the design of a switched capacitor biquad given the coefficients of Eq. (1). If Q>1 and $\omega_o T$ <<1, the largest capacitor ratio (α) is α_2 (α_5) or α_4, depending on the values of Q and $\omega_o T$. The high Q realization of Fig. 9.6-7 has eliminated the capacitor spread of $Q/\omega_o T$.

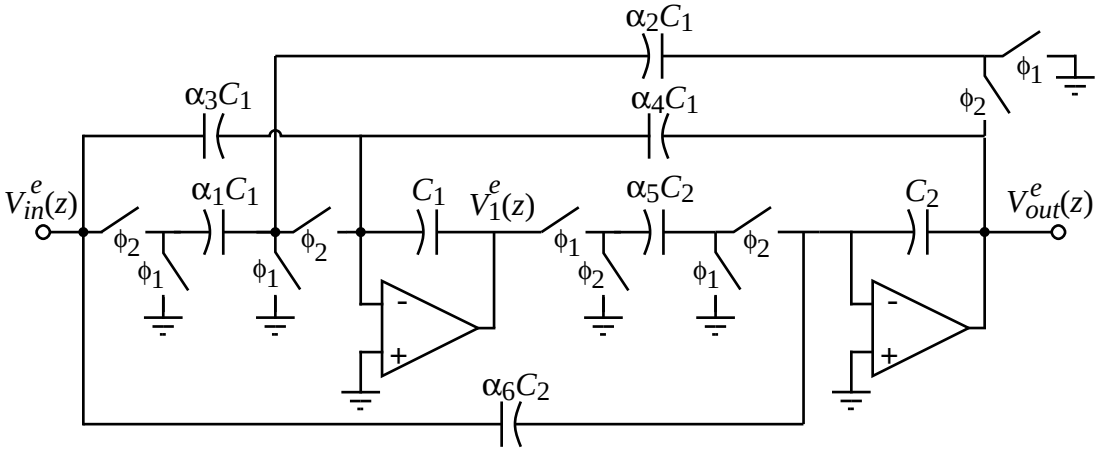


Figure 9.6-7 - High Q, switched capacitor, biquad realization.

Example 9.6-2

Design of a Switched Capacitor, High-Q, Biquad

Assume that the specifications of a biquad are f_o = 1kHz, Q = 10, $K_0 = K_2 = 0$, and $K_1 = 2\pi f_o/Q$ (a bandpass filter). The clock frequency is 100kHz. Design the

capacitor ratios of Fig. 9.6-4 and determine the maximum capacitor ratio and the total capacitance assuming that C_1 and C_2 have unit values.

Solution

From Eq. (23) we get $\alpha_1 = \alpha_6 = 0$, $\alpha_2 = \alpha_5 = 0.0628$, and $\alpha_3 = \alpha_4 = 0.1$. The largest capacitor ratio is α_2 or α_5 and is 1/15.92. The sum of the capacitors connected to the input op amp of Fig. 9.6-7 is 1/0.0628 + 2(0.1/0.0628) + 1 = 20.103. The sum of capacitors connected to the second op amp is 1/0.0628 + 1 = 16.916. Therefore, the total biquad capacitance is 36.02 units of capacitance.

The switched capacitor, high-Q, biquad of Fig. 9.6-7 can also be designed in the z-domain. We can combine Eqs. (18) and (19) to get the following z-domain transfer function for Fig. 9.6-7.

$$\frac{V_{out}^{e}(z)}{V_{in}^{e}(z)} = H^{ee}(z) = -\frac{\alpha_6 z^2 + (\alpha_3\alpha_5 - \alpha_1\alpha_5 - 2\alpha_6)z + (\alpha_6 - \alpha_3\alpha_5)}{z^2 + (\alpha_4\alpha_5 + \alpha_2\alpha_5 - 2)z + (1 - \alpha_4\alpha_5)} \tag{24}$$

A general *z*-domain specification for a biquad can be written as

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + 1} = -\frac{(a_2/b_2)z^2 + (a_1/b_2)z + (a_0/b_2)}{z^2 + (b_1/b_2)z + (b_0/b_2)} \tag{25}$$

Equating coefficients of Eqs. (24) and (25) gives

$$\alpha_6 = \frac{a_2}{b_2},\ \alpha_3\alpha_5 = \frac{a_2 - a_0}{b_2},\ \alpha_1\alpha_5 = \frac{a_2 + a_1 + a_0}{b_2},\ a_4\alpha_5 = 1 - \frac{1}{b_2} \text{ and } \alpha_2\alpha_5 = 1 + \frac{b_1 + 1}{2} \tag{26}$$

Because there are 5 equations and 6 unknowns, an additional relationship can be introduced. One approach would be to select $\alpha_5 = 1$ and solve for the remaining capacitor ratios. Alternately, one could let $\alpha_2 = \alpha_5$ which makes the integrator frequency of both integrators in the feedback loop equal.

The same considerations mentioned for the voltages at V_1 and V_{out} must be applied also to the high-*Q* biquad of Fig. 9.6-7. As before, the choice of $\alpha_2 = \alpha_5$ results in a near-optimally scaled dynamic range realization.

Fleischer-Laker, Switched Capacitor Biquad

In many cases, the previous two switched capacitor biquad realizations are suitable for the majority of switched capacitor filter applications. However, a general biquad capable of realizing any second-order z-transform is presented here for completeness. This biquad is called the *Fliescher-Laker biquad* [15, 16]. It has been used in many switched capacitor filter applications.

The Fleischer-Laker switched capacitor biquad circuit is shown in Fig. 9.6-8. Switches have been shared with various switched capacitor were appropriate. The shaded capacitors, *K* and *L*, will be used to provide further flexibility in reducing total capacitance and/or sensitivity of the Fleischer-Laker biquad. The primary integrator loop that defines the poles is made up of capacitors *A, B, C* and *D*. The switches in series with

the *K* and *L* capacitors are for the purposes of using the z-domain models to analyze this circuit.

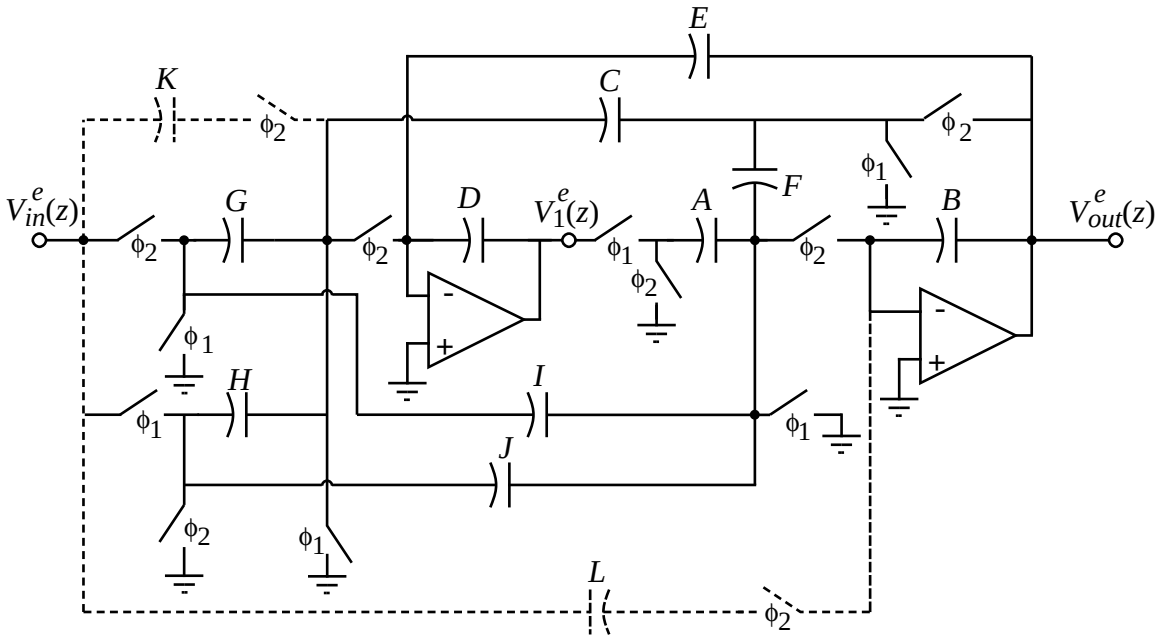


Figure 9.6-8 - Fleischer-Laker, switched capacitor biquad.

The z-domain transfer function of Fig. 9.6-8 can be found from the z-domain equivalent circuit shown in Fig. 9.6-9. The transfer function of the Fleischer-Laker biquad can be found as

$$\frac{V_{out}^e(z)}{V_{in}^e(z)} = \frac{(D\hat{J} - A\hat{H})z^{-2} - [D(\hat{I} + \hat{J}) - A\hat{G}]z - D\hat{I}}{(DB - AE)z^{-2} - [2DB - A(C + E) + DF]z^{-1} + D(B + F)} \tag{27}$$

and

$$\frac{V_1^e(z)}{V_{in}^e(z)} = \frac{(E\hat{J} - B\hat{H})z^{-2} + [B(\hat{G}+\hat{H}) + F\hat{H} - E(\hat{I} + \hat{J}) - C\hat{J}]z^{-1} - [\hat{I}(C+E) - \hat{G}(F+B)]}{(DB - AE)z^{-2} - [2DB - A(C + E) + DF]z^{-1} + D(B + F)} \tag{28}$$

where

$$\hat{G} = G+L, \quad \hat{H} = H+L, \quad \hat{I} = I+K \quad \text{and} \quad \hat{J} = J+L \tag{29}$$

These equations include the *K* and *L* capacitors. If they are left out, the "hatted" symbols become the symbols themselves. Note that the models for the *A* and *H* and *J* switched capacitors have been chosen to acquire the even samples of their respective inputs on the following odd phase.

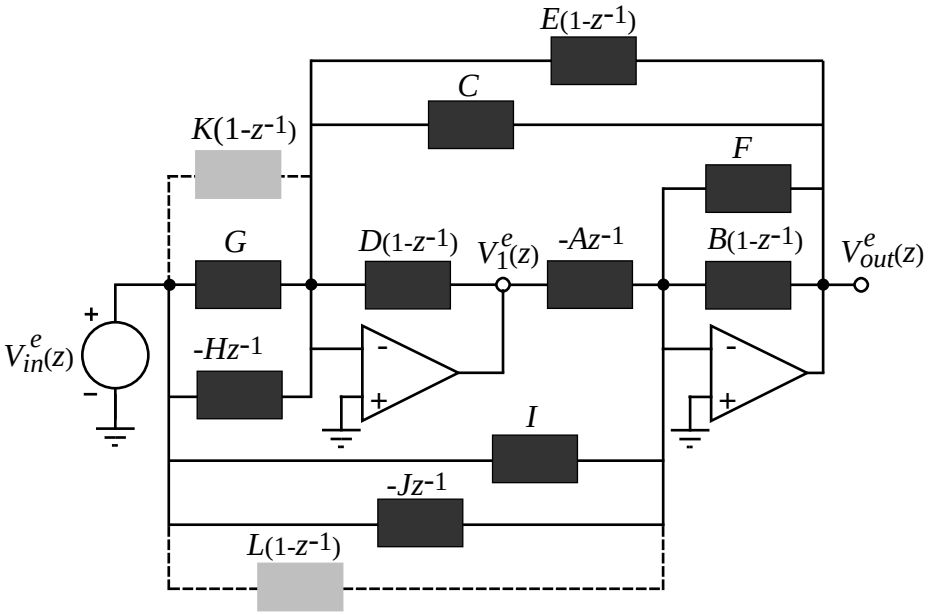


Figure 9.6-9 - z-domain equivalent circuit for the Fleischer-Laker biquad of Fig. 9.6-8.

In practice, rarely are all of the twelve capacitors required. The advantage of this general structure is that it provides a framework for the systematic design of specialized biquads. We will examine two cases of the general structure in the following material. Further information can be found in [15] concerning the details of the application of the Fleischer-Laker switched capacitor biquad. Both capacitors *E* and *F* create damping in the primary integrator loop. We will examine a biquad called *Type 1E* where $F = 0$ and a biquad called *Type 1F* where $E = 0$ and illustrate the design procedure used to design a biquad. In both of these cases, the *K* and *L* capacitors are also zero.

The z-domain transfer functions for the *Type 1E* can be found from Eqs. (27) and (28). They are written as

$$\frac{V_{out}^e}{V_{in}^e} = \frac{z^{-2}(JD - HA) + z^{-1}(AG - DJ - DI) + DI}{z^{-2}(DB - AE) + z^{-1}(AC + AE - 2BD) + BD} \tag{30}$$

and

$$\frac{V_1^e}{V_{in}^e} = \frac{z^{-2}(EJ - HB) + z^{-1}(GB + HB - IE - CJ - EJ) + (IC + IE - GB)}{z^{-2}(DB - AE) + z^{-1}(AC + AE - 2BD) + BD} \tag{31}$$

For the *Type 1F* biquad, the z-domain transfer function are

$$\frac{V_{out}^e}{V_{in}^e} = \frac{z^{-2}(JD - HA) + z^{-1}(AG - DJ - DI) + DI}{z^{-2}DB + z^{-1}(AC - 2BD - DF) + (BD + DF)} \tag{32}$$

and

$$\frac{V_1^e}{V_{in}^e} = \frac{-z^{-2}HB + z^{-1}(GB + HB + HF - CJ) + (IC + GF - GB)}{z^{-2}DB + z^{-1}(AC - 2BD - DF) + (BD + DF)} \tag{33}$$

The design procedure starts with knowing a z-domain transfer function and the numerical value of its coefficients. One simply matches coefficients and solve for the values of the capacitors. It may be necessary to introduce additional relationships to be able to solve for all the capacitors, uniquely. Useful constraints can be found in the sensitivity and element ratio considerations. The following example will illustrate the procedure.

Example 9.6-3

Design of a Switched Capacitor, Fleischer-Laker Biquad

Use the Fleischer-Laker biquad to implement the following z-domain transfer function which has poles in the z-domain at $r = 0.98$ and $\theta = \pm 6.2°$.

$$H(z) = \frac{0.003z^{-2} + 0.006z^{-1} + 0.003}{0.9604z^{-2} - 1.9485z^{-1} + 1}$$

Solution

Let us begin by selecting a *Type 1E* Fleischer-Laker biquad. Equating the numerator of Eq. (30) with the numerator of H(*z*) gives

$$DI = 0.003$$
$$AG\text{-}DJ\text{-}DI = 0.006 \rightarrow AG\text{-}DJ = 0.009$$
$$DJ\text{-}HA = 0.003$$

If we arbitrarily choose $H = 0$, we get

$$DI = 0.003$$
$$JD = 0.003$$
$$AG = 0.012$$

Picking $D = A = 1$ gives $I = 0.003$, $J = 0.003$ and $G = 0.012$. Equating the denominator terms of Eq. (30) with the denominator of H(z), gives

$$BD = 1$$
$$BD\text{-}AE = 0.9604 \rightarrow AE = 0.0396$$
$$AC\text{+}AE\text{-}2BD = -1.9485 \rightarrow AC\text{+}AE = 0.0515 \rightarrow AC = 0.0119$$

Because we have selected $D = A = 1$, we get $B = 1$, $E = 0.0396$, and $C = 0.0119$. If any capacitor value was negative, the procedure would have to be changed by making different choices or choosing a different realization such as *Type 1F*.

Since each of the alphabetic symbols is a capacitor, the largest capacitor ratio will be *D* or *A* divided by *I* or *J* which gives 333. The large capacitor ratio is being caused by the term $BD = 1$. If we switch to the *Type 1F*, the term $BD = 0.9604$ will

cause large capacitor ratios. This is an example is a case where both the E and F capacitors are needed to maintain a smaller capacitor ratio.

This section has introduced three, switched capacitor biquad circuits. The biquad is a very useful building block for switched capacitor filters which we will briefly examine in the next section. As with most switched capacitor circuits, practical implementation of these biquads will be in the form of a differential implementation using differential-in, differential-out op amps.

9.7 - Switched Capacitor Filters

One of the major applications of switched capacitor circuits is linear filters. In Sec. 9.1, we showed that the accuracy of the circuit time constants was proportional to the relative accuracy of capacitors. This accuracy was sufficient to implement practical filters in CMOS technology. During the late 1970's and early 1980's, the use of switched capacitor circuits to implement monolithic filters was developed to maturity [17, 18]. Because of the maturity of this field, it is important to provide a brief overview of the application of switched capacitor filters. More details concerning switched capacitor filter design can be found elsewhere [15, 19, 20].

Continuous Time Filter Theory

The objective of linear filters is frequency dependent processing on continous time signals. In otherwords, signals with various frequencies will be processed differently than signals made up from different frequencies. The processing is constrained to the amplitude and phase of a sinusoid. In an ideal, low pass filter filter, the frequencies of a signal below a certain frequency are amplified by 1 and the frequencies above are rejected. Although, the phase is important, most filter applications focus on the magnitude. It must be realized however, that if the phase is not linear with frequency, that the group delay of various signals will be different and a phase distortion will be seen in the signal processing of the filter.

An ideal filter would have a range of gain which is finite (*passband*) and a range of gain which is zero (*stopband*). Such a filter is not realizable according to circuit theory. As a consequence, practical filters have a passband of finite gain and a stopband with a small, but finite gain. In addition, the passband and stopband are separated by a frequency range called the *transition region.* In addition, it is desirable to control the variation of gain in the passband region so that its influence on the signal is controlled. For example, the passband gain could vary as much as -3dB before it could be detected by a listener hearing the sound passing through the filter. Or, the signal passing through the filter could be applied to an analog-to-digital converter. If the variation of the filter passband gain was not small enough, the converter would not work properly.

Based on the above discussion, all linear filters are characterized by three properties. These properties are the *passband ripple*, the *transition frequency*, and the *stopband gain/attenuation*. It is standard practice to normalize both the magnitude and frequency of a low pass filter. Let $T(j\omega)$ be a low pass filter as shown in Fig. 9.7-1a. $T(j0)$ is gain of the filter at $\omega = 0$. ω_{PB} is the upper passband frequency and ω_{SB} is the lower stopband frequency. The magnitude can be normalized using the following normalization.

$$T_n(j\omega) = \frac{T(j\omega)}{T(j0)} \tag{1}$$

The frequency can be normalized using the following normalization.

$$\omega_n = \frac{\omega}{\omega_{PB}} \tag{2}$$

Combining Eqs. (1) and (2), the normalized low pass transfer function can be expressed as

$$T_n(j\omega_n) = \frac{T(j\omega/\omega_{PB})}{T(0)} \quad . \tag{3}$$

Fig. 9.7-1b shows the amplitude and frequency normalized version of Fig. 9.7-1a. Note that the upper frequency of the passband is 1 and the lower frequency of the stopband ω_{SB}/ω_{SB}. The normalized stopband frequency is defined as

$$\Omega_n = \frac{\omega_{PB}}{\omega_{SB}} \quad . \tag{4}$$

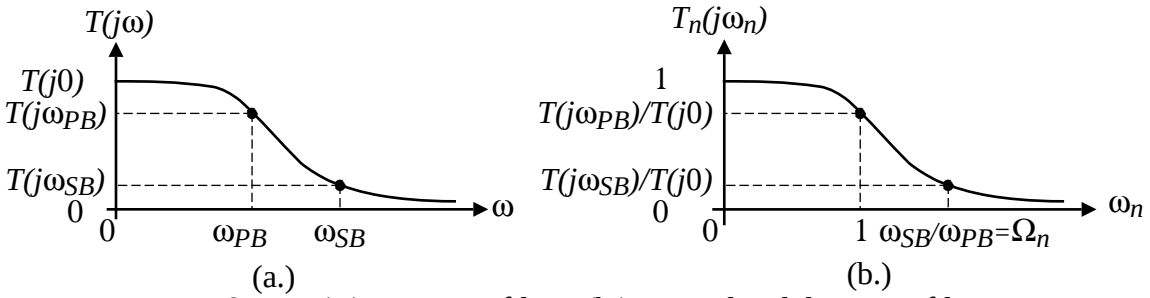


Figure 9.7-1 - (a.) Low pass filter. (b.) Normalized, low pass filter.

The two points on the low pass filter response in Fig. 9.7-1 are sufficient to characterize the filter for design purposes. This set of specifications consists of $T(j\omega_{PB})$, $T(j\omega_{SB})$, ω_{PB}, and ω_{SB}. However, if we normalize the filter as shown in Fig. 9.7-1b, there are only three specifications. Normally, $T(j0)$ is unity so that the three specifications are: 1.) $T(j\omega_{PB})$ called the *passband ripple*, 2.) $T(j\omega_{SB})$ called the *stopband gain/attentuation*, and 3.) Ω_n called the *transition frequency*. Most often, Fig. 9.7-1b is plotted with the magnitude scale in terms of *dB* and the frequency scale as $\log_{10}\omega$ (i.e. a *Bode plot*). Fig. 9.7-2 shows the low pass, normalized filter plotted as a Bode plot in terms of gain and in terms of attenuation. Either gain or attenuation can be used to describe filter specifications.

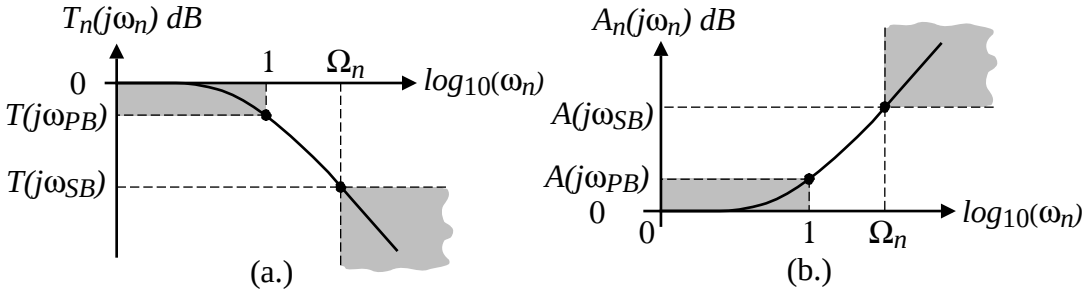


Figure 9.7-2 - (a.) Low pass filter of Fig. 9.7-1 as a Bode plot. (b.) Low pass filter of Fig. 9.7-2a shown in terms of attenuation *(A(jω) = 1/T(jω))*.

The process of filter design finds an approximation that will satisfy the specifications. The specifications are to be interpreted as follows. Between the normalized frequency of 0 and 1, the approximation to the filter must be within 0*dB* to

$T(j\omega_{PB})$. For normalized frequencies above Ω_n, the approximation to the filter must be equal to $T(j\omega_{SB})$ or less. In otherwords, the filter approximation must fall in the shaded areas of Fig. 9.7-2a or b. In between these regions is the transition region and the approximation should monotonically make the transition between the two shaded regions.

There are many filter approximations that have been developed for filter design. One of the more well used is the *Butterworth Approximation* [21]. The magnitude of the Butterworth filter approximation is maximally flat at low frequencies ($\omega \rightarrow 0$) and monotonically rolls off to a value approaching zero at high frequencies ($\omega \rightarrow \infty$). The magnitude of the normalized, Butterworth, low-pass filter approximation can be expressed as

$$|T_{LPn}(j\omega_n)| = \frac{1}{\sqrt{1 + \varepsilon^2 \omega_n^{2N}}} \tag{5}$$

where N is the order of the filter approximation and ε is defined in Fig. 9.7-3. Fig. 9.7-3 shows the magnitude response of the Butterworth filter approximation for several values of N.

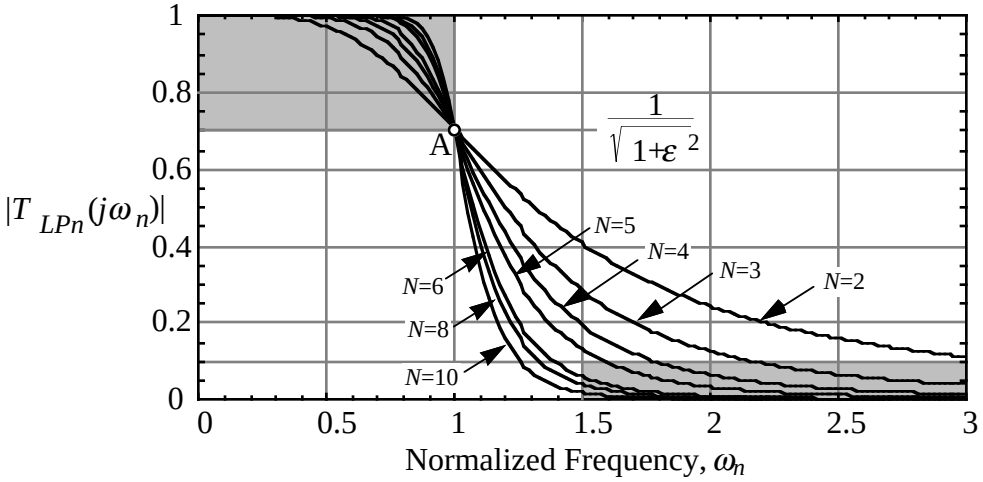


Figure 9.7-3 - Magnitude response of a normalized Butterworth low pass filter approximation for various orders, N, and for $\varepsilon = 1$.

The shaded area on Fig. 9.7-3 corresponds to the shaded area in the passband region of Figs. 9.7-2a . It is characteristic of all filter approximations that they pass through the point A as illustrated on Fig. 9.7-3. The value of ε can be used to adjust the width of the shaded area in Fig. 9.7-3. Normally, Butterworth filter approximations are given for an ε of unity as illustrated. We see from Fig. 9.7-3 that the higher the order of the filter approximation, the smaller the transition region for given value of T_{SB}. For example, if $T_{PB} = 0.707$ ($\varepsilon = 1$), $T_{SB} = 0.1$ and $\Omega_n = 1.5$ (illustrated by the both shaded areas of Fig. 9.7-3), then the order of the Butterworth filter approximation must be 6 or greater to satisfy the specifications. Note that the order must be an integer which means that even though $N = 6$ exceeds the specification it must be used because $N = 5$ does not meet the specification. The magnitude of the Butterworth filter approximation at ω_{SB} can be expressed from Eq. (5) as

$$\left| T_{LPn}\left(\frac{j\omega_{SB}}{\omega_{PB}}\right)\right| = |T_{LPn}(j\Omega_n)| = T_{SB} = \frac{1}{\sqrt{1 + \varepsilon^2\,\Omega_n^{2N}}} \quad . \tag{6}$$

This equation is useful for determining the order required to satisfy a given filter specification. Often, the filter specification is given in terms of *dB*. In this case, Eq. (6) is rewritten as

$$20\ log_{10}(T_{SB}) = T_{SB}\,(dB) = -10\ log_{10}\left(1 + \varepsilon^2\,\Omega_n^{2N}\right) \quad . \tag{7}$$

Example 9.7-1

Determining the Order of A Butterworth Filter Approximation

Assume that a normalized, low-pass filter is specified as T_{PB} = -3*dB*, T_{SB} = -20 *dB*, and Ω_n = 1.5. Find the smallest integer value of *N* of the Butterworth filter approximation which will satisfy this specification.

Solution

T_{PB} = -3*dB* corresponds to T_{PB} = 0.707 which implies that ε = 1. Thus, substituting ε = 1 and Ω_n = 1.5 into Eq. (7) gives

$$T_{SB}\,(dB) = -\,10\ log_{10}(1 + 1.5^{2N}) \quad .$$

Substituting values of *N* into this equation gives T_{SB} = -7.83 *dB* for *N* = 2, -10.93 *dB* for *N* = 3, -14.25 *dB* for *N* = 4, -17.68 *dB* for *N* = 5, and -21.16 *dB* for *N* = 6. Thus, *N* must be 6 or greater to meet the filter specification.

Once the order of the Butterworth filter approximation is known, then one must find the corresponding Butterworth function. Although there are a number of computer programs that can start with T_{PB}, T_{SB}, and Ω_n, and go directly to a realization of the filter in the continuous-time or discrete-time domain [14], we will outline the procedure such programs follow in order to be able understand their operation. If we assume that ε = 1, then Table 9.7-1 shows the pole locations for the low pass, normalized Butterworth approximations in the form of quadratic factors including the first-order product, (s_n+1) when the order is odd. It can be shown that all poles for the Butterworth approximation for ε = 1 lie on a unit circle in the left-half complex frequency plane.

Example 9.7-2

Finding the Butterworth Roots and Polynomial for a given *N*

Find the roots for a Butterworth approximation with ε =1 for *N* = 5.

Solution

For *N* = 5, the following first- and second-order products are obtained from Table 9.7-1

$$T_{LPn}(s_n) = T_1(s_n)T_2(s_n)T_3(s_n) = \left(\frac{1}{s_n+1}\right)\left(\frac{1}{s_n^2+0.6180s_n+1}\right)\left(\frac{1}{s_n^2+1.6180s_n+1}\right)$$

Table 9.7-1 - Pole locations and quadratic factors ($s_n^2 + a_1 s_n + 1$) of normalized, low pass Butterworth functions for $\varepsilon = 1$. Odd orders have a product (s_n+1).

N	Poles	a_1 coefficient
2	-0.70711 ± j0.70711	1.41421
3	-0.50000 ± j0.86603	1.00000
4	-0.38268 ± j0.92388	0.76536
	-0.92388 ± j0.38268	1.84776
5	-0.30902 ± j0.95106	0.61804
	-0.80902 ± j0.58779	1.61804
6	-0.25882 ± j0.96593	0.51764
	-0.70711 ± j0.70711	1.41421
	-0.96593 ± j0.25882	1.93186
7	-0.22252 ± j0.97493	0.44505
	-0.62349 ± j0.78183	1.24698
	-0.90097 ± j0.43388	1.80194
8	-0.19509 ± j0.98079	0.39018
	-0.55557 ± j0.83147	1.11114
	-0.83147 ± j0.55557	1.66294
	-0.98079 ± j0.19509	1.96158
9	-0.17365 ± j0.98481	0.34730
	-0.50000 ± j0.86603	1.00000
	-0.76604 ± j0.64279	1.53208
	-0.93969 ± j0.34202	1.87938
10	-0.15643 ± j0.98769	0.31286
	-0.45399 ± j0.89101	0.90798
	-0.70711 ± j0.70711	1.41421
	-0.89101 ± j0.45399	1.78202
	-0.98769 ± j0.15643	1.97538

In the above example, the contributions of the first-order term, $T_1(s_n)$, and the two second-order terms, $T_2(s_n)$ and $T_3(s_n)$, can be illustrated by plotting each one separately and then taking the products of all three. Figure 9.7-4 shows the result. Interestingly enough, we see that the magnitude of $T_2(s_n)$ has a peak that is about 1.7 times the gain of the fifth-order filter at low frequencies. If we plotted Fig. 9.7-4 with the vertical scale in dB, we could identify the Q by comparing the results with the standard, normalized second-order, magnitude response. Consequently, all filter approximations that are made up from first-order and/or second-order products do not necessarily have the properties of the filter approximation until all the terms are multiplied (added on a dB scale).

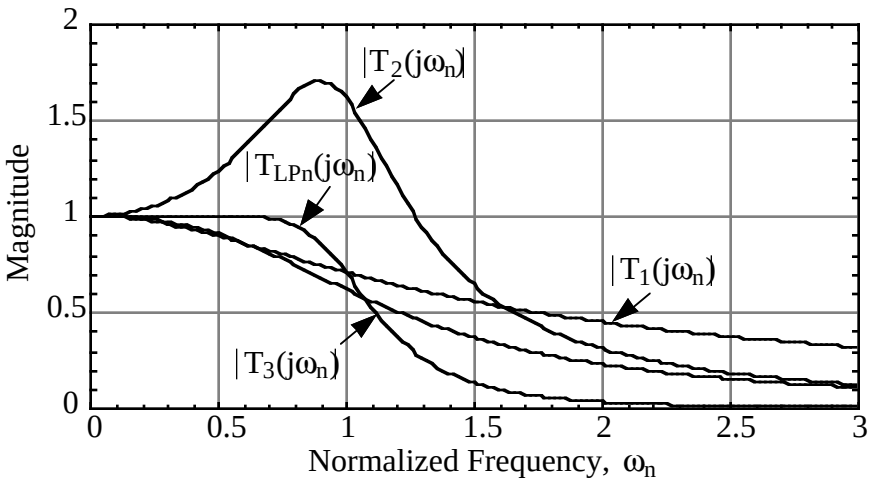


Figure 9.7-4 - Individual magnitude contributions of a fifth-order, Butterworth filter approximation.

A second useful filter approximation to the ideal normalized, low pass filter is called a Chebyshev filter approximation [22]. The Chebyshev low-pass filter approximation has equal-ripples in the passband and then is monotonic outside of the passband. The equal-ripple in the passband allows the Chebyshev filter approximation to fall off more quickly than the Butterworth filter approximation of the same order. This increased rolloff occurs only for frequencies just above ω_{PB}. As the frequency becomes large, filter approximations of the same order will have the same rate of decrease in the magnitude response. The magnitude of the normalized, Chebyshev, low-pass, filter approximation can be expressed as

$$|T_{LPn}(j\omega_n)| = \frac{1}{\sqrt{1 + \varepsilon^2 \cos^2[N\cos^{-1}(\omega_n)]}} \quad , \quad \omega_n \le 1 \tag{8}$$

and

$$|T_{LPn}(j\omega_n)| = \frac{1}{\sqrt{1 + \varepsilon^2 \cosh^2[N\cosh^{-1}(\omega_n)]}} \quad , \quad \omega_n > 1 \tag{9}$$

where N is the order of the filter approximation and ε is defined in Fig. 9.7-5. Fig. 9.7-5 shows the magnitude response of the Chebyshev filter approximation for ε = 0.5088.

The values of ε are normally chosen so that the ripple width is between 0.1*dB* (ε = 0.0233) and 1 *dB* (ε = 0.5088). We can show that the Chebyshev has a smaller transition region by considering the order necessary to satisfy the partial specification of $T_{SB} = 0.1$ and $\Omega_n = 1.5$. We see from Fig. 9.7-5 that $N = 4$ will easily satisfy this requirement. We also note that $T_{PB} = 0.8913$ which is better than 0.7071 of the Butterworth filter approximation. Thus, we see that ε determines the width of the passband ripple and is given as

$$|T_{LP}(\omega_{PB})| = |T_{LPn}(1)| = T_{PB} = \frac{1}{\sqrt{1+\varepsilon^2}} \quad . \tag{10}$$

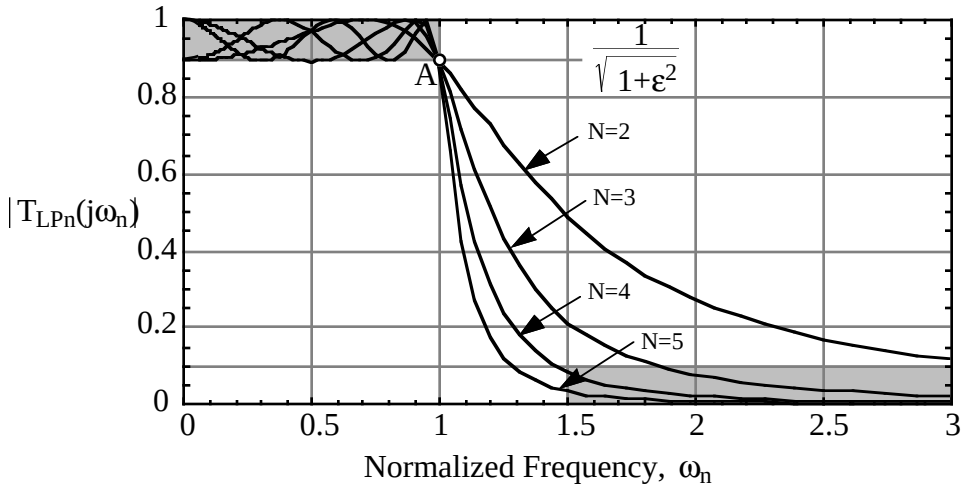


Figure 9.7-5 - Magnitude response of a normalized Chebyshev low-pass filter approximation for various orders of N and for $\varepsilon = 0.5088$.

The magnitude of the Chebyshev filter approximation at ω_{SB} can be expressed from Eq. (10) as

$$\left|T_{LPn}\left(\frac{\omega_{SB}}{\omega_{PB}}\right)\right| = |T_{LPn}(\Omega_n)| = T_{SB} = \frac{1}{\sqrt{1+\varepsilon^2\,cosh^2[Ncosh^{-1}(\Omega_n)]}} \quad . \qquad (11)$$

If the specifications are in terms of decibels, then the following is more convenient.

$$20\,log_{10}(T_{SB}) = T_{SB}\,(dB) = -10log_{10}\{1+\varepsilon^2 cosh^2[Ncosh^{-1}(\Omega_n)]\} \qquad (12)$$

Example 9.7-3

Determining the Order of A Chebyshev Filter Approximaton

Repeat Ex. 9.7-1 for the Chebyshev filter approximation.

Solution

In Ex. 9.7-2, ε = 1 which means the ripple width is 3 *dB* or $T_{PB} = 0.707$. Now we substitute $\varepsilon = 1$ into Eq. (12) and find the value of N which satisfies $T_{SB} = -20dB$. For $N = 2$, we get $T_{SB} = -11.22\ dB$. For $N = 3$, we get $T_{SB} = -19.14\ dB$. Finally, for $N = 4$, we get $T_{SB} = -27.43$ dB. Thus $N = 4$ must be used although $N = 3$ almost satisfies the specifications. This result compares with $N = 6$ for the Butterworth approximation.

As with the Butterworth approximations, we must be able to find the roots of the Chebyshev functions for various values of ε and N. We will illustrate a subset of this information by providing the polynomials and roots for $\varepsilon = 0.5088$ which corresponds to T_{PB} of $1dB$ for values of N up to 7. This information is found in Tables 9.7-2 .

Table 9.7-2 - Pole locations and quadratic factors ($a_0 + a_1 s_n + s_n^2$) of normalized, low pass Chebyshev functions for $\varepsilon = 0.5088$ (1*dB*).

N	Normalized Pole Locations	a_0	a_1
2	-0.54887 ± j0.89513	1.10251	1.09773
3	-0.24709 ± j0.96600 -0.49417	0.99420	0.49417
4	-0.13954 ± j0.98338 -0.33687 ± j0.40733	0.98650 0.27940	0.27907 0.67374
5	-0.08946 ± j0.99011 -0.23421 ± j0.61192 -0.28949	0.98831 0.42930	0.17892 0.46841
6	-0.06218 ± j0.99341 -0.16988 ± j0.72723 -0.23206 ± j0.26618	0.99073 0.55772 0.12471	0.12436 0.33976 0.46413
7	-0.04571 ± j0.99528 -0.12807 ± j0.79816 -0.18507 ± j0.44294 -0.20541	0.99268 0.65346 0.23045	0.09142 0.25615 0.37014

Example 9.7-4

Finding the Chebyshev Roots for a given *N*

Find the roots for the Chebyshev approximation with $\varepsilon = 1$ for $N = 5$.

Solution

For $N = 5$, we get the following quadratic factors which give the transfer function as

$$T_{LPn}(s_n) = T_1(s_n)T_2(s_n)T_3(s_n)$$

$$= \left(\frac{0.2895}{s_n+0.2895}\right)\left(\frac{0.9883}{s_n^2+0.1789s_n+0.9883}\right)\left(\frac{0.4239}{s_n^2+0.4684s_n+0.4239}\right).$$

The are many other filter approximations besides the Butterworth and Chebyshev that have been introduced above. One is the elliptic filter approximation which provides the smallest transition region possible for a given filter order, *N*. Other filter approximations result in filters with a more linear delay. These approximations and others can be found in the literature [23, 24].

Higher Order Filter Design - Cascade Approach

Fig. 9.7-6 shows the general design approach for continuous and switched capacitor filters of order higher than two. The two general approaches are the *cascade* and *ladder* filter design approaches. All approaches start with a normalized, low pass filter with a

passband of 1 radian/second and an impedance of 1Ω that will satisfy the filter specification. In the cascade approach, the root locations for the desired are identified and then transformed to the roots of an unnormalized low pass realizations. If the filter is to be low pass, then these roots are grouped into products of second-order functions. If the filter order is odd, then one first-order product is required. Next, the second-order and first-order functions are realized using low pass circuits that realize each product. If the filter is to be bandpass, high pass or bandstop, then a transformation is made on the low pass roots to the desired frequency characteristic. Again, the second-order and first-order (if any) products are identified and realized by the appropriate first- or second-order circuit.

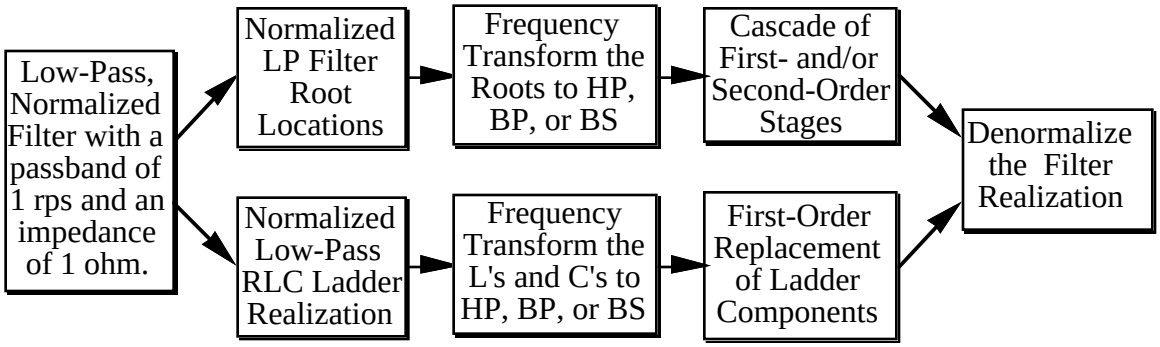


Figure 9.7-6 - General design approach for continuous and switched capacitor filters.

A design procedure for low pass, switched capacitor filters using the cascade approach can be outlined as follows.

1.) From T_{PB}, T_{SB}, and Ω_n (or A_{PB}, A_{SB}, and Ω_n) determine the required order of the filter approximation using Eq. (7) or Eq. (12).

2.) From tables similar to Table 9.7-1 and 9.7-2 find the normalized poles of the approximation.

3.) Group the complex-conjugate poles into second-order realizations. For odd-order realizations there will be one first-order term.

4.) Realize each of the second-order terms using the first- and second-order blocks of Secs. 9.5 and 9.6.

5.) Cascade the realizations in the order from input to output of the lowest-Q stage first (first-order stages generally should be first).

This design procedure will be illustrated by the following example. Much more information and detail can be found in other references [15, 19, 20, 23].

Example 9.7-5

Fifth-order, Low Pass, Switched Capacitor Filter using the Cascade Approach

Design a cascade, switched capacitor realization for a Chebyshev filter approximation to the filter specifications of T_{PB} = -1dB, T_{SB} = -25dB, f_{PB} = 1kHz and f_{SB} = 1.5kHz. Give a schematic and component value for the realization. Also simulate the realization and compare to an ideal realization. Use a clock frequency of 20kHz.

Solution

First we must find Ω_n from Eq. (4) as 1.5 and recall that when T_{PB} = -1dB that this corresponds to ε = 0.5088. From Eq. (13) we find that N = 5 satisfies the specifications (T_{SP} = -29.9dB). Using the results of Ex. 9.7-4, we may write $T_{LPn}(s_n)$ as

$$T_{LPn}(s_n) = \left(\frac{0.2895}{s_n+0.2895}\right)\left(\frac{0.9883}{s_n^2+0.1789s_n+0.9883}\right)\left(\frac{0.4239}{s_n^2+0.4684s_n+0.4239}\right).$$

Next, we design each of the three stages individually.

Stage 1 - First-order Stage

Let us select Fig. 9.5-1 to realize the first-order stage. We will assume that f_c is much greater than f_{PB} (i.e. 100) and use Eq. (10) of Sec. 9.5 repeated below to accomplish the design.

$$T_1(s) \approx \frac{\alpha_{11}/\alpha_{21}}{1 + s(T/\alpha_{21})} \tag{15}$$

Note that we have used the second subscript 1 to denote the first stage. Before we can use Eq. (15) we must normalize the sT factor. This normalization is accomplished by

$$sT = \left(\frac{s}{\omega_{PB}}\right)\cdot(\omega_{PB}T) = s_nT_n\,. \tag{16}$$

Therefore, Eq. (15) can be written as

$$T_1(s_n) \approx \frac{\alpha_{11}/\alpha_{21}}{1 + s_n(T_n/\alpha_{21})} = \frac{\alpha_{11}/T_n}{s_n + \alpha_{21}/T_n} \tag{17}$$

where $\alpha_{11} = C_{11}/C$ and $\alpha_{21} = C_{21}/C$. Equating Eq. (17) to the first term in $T_{LPn}(s_n)$ gives the design of Fig. 9.5-1 as

$$\alpha_{21} = \alpha_{11} = 0.2895T_n = \frac{0.2895\cdot\omega_{PB}}{f_c} = \frac{0.2895\cdot 2000\pi}{20{,}000} = 0.0909$$

The sum of capacitances for the first stage is

$$\text{First-stage capacitance} = 2 + \frac{1}{0.0909} = 13 \text{ units of capacitance}$$

Stage 2 - Second-order, High-Q Stage

The next product of $T_{LPn}(s_n)$ is

$$\frac{0.9883}{s_n^2 + 0.1789s_n + 0.9883} = \frac{T(0)\omega_n^2}{s_n^2 + \frac{\omega_n}{Q}s_n + \omega_n^2} \tag{18}$$

where we see that $T(0) = 1$, $\omega_n = 0.9941$ and $Q = (0.9941/0.1789) = 5.56$. Therefore, we will select the low pass version of the high-Q biquad of Fig. 9.6-7. First, we must normalize Eq. (21) of Sec. 9.6 according to the normalization of Eq. (16) to get

$$T_2(s_n) \approx \frac{-\left[\alpha_{62}s_n^2 + \frac{s_n\alpha_{32}\alpha_{52}}{T_n} + \frac{\alpha_{12}\alpha_{52}}{T_n^2}\right]}{s_n^2 + \frac{s_n\alpha_{42}\alpha_{52}}{T_n} + \frac{\alpha_{22}\alpha_{52}}{T_n^2}} \quad . \tag{19}$$

To get a low pass realization, select $\alpha_{32} = \alpha_{62} = 0$ to get

$$T_2(s_n) \approx \frac{-\frac{\alpha_{12}\alpha_{52}}{T_n^2}}{s_n^2 + \frac{s_n\alpha_{42}\alpha_{52}}{T_n} + \frac{\alpha_{22}\alpha_{52}}{T_n^2}} \quad . \tag{20}$$

Equating Eq. (20) to the middle term of $T_{LPn}(s_n)$ gives

$$\alpha_{12}\alpha_{52} = \alpha_{22}\alpha_{52} = 0.9883T_n^2 = \frac{0.9883\cdot\omega_{PB}{}^2}{f_c{}^2} = \frac{0.9883\cdot 4\pi^2}{400} = 0.09754$$

and

$$\alpha_{42}\alpha_{52} = 0.1789T_n^2 = \frac{0.1789\cdot\omega_{PB}{}^2}{f_c{}^2} = \frac{0.1789\cdot 2\pi}{20} = 0.05620$$

Choose $a_{12} = a_{22} = \alpha_{52}$ to get optimum voltage scaling. Thus we get, $\alpha_{12} = \alpha_{22} = \alpha_{52} = 0.3123$ and $\alpha_{42} = 0.05620/0.3123 = 0.1800$. The second-stage capacitance is

$$\text{Second-stage capacitance} = 1 + \frac{3(0.3123)}{0.1800} + \frac{1}{0.1800} = 11.76 \text{ units of capacitance}$$

Stage 3 - Second-order, Low-Q Stage

The last product of $T_{LPn}(s_n)$ is

$$\frac{0.4293}{s_n^2 + 0.4684s_n + 0.4293} = \frac{T(0)\omega_n^2}{s_n^2 + \frac{\omega_n}{Q}s_n + \omega_n^2} \tag{21}$$

where we see that $T(0) = 1$, $\omega_n = 0.6552$ and $Q = (0.6552/0.4684) = 1.3988$. Therefore, we will select the low pass version of the low-Q biquad of Fig. 9.6-4. First, we must normalize Eq. (10) of Sec. 9.6 according to the normalization of Eq. (16) to get

$$T_3(s_n) \approx \frac{-\left[\alpha_{33}s_n^2 + \frac{s_n\alpha_{43}}{T_n} + \frac{\alpha_{13}\alpha_{53}}{T_n^2}\right]}{s_n^2 + \frac{s_n\alpha_{63}}{T_n} + \frac{\alpha_{23}\alpha_{53}}{T_n^2}} \quad . \tag{22}$$

To get a low pass realization, select $\alpha_{33} = \alpha_{43} = 0$ to get

$$T_3(s_n) \approx \frac{-\frac{\alpha_{13}\alpha_{53}}{T_n^2}}{s_n^2 + \frac{s_n\alpha_{63}}{T_n} + \frac{\alpha_{23}\alpha_{53}}{T_n^2}} \quad . \tag{23}$$

Equating Eq. (23) to the last term of $T_{LPn}(s_n)$ gives

$$\alpha_{13}\alpha_{53} = \alpha_{23}\alpha_{53} = 0.4293T_n^2 = \frac{0.4239\cdot\omega_{PB}{}^2}{f_c{}^2} = \frac{0.4239\cdot 4\pi^2}{400} = 0.04184$$

and

$$\alpha_{63} = 0.4684T_n^2 = \frac{0.4684\cdot\omega_{PB}{}^2}{f_c{}^2} = \frac{0.4684\cdot 2\pi}{20} = 0.1472$$

Choose $a_{13} = a_{23} = \alpha_{53}$ to get optimum voltage scaling. Thus we get, $\alpha_{13} = \alpha_{23} = \alpha_{53} = 0.2045$ and $\alpha_{43} = 0.1472$. The third-stage capacitance is

$$\text{Third-stage capacitance} = 1 + \frac{3(0.2045)}{0.1472} + \frac{1}{0.1472} = 11.96 \text{ units of capacitance}$$

Although it would advisable to use the high-Q realization of Fig. 9.6-7 for the third stage in order to reduce the required capacitance, we will leave the design as is for illustration purposes. The total capacitance of this design is 36.72 units of capacitance.

Fig. 9.7-7 shows the resulting design with the low-Q stage connected before the high-Q stage in order to maximize the dynamic range. Fig. 9.7-8 shows the simulated filter response for this example. Fig. 9.7-9 shows the magnitude of the output voltage of each stage in the filter realization. There appears to be a sinx/x effect on the magnitude which causes the passband specification not to be satisfied. This could be avoided by prewarping the specifications before designing the filter.

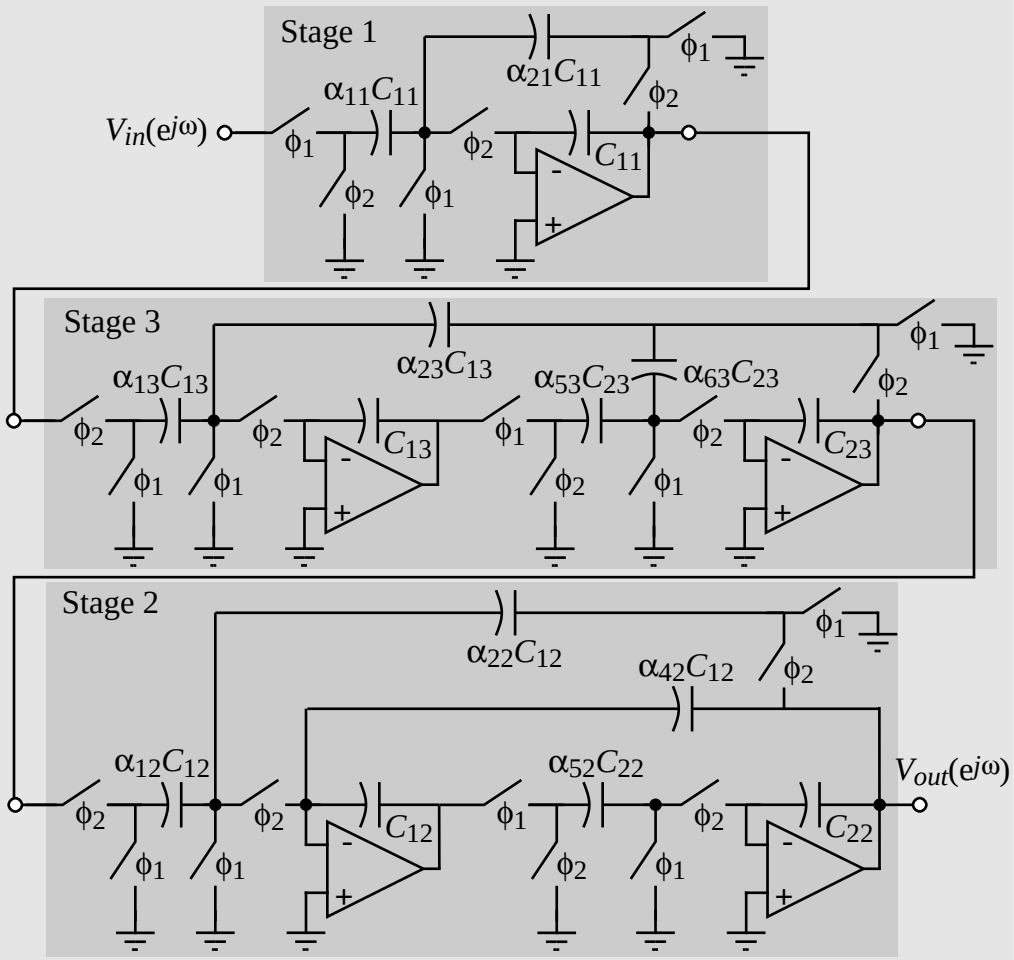


Figure 9.7-7 - Fifth-order, Chebyshev, low pass, switched capacitor filter of Example 9.7-5.

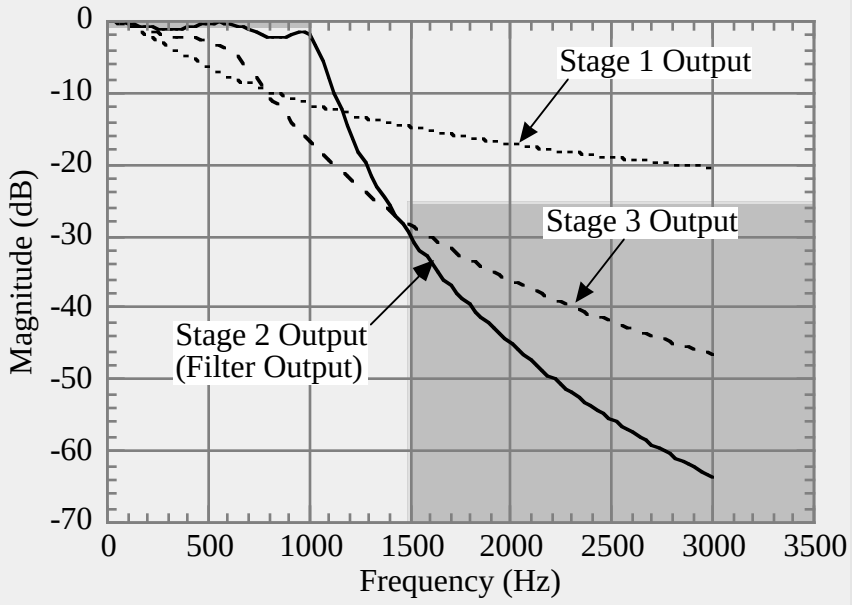


Figure 9.7-8a - Simulated magnitude response of Ex. 9.7-5

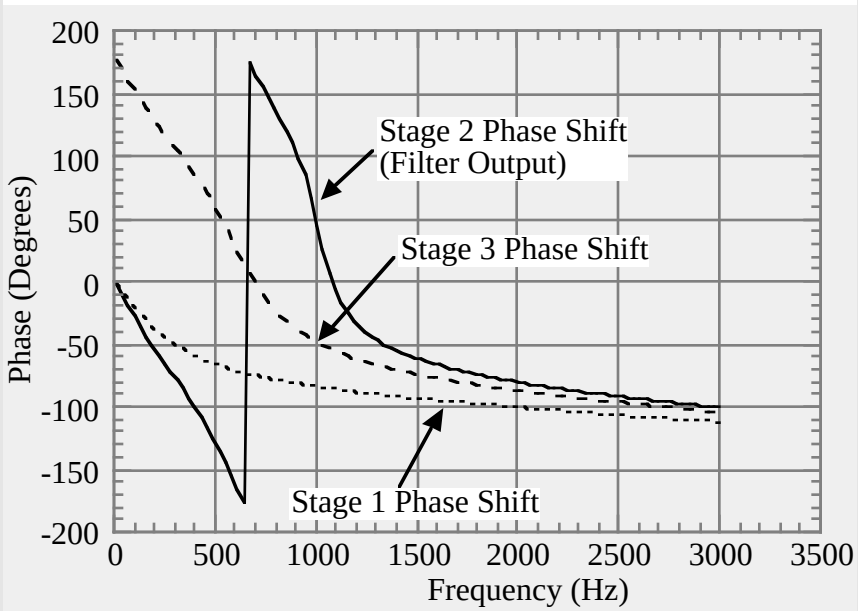


Figure 9.7-8b - Simulated phase response of Ex. 9.7-5

```
******** 08/29/97 13:17:44 *********
*******PSpice 5.2 (Jul 1992) ********

*SPICE FILE FOR EXAMPLE 9.7-5
*EXAMPLE 9-7-5: nodes 5 is the output *of
1st stage, node 13 : second stage (in *the
figure it is second while in design it *is third,
low Q stage), and node 21 is the *final output
of the *filter.

**** CIRCUIT DESCRIPTION ****

VIN    1 0 DC 0 AC 1

*.PARAM CNC=1 CNC_1=1 CPC_1=1

XNC1    1 2 3 4 NC1
XUSCP1    3 4 5 6 USCP
XPC1    5 6 3 4 PC1
XAMP1    3 4 5 6 AMP

XPC2    5 6 7 8 PC2
XUSCP2    7 8 9 10 USCP
XAMP2    7 8 9 10 AMP
XNC3    9 10 11 12 NC3
XAMP3    11 12 13 14 AMP
XUSCP3    11 12 13 14 USCP
XPC4    13 14 11 12 PC4
XPC5    13 14 7 8 PC2

XPC6    13 14 15 16 PC6
XAMP4    15 16 17 18 AMP
XUSCP4    15 16 17 18 USCP
XNC7    17 18 19 20 NC7
XAMP5    19 20 21 22 AMP
XUSCP5 19 20 21 22 USCP
XUSCP6    21 22 15 16 USCP1
XPC8    21 22 15 16 PC6

.SUBCKT DELAY 1 2 3
ED    4 0 1 2 1
TD    4 0 3 0 ZO=1K TD=25US
RDO    3 0 1K
.ENDS DELAY

.SUBCKT NC1 1 2 3 4
RNC1    1 0 11.0011
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 0.0909
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.0909
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.0909
RNC2    4 0 11.0011
.ENDS NC1

.SUBCKT NC3 1 2 3 4
RNC1    1 0 4.8581
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 0.2058
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.2058
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.2058
RNC2    4 0 4.8581
.ENDS NC3
```

```
.SUBCKT NC7 1 2 3 4
RNC1    1 0 3.2018
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 0.3123
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.3123
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.3123
RNC2    4 0 3.2018
.ENDS NC7

.SUBCKT PC1 1 2 3 4
RPC1    2 4 11.0011
.ENDS PC1

.SUBCKT PC2 1 2 3 4
RPC1    2 4 4.8581
.ENDS PC2

.SUBCKT PC4 1 2 3 4
RPC1    2 4 6.7980
.ENDS PC4

.SUBCKT PC6 1 2 3 4
RPC1    2 4 3.2018
.ENDS PC6

.SUBCKT USCP 1 2 3 4
R1    1 3 1
R2    2 4 1
XUSC1    1 2 12 DELAY
GUSC1    1 2 12 0 1
XUSC2    1 4 14 DELAY
GUSC2    4 1 14 0 1
XUSC3    3 2 32 DELAY
GUSC3    2 3 32 0 1
XUSC4    3 4 34 DELAY
GUSC4    3 4 34 0 1
.ENDS USCP

.SUBCKT USCP1 1 2 3 4
R1    1 3 5.5586
R2    2 4 5.5586
XUSC1    1 2 12 DELAY
GUSC1    1 2 12 0 0.1799
XUSC2    1 4 14 DELAY
GUSC2    4 1 14 0 .1799
XUSC3    3 2 32 DELAY
GUSC3    2 3 32 0 .1799
XUSC4    3 4 34 DELAY
GUSC4    3 4 34 0 .1799
.ENDS USCP1


.SUBCKT AMP 1 2 3 4
EODD    3 0 1 0 1E6
EVEN    4 0 2 0 1E6
.ENDS AMP

.AC LIN 100 10 3K
.PRINT AC V(5) VP(5) V(13) VP(13) V(21) VP(21)
.PROBE
.END
```

Figure 9.7-9 - SPICE input file for the simulation of Fig. 9.7-7.

Example 9.7-5 clearly illustrates the cascade design procedure for low pass filters. If the filter is to be high pass, bandpass, or bandstop, we must first transform the low pass normalized roots accordingly. Let us briefly outline how this could be accomplished. First, let s_{ln} be the normalized, low-pass frequency variable, the *normalized, low-pass to normalized, high-pass transformation* is defined as

$$s_{ln} = \frac{1}{s_{hn}} \tag{24}$$

where s_{hn} is the normalized, high-pass frequency variable (normally the subscripts h and l are not used when the meaning is understood). We have seen from the previous work that a general form of the normalized, low-pass transfer function is

$$T_{LPn}(s_{ln}) = \frac{p_{1ln}p_{2ln}p_{3ln}\cdots p_{Nln}}{(s_{ln}+p_{1ln})(s_{ln}+p_{2ln})(s_{ln}+p_{3ln})\cdots(s_{ln}+p_{Nln})} \tag{25}$$

where p_{kln} is the kth normalized, low-pass pole. If we apply the normalized, low-pass to high-pass transformation to Eq. (25) we get

$$\begin{aligned} T_{HPn}(s_{hn}) &= \frac{p_{1ln}p_{2ln}p_{3ln}\cdots p_{Nln}}{\left(\frac{1}{s_{hn}}+p_{1ln}\right)\left(\frac{1}{s_{hn}}+p_{2ln}\right)\left(\frac{1}{s_{hn}}+p_{3ln}\right)\cdots\left(\frac{1}{s_{hn}}+p_{Nln}\right)} \\ &= \frac{s_{hn}^N}{\left(s_{hn}+\frac{1}{p_{1ln}}\right)\left(s_{hn}+\frac{1}{p_{2ln}}\right)\left(s_{hn}+\frac{1}{p_{3ln}}\right)\cdots\left(s_{hn}+\frac{1}{p_{Nln}}\right)} \\ &= \frac{s_{hn}^N}{(s_{hn}+p_{1hn})(s_{hn}+p_{2hn})(s_{hn}+p_{3hn})\cdots(s_{hn}+p_{Nhn})} \end{aligned} \tag{26}$$

where p_{khn} is the kth normalized high-pass pole. At this point, the products of the filter approximation are broken into quadratic factors and one first-order product if the filter is odd. The realizations use the switched capacitor circuits of Secs. 9.5 and 9.6 that are high pass to achieve the implementation. Because of the clock frequency, the high pass filter will not continue to pass frequencies above the Nyquist frequency ($0.5f_c$). The high pass filter specifications can be translated to the normalized low pass specifications by using the following definition for Ω_n.

$$\Omega_n = \frac{1}{\Omega_{hn}} = \frac{\omega_{PB}}{\omega_{SB}} \tag{27}$$

We will now show how to design bandpass filters which are based on the normalized, low-pass filter. First, we define the width of the passband and the width of the stopband of the bandpass filter as

$$BW = \omega_{PB2} - \omega_{PB1} \tag{28}$$

and

$$SW = \omega_{SB2} - \omega_{SB1} , \tag{29}$$

respectively. ω_{PB2} is the larger passband frequency and ω_{PB1} is the smaller passband frequency of the bandpass filter. ω_{SB2} is the larger stopband frequency and ω_{SB1} is the smaller stopand frequency. Our study here only pertains to a certain category of bandpass filters. This category is one where the passband and stopband are geometrically centered about a frequency, ω_r, which is called *the geometric center frequency* of the bandpass filter. The geometric center frequency of the bandpass filter is defined as

$$\omega_r = \sqrt{\omega_{PB1}\omega_{PB2}} = \sqrt{\omega_{SB2}\omega_{SB1}} . \tag{30}$$

The geometrically centered bandpass filter can be developed from the normalized low-pass filter by the use of a frequency transformation. If s_b is the bandpass complex frequency variable, then we define a *normalized low-pass to unnormalized bandpass transformation* as

$$s_{ln} = \frac{1}{BW}\left(\frac{s_b^2 + \omega_r^2}{s_b}\right) = \frac{1}{BW}\left(s_b + \frac{\omega_r^2}{s_b}\right). \tag{31}$$

A *normalized low-pass to normalized bandpass transformation* is achieved by dividing the bandpass variable, s_b, by the geometric center frequency, ω_r, to get

$$s_{ln} = \left(\frac{\omega_r}{BW}\right)\left(\frac{s_b}{\omega_r} + \frac{1}{(s_b/\omega_r)}\right) = \left(\frac{\omega_r}{BW}\right)\left(s_{bn} + \frac{1}{s_{bn}}\right) \tag{32}$$

where

$$s_{bn} = \frac{s_b}{\omega_r} . \tag{33}$$

We can multiply Eq. (32) by BW/ω_r and define yet a further normalization of the low-pass, complex frequency variable as

$$s'_{ln} = \left(\frac{BW}{\omega_r}\right)s_{ln} = \Omega_b s_{ln} = \Omega_b\left(\frac{s_l}{\omega_{PB}}\right) = \left(s_{bn} + \frac{1}{s_{bn}}\right) \tag{34}$$

where Ω_b is a bandpass normalization of the low-pass frequency variable given as

$$\Omega_b = \frac{BW}{\omega_r} . \tag{35}$$

We will call the normalization of Eq. (34) a *bandpass normalization* of the low-pass complex frequency variable.

In order to be able to use this transformation, we need to solve for s_{bn} in terms of s'_{ln}. From Eq. (34) we get the following quadratic equation.

$$s_{bn}^2 - s'_{ln}\, s_{bn} + 1 = 0 . \tag{36}$$

Solving for s_{bn} from Eq. (36) gives

$$s_{bn} = \left(\frac{s_{ln}'}{2}\right) \pm \sqrt{\left(\frac{s_{ln}'}{2}\right)^2 - 1} \quad . \tag{37}$$

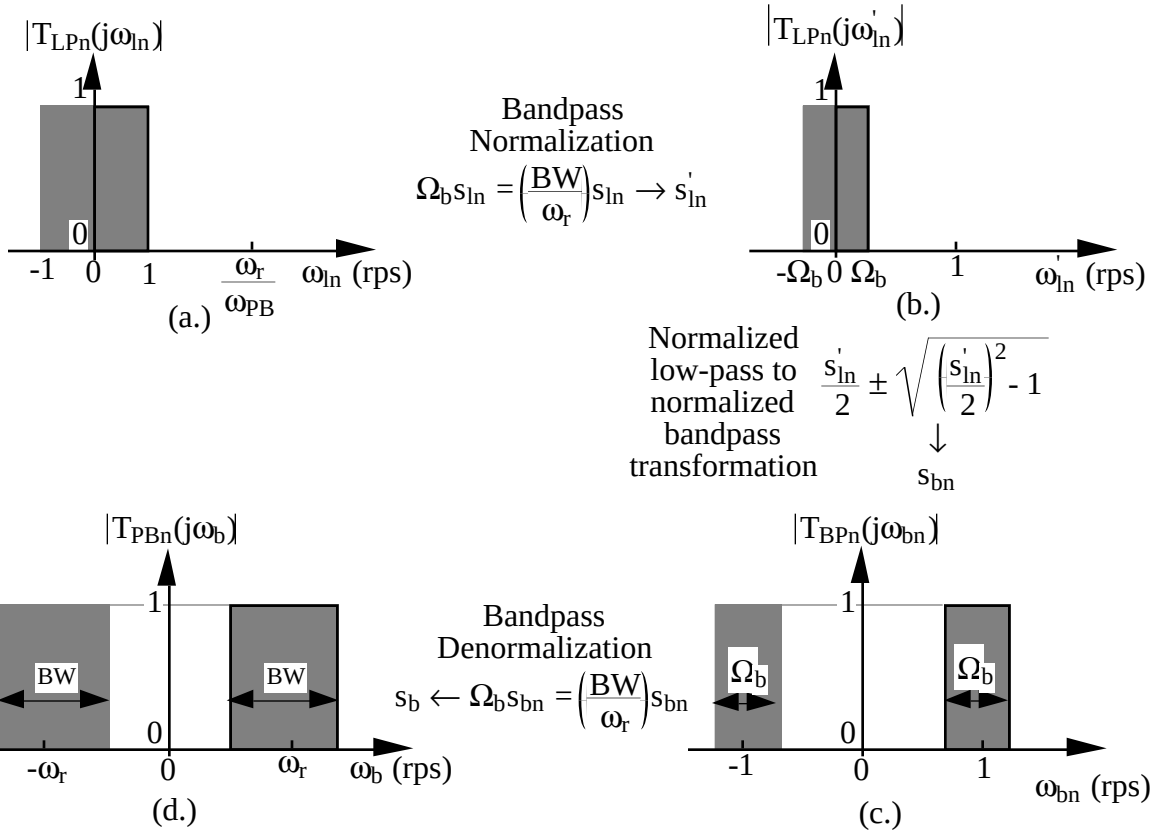


Figure 9.7-10 - Illustration of the development of a bandpass filter from a low-pass filter. (a.) Ideal normalized, low-pass filter. (b.) Normalization of (a.) for bandpass transformation. (c.) Application of low-pass to bandpass transformation. (d.) Denormalized bandpass filter.

Once the normalized, low-pass poles, p_{kln}', are known, then the normalized bandpass poles can be found from Figure 9.7-10 shows how transformation of Eq. (31) is used to create an unnormalized bandpass filter from an unnormalized low-pass filter. We must remember that the low-pass filter magnitude includes negative frequencies as indicated by the area enclosed by dashed lines to the left of the vertical axis of Fig. 9.7-10a. The low-pass filter has been amplitude normalized so that the passband gain is unity. Fig. 9.7-10b shows the normalization of the frequency by ω_{PBl}. Next, the low-pass to bandpass transformation of Eq. (32) is applied to get the normalized, band-pass magnitude in Fig. 9.7-10c. Finally, the bandpass filter is frequency denormalized to get the frequency unnormalized bandpass magnitude response of Fig. 9.7-10d. The stopbands of the bandpass filter were not included for purposes of simplicity but can be developed in the same manner.

The normalized bandpass poles can be found from the normalized, low pass poles, p_{kln}' using

$$p_{kbn} = \frac{p'_{kln}}{2} \pm \sqrt{\left(\frac{p'_{kln}}{2}\right)^2 - 1} \quad . \tag{38}$$

which is written from Eq. (37). For each pole of the low-pass filter, two poles result for the bandpass filter. Consequently, the order of complexity based on poles is $2N$ for the bandpass filter. If the low-pass pole is on the negative real axis, the two bandpass poles are complex conjugates. However, if the low-pass pole is complex, two bandpass poles result from this pole and two bandpass poles result from its conjugate. Fig. 2-15 shows how the complex conjugate low-pass poles contribute to a pair of complex conjugate bandpass poles. p^* is the designation for the conjugate of p. This figure shows that both poles of the complex conjugate pair must be transformed in order to identify the resulting two pairs of complex conjugate poles.

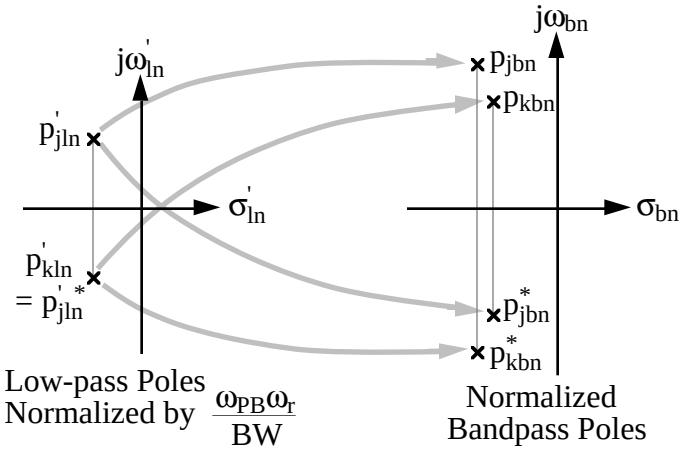


Figure 9.7-11 - Illustration of how the normalized, low-pass, complex conjugate poles are transformed into two normalized, bandpass, complex conjugate poles.

It can also be shown that the low-pass to bandpass transformation takes each zero at infinity and transforms to a zero at the origin and a zero at infinity. After the low-pass to bandpass transformation is applied to N-th order low-pass filter, there will be N complex conjugate poles, N zeros at the origin, and N zeros at infinity. We can group the poles and zeros into second-order products having the following form

$$T_k(s_{bn}) = \frac{K_k s_{bn}}{(s_{bn} + p_{kbn})(s_{bn} + p^*_{jbn})} = \frac{K_k s_{bn}}{(s_{bn}+\sigma_{kbn}+j\omega_{kbn})(s_{bn}+\sigma_{kbn}-j\omega_{kbn})}$$

$$= \frac{K_k s_{bn}}{s^2_{bn}+(2\sigma_{kbn})s_{bn}+(\sigma^2_{bn}+\omega^2_{kbn})} = \frac{T_k(\omega_{kon})\left(\frac{\omega_{kon}}{Q_k}\right)s_{bn}}{s^2_{bn} + \left(\frac{\omega_{kon}}{Q_k}\right)s_{bn} + \omega^2_{kon}} \tag{39}$$

where j and k corresponds to the jth and kth low-pass poles which are a complex conjugate pair, K_k is a gain constant, and

$$\omega_{kon} = \sqrt{\sigma^2_{kbn}+\omega^2_{kbn}} \tag{40}$$

and

$$Q_k = \frac{\sqrt{\sigma_{bn}^2 + \omega_{kbn}^2}}{2\sigma_{bn}} \quad . \tag{41}$$

Normally, the gain of $T_k(\omega_{kon})$ is unity.

The order of the bandpass filter is determined by translating its specifications to an equivalent low-pass filter. The ratio of the stop bandwidth to the pass bandwidth for the bandpass filter is defined as

$$\Omega_n = \frac{SW}{BW} = \frac{\omega_{SB2} - \omega_{SB1}}{\omega_{BP2} - \omega_{PB1}}. \tag{42}$$

We will not illustrate bandstop filters but the procedure is to first apply the high pass transformation to the low pass normalized roots followed by the bandpass transformation. The references will provide further information on the cascade filter design approach.

Higher Order Filters - Ladder Approach

The second major approach to designing higher-order, switched capacitor circuits shown in Fig. 9.7-6 is called the ladder approach. It has the advantage of being less sensitive to the capacitor ratios than the cascade approach. Its disadvantage is that the design approach is slightly more complex and is only applicable to filters that can be expressed as *RLC* circuits. The ladder approach begins with the normalized, low pass, *RLC* prototype filter structure. Next, state equations are written based on the *RLC* prototype circuit. Lastly, the state equations are synthesized using the appropriate switched capacitor circuits. For low pass filters, these circuits are the integrators of Sec. 9.3.

RLC, low-pass ladder filters are the result of network synthesis and are based on techniques well known in circuit theory [25]. The resulting realizations of these synthesis techniques always start with a load resistor of 1 ohm and work toward the input of the filter. Fig. 9.7-12 shows the form for a singly-terminated *RLC* filter for the case of even and odd order functions with the numbering of components going from the output to the input of the filter. The *RLC* ladder filters of Fig. 9.7-12 are normalized to a passband of 1

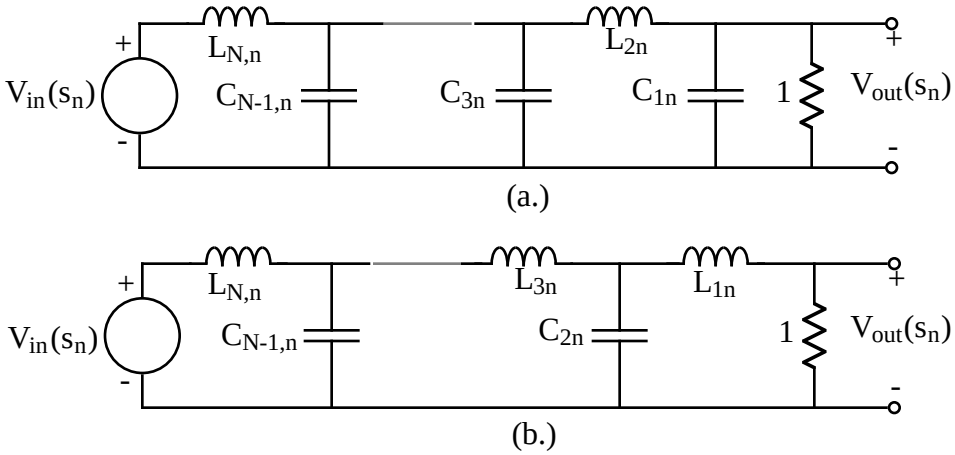


Figure 9.7-12 - Singly-terminated, *RLC* filters. (a.) *N* even. (b.) *N* odd.

rps and an impedance of 1Ω. The denormalizations of Table 9.7-3 are applicable to the elements of Fig. 9.7-12.

Table 9.7-3 - Nomalized component values for Fig. 9.7-12 for the Butterworth and Chebyshev singly-terminated, *RLC* filter approximations.

	Use these component designations for even order circuits of Fig. 9.7-12a.									
N	C_{1n}	L_{2n}	C_{3n}	L_{4n}	C_{5n}	L_{6n}	C_{7n}	L_{8n}	C_{9n}	L_{10n}
2	0.7071	1.4142								
3	0.5000	1.3333	1.5000			Butterworth (1 rps passband)				
4	0.3827	1.0824	1.5772	1.5307						
5	0.3090	0.8944	1.3820	1.6944	1.5451					
6	0.2588	0.7579	1.2016	1.5529	1.7593	1.5529				
7	0.2225	0.6560	1.0550	1.3972	1.6588	1.7988	1.5576			
8	0.1951	0.5576	0.9370	1.2588	1.5283	1.7287	1.8246	1.5607		
9	0.1736	0.5155	0.8414	1.1408	1.4037	1.6202	1.7772	1.8424	1.5628	
10	0.1564	0.4654	0.7626	1.0406	1.2921	1.5100	1.6869	1.8121	1.8552	1.5643
2	0.9110	0.9957								
3	1.0118	1.3332	1.5088		1-dB ripple Chebyshev (1 rps passband)					
4	1.0495	1.4126	1.9093	1.2817						
5	1.0674	1.4441	1.9938	1.5908	1.6652					
6	1.0773	1.4601	2.0270	1.6507	2.0491	1.3457				
7	1.0832	1.4694	2.0437	1.6736	2.1192	1.6489	1.7118			
8	1.0872	1.4751	2.0537	1.6850	2.1453	1.7021	2.0922	1.3691		
9	1.0899	1.4790	2.0601	1.6918	2.1583	1.7213	2.1574	1.6707	1.7317	
10	1.0918	1.4817	2.0645	1.6961	2.1658	1.7306	2.1803	1.7215	2.1111	1.3801
	L_{1n}	C_{2n}	L_{3n}	C_{4n}	L_{5n}	C_{6n}	L_{7n}	C_{8n}	L_{9n}	C_{10n}
	Use these component designations for odd order circuits of Fig. 9.7-12b.									

Example 9.7-6

Use of the Table 9.7-3 to Find a Singly-Terminated, *RLC* Low pass Filter

Find a singly-terminated, normalized, *RLC* filter for a 4th-order Butterworth low pass filter approximation.

Solution

Use Table 9.7-3 with the component designations at the top to get Fig. 9.7-13.

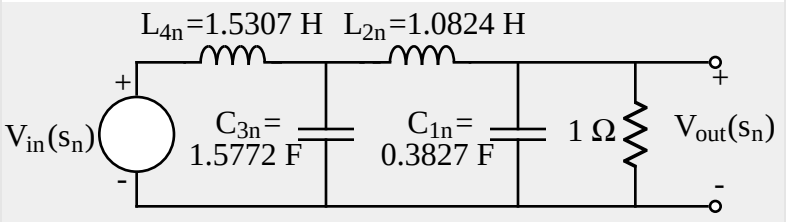


Figure 9.7-13 - Realization for Ex. 9.7-6.

Fig. 9.7-14 shows the normalized ladder filters for doubly-terminated, *RLC* filters. These filters are similar to those of Fig. 9.7-12 except for a series source resistance. Table 9.7-4 gives the normalized component values for the doubly-terminated *RLC* circuits of Fig. 9.7-13 for the Butterworth and 1-*dB* Chebyshev approximations.

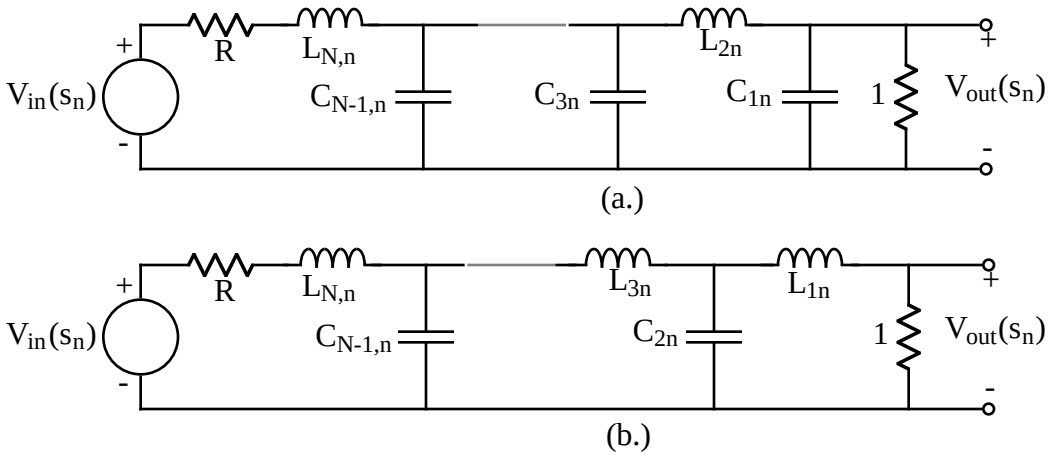


Figure 9.7-14 - Doubly-terminated, *RLC* filters. (a.) *N* even. (b.) *N* odd.

Table 9.7-4 - Normalized component values for Fig. 9.7-14 for the Butterworth and 1-*dB* Chebyshev doubly-terminated *RLC* approximations.

	Use these component designations for even order of Fig. 9.7-14a, R = 1Ω.									
N	C_{1n}	L_{2n}	C_{3n}	L_{4n}	C_{5n}	L_{6n}	C_{7n}	L_{8n}	C_{9n}	L_{10n}
2	1.4142	1.4142								
3	1.0000	2.0000	1.0000			Butterworth (1 rps passband)				
4	0.7654	1.8478	1.8478	0.7654						
5	0.6180	1.6180	2.0000	1.6180	0.6180					
6	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176				
7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2740	0.4450			
8	0.3902	1.1111	1.6629	1.9616	1.9616	1.6629	1.1111	0.3902		
9	0.3473	1.0000	1.5321	1.8794	2.0000	1.8794	1.5321	1.0000	0.3473	
10	0.3129	0.9080	1.4142	1.7820	1.9754	1.9754	1.7820	1.4142	0.9080	0.3129
3	2.0236	0.9941	2.0236		1-dB ripple Chebyshev (1 rps passband)					
5	2.1349	1.0911	3.0009	1.0911	2.1349					
7	2.1666	1.1115	3.0936	1.1735	3.0936	1.1115	2.1666			
9	2.1797	1.1192	3.1214	1.1897	3.1746	1.1897	3.1214	1.1192	2.1797	
	L_{1n}	C_{2n}	L_{3n}	C_{4n}	L_{5n}	C_{6n}	L_{7n}	C_{8n}	L_{9n}	C_{10n}
	Use these component designations for odd order of Fig. 9.7-14b, R = 1Ω.									

The tabular information for the design of *RLC* filters consists of the normalized component values of Figs. 9.7-12 and 9.7-14. Each of the many different types of filter approximations have been tabulated for values of *N* up to 10 or more[24].

Note that no solution exists for the even-order cases of the doubly-terminated, *RLC* Chebyshev approximations for $R = 1\ \Omega$. This is a special result for $R = 1\ \Omega$ and is

not true for other values of *R*. Also, the gain in the passband will be no more than -6 *dB* because of the equal source and load resistances causing an gain of 0.5 at low frequencies where the inductors are short-circuits and the capacitors are open-circuits.

Example 9.7-7

Use of Table 3-2 to Find a Doubly-Terminated, RLC Low-pass Filter

Find a doubly-terminated, RLC filter using minimum capacitors for a fifth-order Chebyshev filter approximation having 1 dB ripple in the passband and a source resistance of 1 Ω.

Solution

Using Table 9.7-4 and using the component designations at the top of the table gives Fig. 9.7-15.

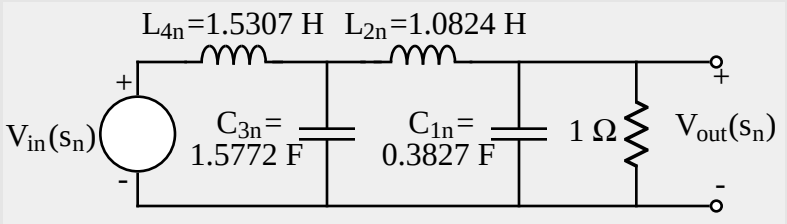


Figure 9.7-15 - Fifth-order, doubly-terminated, normalized, Chebyshev low-pass *RLC* filter realization.

The next step in the design of ladder filters is to show how to use active elements and resistors and capacitors to realize a low-pass ladder filter. Let us demonstrate the approach by using an example. Consider the doubly-terminated, fifth-order, *RLC*, low-pass ladder filter of Fig. 9.7-16. Note that we have reordered the numbering of the components to start with the source and proceed to the load. We are also dropping the "*l*" from the component subscripts because we will only be dealing with low-pass structures in this discussion.

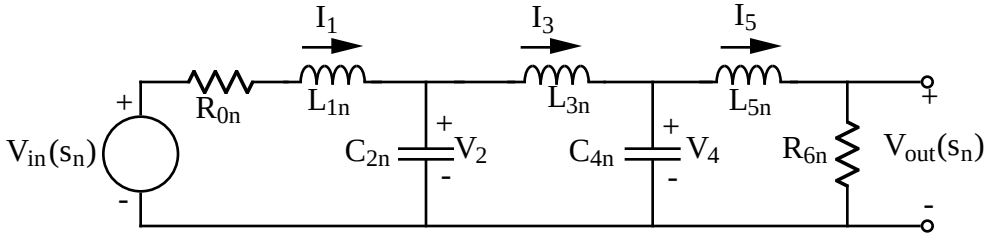


Figure 9.7-16 - A fifth-order, low-pass, normalized RLC ladder filter.

The first step in realizing the *RLC* filter of Fig. 9.7-16 by switched capacitor circuits is to assign a current I_j to every *j*-th series element (or combination of elements in series) of the ladder filter and a voltage V_k to every *k*-th shunt element (or combination of elements in shunt) ofthe ladder filter. These currents and voltages for the example of Fig. 9.7-16 are shown on the figure. These variables are called *state variables*.

The next step is to alternatively use loop (*KVL*) and node (*KCL*) equations expressed in terms of the state variables only. For example, we begin at the source of Fig. 9.7-16 and write the loop equation

$$V_{in}(s) - I_1(s)R_{0n} - sL_{1n}I_1(s) - V_2(s) = 0 \quad . \tag{43}$$

Next, we write the nodal equation

$$I_1(s) - sC_{2n}V_2(s) - I_3(s) = 0 \quad . \tag{44}$$

We continue in this manner to get the following state equations.

$$V_2(s) - sL_{3n}I_3(s) - V_4(s) = 0 \tag{45}$$

$$I_3(s) - sC_{4n}V_4(s) - I_5(s) = 0 \tag{46}$$

and

$$V_4(s) - sL_{5n}I_5(s) - R_{6n}I_{5n}(s) = 0 \tag{47}$$

Eqs. (43) through (47) constitute the state equations which completely describe the ladder filter of Fig. 9.7-16. A supplementary equation of interest is

$$V_{out}(s) = I_5(s)R_{6n} \quad . \tag{48}$$

Once, the state equations for a ladder filter are written, then we define a *voltage analog, V_j' of current I_j* as

$$V_j' = R'I_j \tag{49}$$

where R' is an arbitrary resistance (normally 1 ohm). The voltage analog concept allows us to convert from impedance and admittance functions to voltage transfer functions which is a useful step in the implementation of the ladder filter. Now if for every current in the state equations of Eq. (43) through Eq. (47) we replace currents I_1, I_3, and I_5 by their voltage analogs, we get the following modified set of state equations.

$$V_{in}(s) - \left(\frac{V_1'(s)}{R'}\right)(R_{0n} + sL_{1n}) - V_2(s) = 0 \tag{50}$$

$$\left(\frac{V_1'(s)}{R'}\right) - sC_{2n}V_2(s) - \left(\frac{V_3'(s)}{R'}\right) = 0 \tag{51}$$

$$V_2(s) - sL_{3n}\left(\frac{V_3'(s)}{R'}\right) - V_4(s) = 0 \tag{52}$$

$$\left(\frac{V_3'(s)}{R'}\right) - sC_{4n}V_4(s) - \left(\frac{V_5'(s)}{R'}\right) = 0 \tag{53}$$

and

$$V_4(s) - \left(\frac{V_5'(s)}{R'}\right)(sL_{5n} + R_{6n}) = 0 \tag{54}$$

The next step is to use the 5 equations of Eqs. (50) through (54) to solve for each of the state variables. The result is

$$V_1'(s) = \frac{R'}{sL_{1n}}\left[V_{in}(s) - V_2(s) - \left(\frac{R_{0n}}{R'}\right)V_1'(s)\right] \tag{55}$$

$$V_2(s) = \frac{1}{sR'C_{2n}}\,[V_1'(s) - V_3'(s)] \tag{56}$$

$$V_3'(s) = \frac{R'}{sL_{3n}}\,[V_2(s) - V_4(s)] \tag{57}$$

$$V_4(s) = \frac{1}{sR'C_{4n}}\,[V_3'(s) - V_5'(s)] \tag{58}$$

and

$$V_5'(s) = \frac{R'}{sL_{5n}}\,[V_4(s) - \frac{R_{6n}}{R'}V_5'(s)]\,. \tag{59}$$

However, we would prefer to have the variable $V_{out}(s)$ used in place of $V_5'(s)$. From Eq. (48) we get

$$V_{out}(s) = \left(\frac{R_{6n}}{R'}\right)V_5'(s) \quad . \tag{60}$$

Combining Eqs. (58) and (59) with (60) gives

$$V_4(s) = \frac{1}{sR'C_{4n}}\,[V_3'(s) - \left(\frac{R'}{R_{6n}}\right)V_{out}(s)] \tag{61}$$

$$V_{out}(s) = \frac{R_{6n}}{sL_{5n}}\,[V_4(s) - V_{out}(s)]\,. \tag{62}$$

The next step is to synthesize each of the Eqs. (55), (56), (57), (61) and (62) using the appropriate switched capacitor integrator of Sec. 9.3. The final step is to connect the integrators together as indicated to achieve the switched capacitor realization of the low pass filter. The general procedure for the design of a low pass, switched capacitor filter using the ladder approach is outlined below.

1.) From T_{PB}, T_{SB}, and Ω_n (or A_{PB}, A_{SB}, and Ω_n) determine the reuired order of the filter approximation using Eq. (7) or Eq. (12).

2.) From tables similar to Table 9.7-3 and 9.7-2 find the *RLC* prototype filter approximation.

3.) Write the state equations and rearrange them so each state variable is equal to the integrator of various inputs.

4.) Realize each of rearranged state equations by the switched capacitor integrators of Secs. 9.3.

The following example will illustrate this part of the design procedure.

Example 9.7-8

Fifth-order, Low Pass, Switched Capacitor Filter using the Ladder Approach

Design a ladder, switched capacitor realization for a Chebyshev filter approximation to the filter specifications of T_{PR} = -1dB, T_{SR} = -25dB, f_{PR} = 1kHz and f_{SR} = 1.5 kHz. Give a schematic and component value for the realization. Also simulate the realization and compare to an ideal realization. Use a clock frequency of 20 kHz. Adjust your design so that it does not suffer the -6dB loss in the pass band. (Note that this example should be identical with Ex. 9.7-5.)

Solution

From Ex. 9.7-5, we know that a 5th-order, Chebyshev approximation will satisfy the specification. The corresponding low pass, *RLC* prototype filter is given in Fig. 9.7-15. Next, we must find the state equations and express them in the form of an integrator. Fortunately, we can use the above that results in Eqs. (55), (56), (57), (61) and (62) as the desired relationships. Next, use the switched-capacitor integrators of Sec. 9.3 to realize each of these five equations.

Eq. (55) - L_{1n}

Eq. (55) can be realized by the switched capacitor integrator of Fig. 9.7-17 which has one noninverting input and two inverting inputs. Using the results of Eqs. (16) and (24) of Sec. 9.3, we can write that

$$V_1'(z) = \frac{1}{z\text{-}1}\left[\alpha_{11}V_{in}(z) - \alpha_{21}zV_2(z) - \alpha_{31}zV_1'(z)\right]. \qquad (63)$$

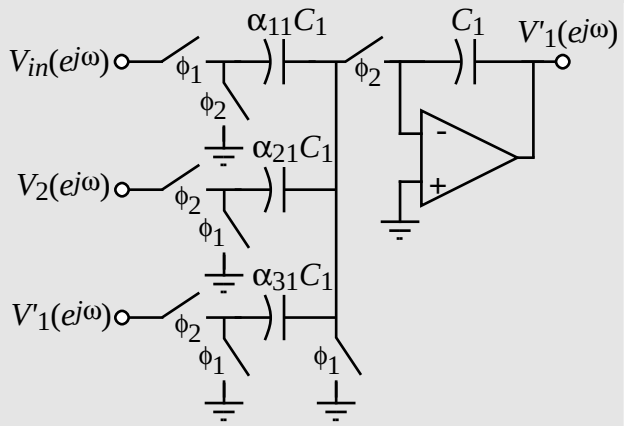


Figure 9.7-17 - Realization of Eq. (55).

However, since $f_{PR} < f_c$, we can replace z by 1 and z-1 by sT. Further, let us use the normalization of Eq. (16) to get

$$V_1'(s_n) \approx \frac{1}{s_nT_n}\left[\alpha_{11}V_{in}(s) - \alpha_{21}V_2(s) - \alpha_{31}V_1'(s)\right]. \qquad (64)$$

Equating Eq. (64) to Eq. (55) gives the design of the capacitor ratios for the first integrator as

$$\alpha_{11} = \alpha_{21} = \frac{R'T_n}{L_{1n}} = \frac{R'\omega_{PB}}{f_c L_{1n}} = \frac{1 \cdot 2000\pi}{20{,}000 \cdot 2.1349} = 0.1472$$

and

$$\alpha_{31} = \frac{R_{0n}T_n}{L_{1n}} = \frac{R_{0n}\omega_{PB}}{f_c L_{1n}} = \frac{1 \cdot 2000\pi}{20{,}000 \cdot 2.1349} = 0.1472$$

assuming that $R_{0n} = R' = 1\Omega$. In the actual realization, we will double the value of α_{11} ($\alpha_{11} = 0.2943$) in order to gain 6*dB* and remove the -6*dB* of the *RLC* prototype. The total capacitance of the first integrator is

$$\text{First integrator capacitance} = 2 + \frac{2(0.2943)}{0.1472} + \frac{1}{0.1472} = 10.79 \text{ units of capacitance.}$$

Eq. (56) - C_{2n}

Eq. (56) can be realized by the switched capacitor integrator of Fig. 9.7-18 which has one noninverting input and one inverting input. As before we write that

$$V_2(z) = \frac{1}{z\text{-}1}\left[\alpha_{12}V_1'(z) - \alpha_{22}zV_3'(z)\right]. \tag{65}$$

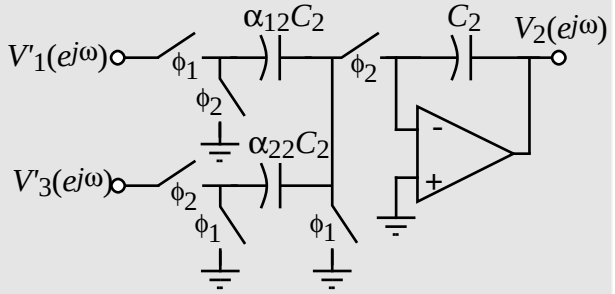


Figure 9.7-18 - Realization of Eq. (56).

Simplifying as above gives

$$V_2(s_n) \approx \frac{1}{s_n T_n}\left[\alpha_{12}V_1'(s_n) - \alpha_{22}V_3'(s_n)\right]. \tag{66}$$

Equating Eq. (66) to Eq. (56) yields the design of the capacitor ratios for the second integrator as

$$\alpha_{12} = \alpha_{22} = \frac{T_n}{R'C_{2n}} = \frac{\omega_{PB}}{R'f_c C_{2n}} = \frac{2000\pi}{1 \cdot 20{,}000 \cdot 1.0911} = 0.2879.$$

The second integrator has a total capacitance of

$$\text{Second integrator capacitance} = \frac{1}{0.2879} + 2 = 5.47 \text{ units of capacitance.}$$

Eq. (57) - L_{3n}

Eq. (57) can be realized by the switched capacitor integrator of Fig. 9.7-19 which has one noninverting input and one inverting input. For this circuit we get

$$V_3'(z) = \frac{1}{z-1}[\alpha_{13}V_2(z) - \alpha_{23}zV_4(z)]. \quad (67)$$

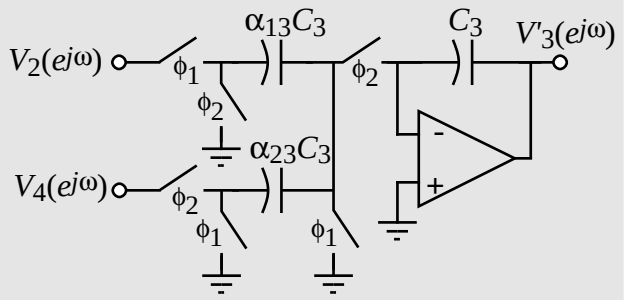


Figure 9.7-19 - Realization of Eq. (57).

Simplifying as above gives

$$V_3'(s_n) \approx \frac{1}{s_n T_n}[\alpha_{13}V_2(s_n) - \alpha_{23}V_4(s_n)]. \quad (68)$$

Equating Eq. (68) to Eq. (57) yields the capacitor ratios for the third integrator as

$$\alpha_{13} = \alpha_{23} = \frac{R'T_n}{L_{3n}} = \frac{R'\omega_{PB}}{f_c L_{3n}} = \frac{1 \cdot 2000\pi}{20{,}000 \cdot 3.0009} = 0.1047.$$

The third integrator has a total capacitance of

$$\text{Third integrator capacitance} = \frac{1}{0.1047} + 2 = 11.55 \text{ units of capacitance}$$

Eq. (61) - C_{4n}

Eq. (61) can be realized by the switched capacitor integrator of Fig. 9.7-20 with one noninverting and one inverting input. As before we write that

$$V_4(z) = \frac{1}{z-1}\left[\alpha_{14}V_3'(z) - \alpha_{24}zV_{out}(z)\right]. \quad (69)$$

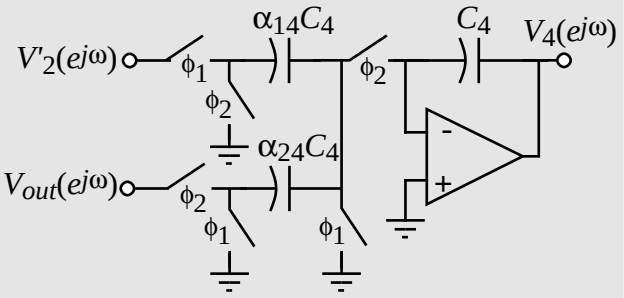


Figure 9.7-20 - Realization of Eq. (61).

Assuming that $f_{PB} < f_c$ gives

$$V_4(s_n) \approx \frac{1}{s_n T_n}\left[\alpha_{14} V_3'(s_n) - \alpha_{24} V_{out}(s_n)\right]. \qquad (70)$$

Equating Eq. (70) to Eq. (61) yields the design of the capacitor ratios for the fourth integrator as

$$\alpha_{14} = \alpha_{24} = \frac{T_n}{R'C_{4n}} = \frac{\omega_{PB}}{R'f_c C_{4n}} = \frac{2000\pi}{1 \cdot 20{,}000 \cdot 1.0911} = 0.2879.$$

if $R' = R_{0n}$. In this case, we note that fourth integrator is identical to the second integrator with the same total integrator capacitance.

Eq. (62) - L_{5n}

The last state equation, Eq. (62), can be realized by the switched capacitor integrator of Fig. 9.7-21 which has one noninverting input and one inverting input. For this circuit we get

$$V_{out}(z) = \frac{1}{z-1}\left[\alpha_{15} V_4(z) - \alpha_{25} z V_{out}(z)\right]. \qquad (71)$$

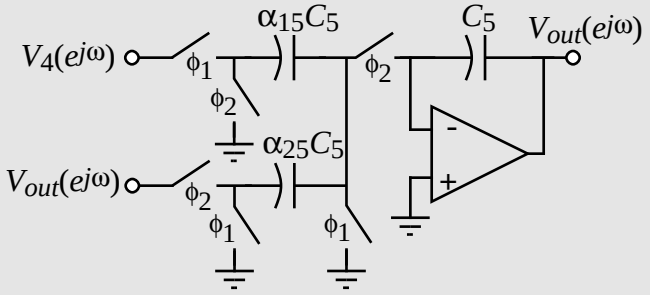


Figure 9.7-21 - Realization of Eq. (62).

Simplifying as before gives

$$V_{out}(s_n) \approx \frac{1}{s_n T_n}\left[\alpha_{15} V_4(s_n) - \alpha_{25} V_{out}(s_n)\right]. \qquad (72)$$

Equating Eq. (72) to Eq. (62) yields the capacitor ratios for the fifth integrator as

$$\alpha_{15} = \alpha_{25} = \frac{R_{6n} T_n}{L_{3n}} = \frac{R_{6n}\omega_{PB}}{f_c L_{3n}} = \frac{1 \cdot 2000\pi}{20{,}000 \cdot 2.1349} = 0.1472$$

where $R_{6n} = 1\Omega$.

The total capacitance of the fifth integrator is

$$\text{Fifth integrator capacitance} = \frac{1}{0.1472} + 2 = 8.79 \text{ units of capacitance}$$

We see that the total capacitance of this filter is 10.79 + 5.47 + 11.53 + 5.47 + 8.79 = 42.05. We note that Ex. 9.7-5 which used the cascade approach for the same specification required 36.72 units of capacitance.

The overall realization of this filter is shown in Fig. 9.7-22. Fig. 9.7-23 shows the simulated and ideal filter responses for this example. Fig. 9.7-24 shows the magnitude and phase of the output voltage of each of the five op amps in the filter realization. We see that some of the op amps are exceeding a gain of 0dB and that voltage scaling should be applied to those op amps to achieve maximum dynamic range.

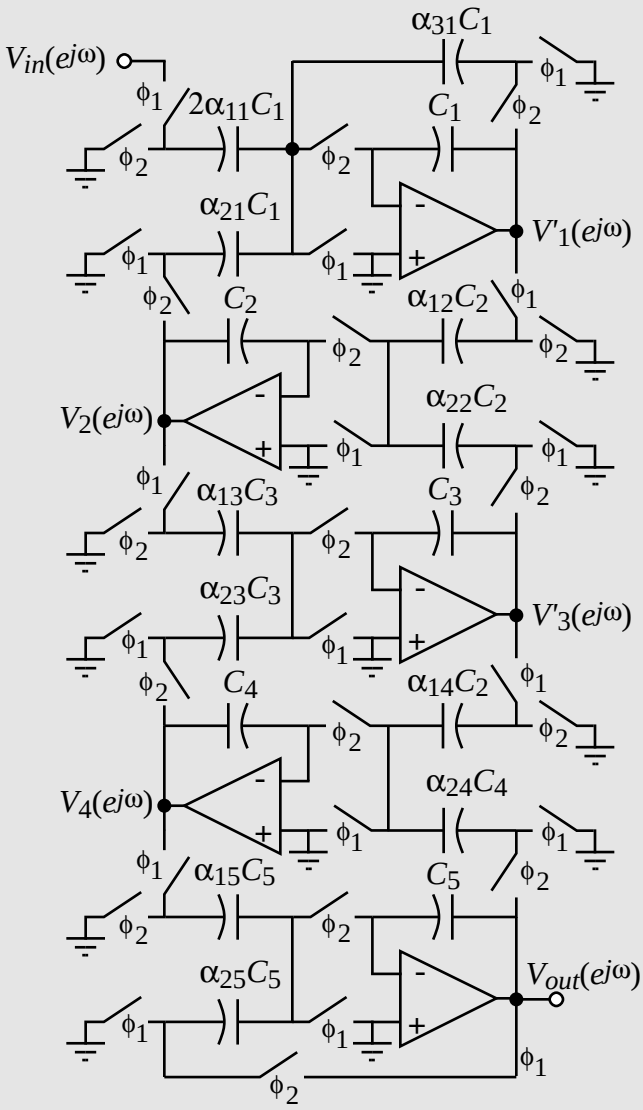
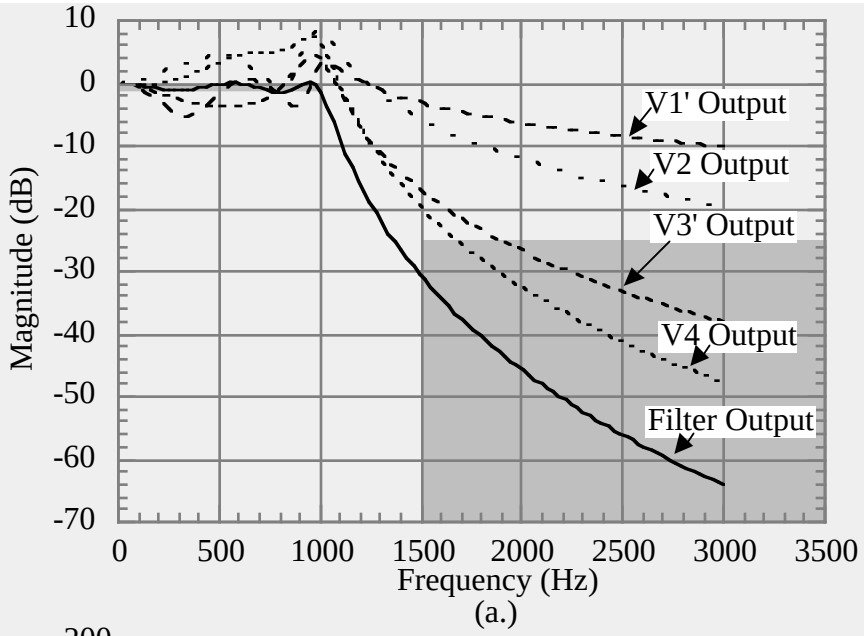
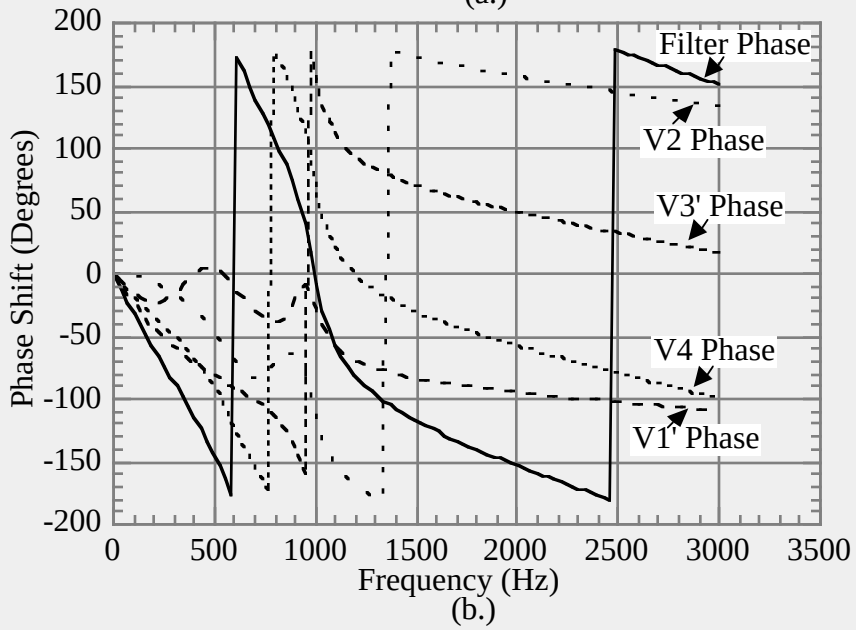


Figure 9.7-22 - Fifth-order, Chebyshev, low pass switched capacitor filter of Example 9.7-8.



(a.)



(b.)

Figure 9.7-23 - (a.) Simulated magnitude and (b.) phase response of Ex. 9.7-8.

```
*******   08/29/97   13:12:51   ******
******PSpice 5.2 (Jul 1992) ********

****     CIRCUIT DESCRIPTION ****

*SPICE FILE FOR EXAMPLE 9.7_5
*Example 9.7-8 : ladder filter
*Node 5 is the output at V1'
*Node 7 is the output at V2
*Node 9 is the output of V3'
*Node 11 is the output of V4
*Node 15 is the final output
VIN    1 0 DC 0 AC 1
```

```
**************************
* V1' STAGE
XNC11    1 2 3 4 NC11
XPC11    7 8 3 4 PC1
XPC12    5 6 3 4 PC1
XUSC1    5 6 3 4 USCP
XAMP1    3 4 5 6 AMP
**************************
*V4 STAGE
XNC41    9 10 25 26 NC2
XPC41    15 16 25 26 PC2
XUSC4    11 12 25 26 USCP
XAMP4    25 26 11 12 AMP
```

```
**************************
*V2 STAGE
XNC21    5 6 19 20 NC2
XPC21    9 10 19 20 PC2
XUSC2    7 8 19 20 USCP
XAMP2    19 20 7 8 AMP
**************************
*V3' STAGE
XNC31    7 8 13 14 NC3
XPC31    11 12 13 14 PC3
XUSC3    9 10 13 14 USCP
XAMP3    13 14 9 10 AMP
**************************
*VOUT STAGE
XNC51    11 12 17 18 NC1
XPC51    15 16 17 18 PC1
XUSC5    15 16 17 18 USCP
XAMP5    17 18 15 16 AMP
**************************

.SUBCKT DELAY 1 2 3
ED    4 0 1 2 1
TD    4 0 3 0 ZO=1K TD=25US
RDO    3 0 1K
.ENDS DELAY

.SUBCKT NC1 1 2 3 4
RNC1    1 0 6.7934
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 .1472
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 .1472
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 .1472
RNC2    4 0 6.7934
.ENDS NC1

.SUBCKT NC11 1 2 3 4
RNC1    1 0 3.3978XNC1    1 0 10 DELAY
GNC1    1 0 10 0 .2943
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 .2943
XNC3     4 0 40 DELAYGNC3     4 0 40 0
.2943
RNC2    4 0 3.3978
.ENDS NC11
.
SUBCKT NC2 1 2 3 4
RNC1    1 0 3.4730
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 .2879
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.2879
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.2879
RNC2    4 0 3.4730
.ENDS NC2

.SUBCKT NC3 1 2 3 4
RNC1    1 0 9.5521
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 0.1047
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.1047
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.1047
RNC2    4 0 9.5521
.ENDS NC3

.SUBCKT NC4 1 2 3 4
RNC1    1 0 3.4730
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 .2879
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 .2879
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 .1472
RNC2    4 0 6.7955
.ENDS NC4

.SUBCKT PC1 1 2 3 4
RPC1    2 4 6.7934
.ENDS PC1

.SUBCKT PC2 1 2 3 4
RPC1    2 4 3.4730
.ENDS PC2

.SUBCKT PC3 1 2 3 4
RPC1    2 4 9.5521
.ENDS PC3

.AC LIN 100 10 3K
.PRINT AC V(5) VP(5) V(7)
+ VP(7) V(9) VP(9) V(11)
+ VP(11) V(15) VP(15)
.PROBE
.END
```

Figure 9.7-24 - SPICE input file for the simulation of Fig. 9.7-23.

Example 9.7-8 illustrates the ladder design procedure for low pass filters. This procedure is easily adaptable to filters with jω axis zeros. *RLC* filters with jω axis zeros have and *LC* in the shunt brand or a parallel *LC* in the series branch of the *RLC* prototype. Such circuits either have *inductor-cutsets* or *capacitor-loops*. An equivalent circuit can be developed which removes the inductor-cutsets or capacitor-loops using dependent sources. The dependent sources are easily realized using an unswitched capacitor applied to the integrator summing node [19].

The ladder design approach can be used for high pass, bandpass, and bandstop filters. The method is straightforward and is based on the frequency transformation of the low pass prototype *RLC* circuit. We will briefly describe the approach for the high pass and bandpass ladder filters.

The frequency transformation from the normalized, low-pass to normalized high-pass was given by Eq. (24). If we apply this transformation to an inductor of a normalized, low-pass realization, we obtain

$$s_{ln}L_{ln} = \left(\frac{1}{s_{hn}}\right) L_{ln} = \frac{1}{s_{hn}C_{hn}} \quad . \tag{73}$$

Similarly, if applying the transformation to a capacitor, C_{ln}, of a normalized, low-pass realization, we obtain

$$\frac{1}{s_{ln}C_{ln}} = \left(\frac{s_{hn}}{1}\right)\frac{1}{C_{ln}} = s_{hn}L_{hn} \, . \tag{74}$$

From Eqs. (73) and (74), we see that the normalized, low-pass to normalized, high-pass frequency transformation takes an inductor, L_{ln}, and replaces it by a capacitor, C_{hn}, whose value is $1/L_{ln}$. This transformation also takes a capacitor, C_{ln}, and replaces it by an inductor, L_{hn}, whose value is $1/C_{ln}$. Fig. 9.7-25 illustrates these important relationships.

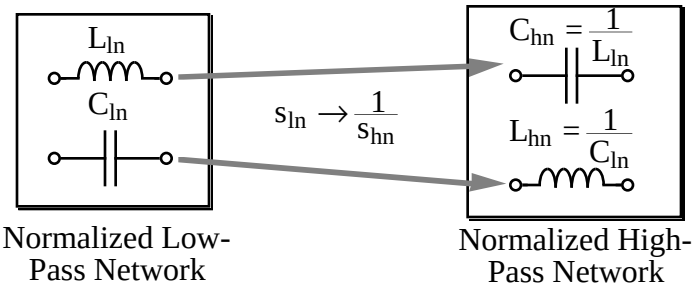


Figure 9.7-25 - Influence of the normalized, low-pass to normalized, high-pass frequency transformation on the inductors and capacitors.

From the above results, we see that to achieve a normalized, high-pass *RLC* filter, we replace each inductor, L_{ln}, with a capacitor, C_{hn}, whose value is $1/L_{ln}$ and each capacitor, C_{ln}, with an inductor, L_{hn}, whose value is $1/C_{ln}$. Next, the state equations are written and converted to the form where each state variable is expressed as the derviative of various inputs. A realization of the derivative circuit is shown in Fig. 9.7-26. Alternately, one can rewrite the high pass state equations in terms of integrators although the procedure for doing this requires cleverness in formulating the equations.

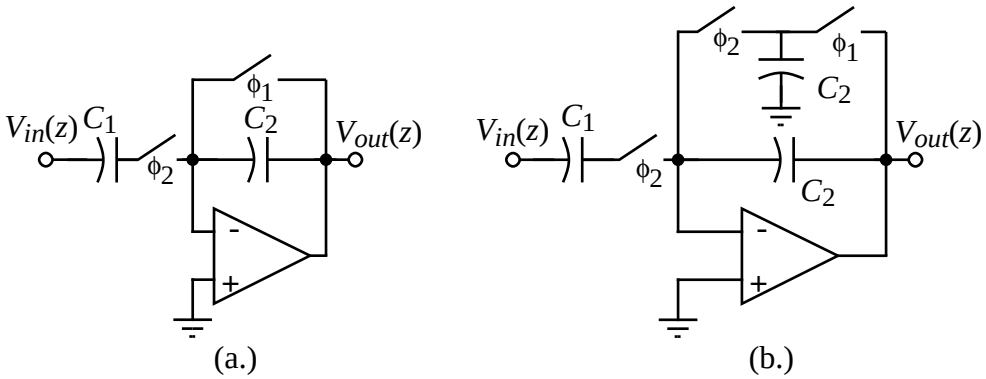


Figure 9.7-26 - (a.) Switched capacitor differentiator circuit. (b.) Modification to keep op amp output from being discharged to ground during ϕ_1.

The design of *RLC* bandpass ladder filters starts with the normalized low pass filter and uses the normalized bandpass transformation of Eq. (32) to obtain a bandpass, normalized *RLC* filter. This transformation will be applied to the inductors and capacitors of the low pass circuit as follows.

Consider first the inductor, L_{ln}, of a normalized, low pass filter. Let us simultaneously apply the bandpass normalization and the frequency transformation by using Eq. (32). The normalized, inductance L_{ln} can be expressed as

$$s_{ln}L_{ln} = \left[\left(\frac{\omega_r}{BW}\right)\left(s_{bn}+\frac{1}{s_{bn}}\right)\right]L_{ln} = s_{bn}\left(\frac{\omega_r L_{ln}}{BW}\right)+\frac{1}{s_{bn}}\left(\frac{\omega_r L_{ln}}{BW}\right) = s_{bn}L_{bn}+\frac{1}{s_{bn}C_{bn}}. \quad (75)$$

Thus we see that the bandpass normalization and frequency transformation takes an inductance, L_{ln}, and replaces it by an inductor, L_{bn}, in series with a capacitor, C_{bn}, whose values are given as

$$L_{bn} = \left(\frac{\omega_r}{BW}\right)L_{ln} = \frac{L_{ln}}{\Omega_b} \quad (76)$$

and

$$C_{bn} = \left(\frac{BW}{\omega_r}\right)\frac{1}{L_{ln}} = \frac{\Omega_b}{L_{ln}}. \quad (77)$$

Now we apply Eq. (32) to a normalized capacitance, C_{ln}, to get

$$\frac{1}{s_{ln}C_{ln}} = \frac{1}{\left[\left(\frac{\omega_r}{BW}\right)\left(s_{bn}+\frac{1}{s_{bn}}\right)\right]C_{ln}} = \frac{1}{s_{bn}\left(\frac{\omega_r}{BW}\right)C_{ln}+\frac{1}{s_{bn}}\left(\frac{\omega_r C_{ln}}{BW}\right)}$$

$$= \frac{1}{s_{bn}C_{bn}+\frac{1}{s_{bn}L_{bn}}} \quad . \quad (78)$$

From Eq. (78), we see that the bandpass normalization and frequency transformation takes a capacitor, C_{ln}, in a low-pass circuit and transfors to a capacitor, C_{bn}, in parallel with an inductor, L_{bn}, whose values are given as

$$C_{bn} = \left(\frac{\omega_r}{BW}\right) C_{ln} = \frac{C_{ln}}{\Omega_b} \tag{79}$$

and

$$L_{bn} = \left(\frac{BW}{\omega_r}\right) \frac{1}{C_{ln}} = \frac{\Omega_b}{C_{ln}} \quad . \tag{80}$$

Eqs. (76), (77), (79), and (80) are very important in the design of RLC bandpass filters and are illustrated in Fig. 9.7-27.

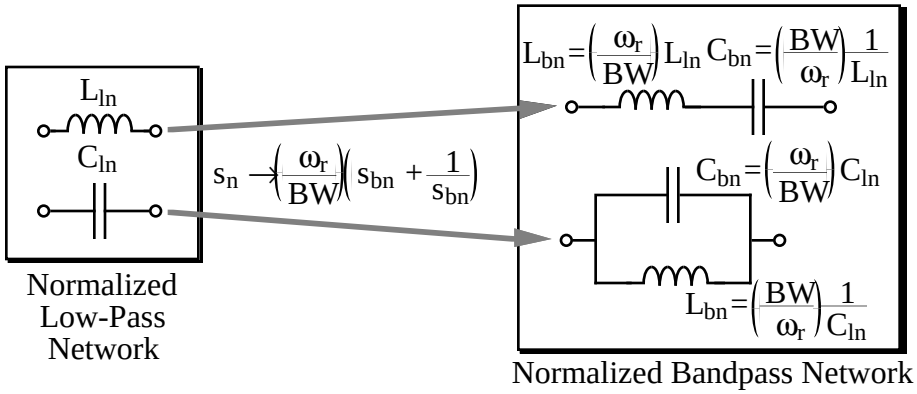
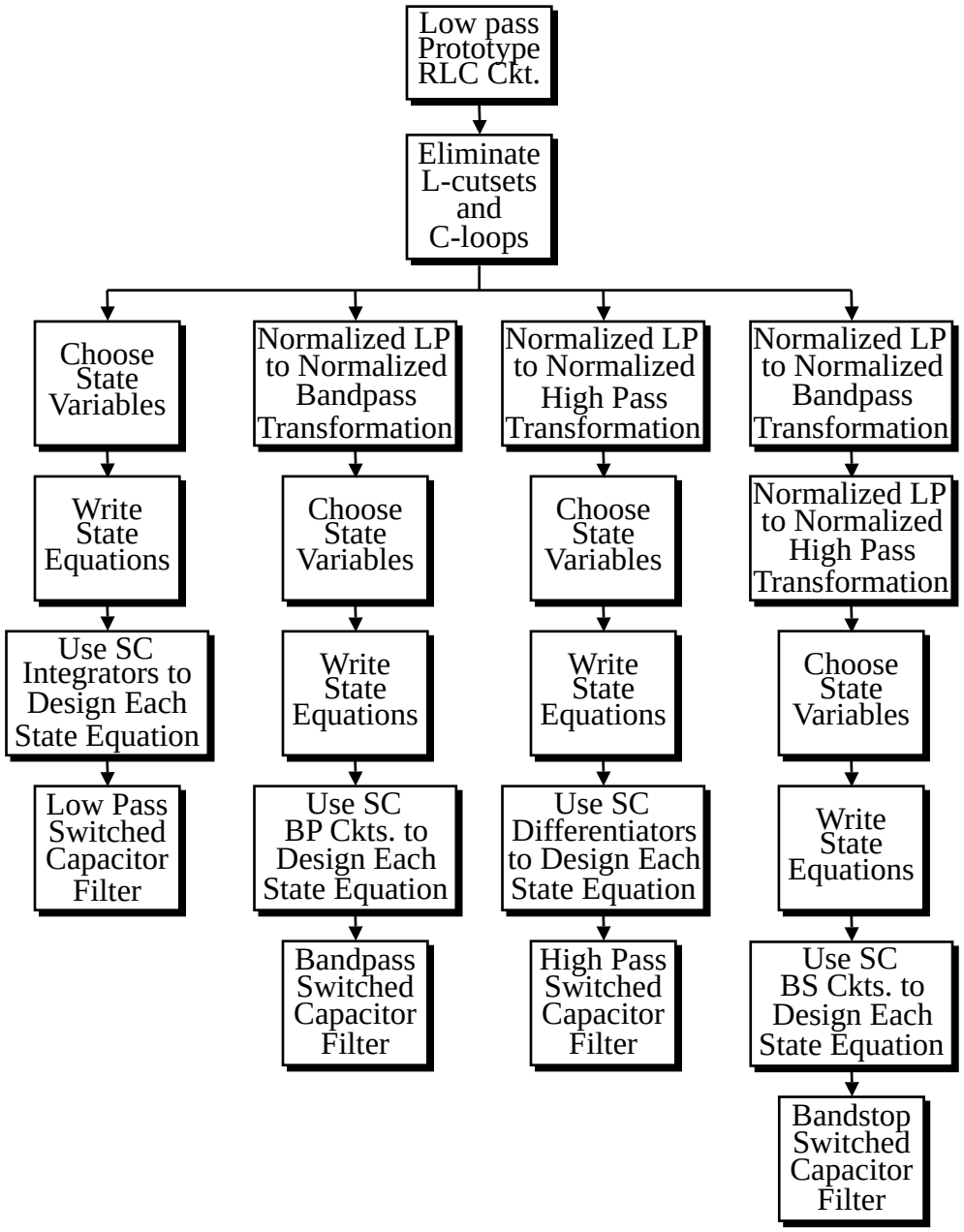


Figure 9.7-27 - Illustration of the influence of the normalized, low-pass to the normalized, bandpass transformation of Eq. (32) on an inductor and capacitor of a low-pass filter.

When the state equations are written for the normalized bandpass network, the state variables will be in a bandpass form. The switched capacitor biquad realizations of Sec. 9.6 can be used to implement each state variable in a many similar to the low pass implementation illustrated earlier. Bandstop filters can be obtained by applying first normalized, low-pass to normalized, high-pass frequency transformation followed by the normalized, low-pass to normalized, bandpass transformation. When the state variables are expressed as a function of themselves plus other variables, the biquad realizations of Sec. 9.6 can also be used for their implementation. Also, high pass and bandpass filters with $j\omega$ axis zeros can be obtained by applying the above transformations to the normalized low pass *RLC* circuits where the inductor cutsets and capacitor loops have been eliminated. The dependent sources will always result in unswitched capacitors connected from a variable to the inverting input of an op amp. Examples of some of these filters are found in the problems at the end of this chapter. Table 9.7-5 summarizes the general approach to designing ladder switched capacitor filters. Most of the applications for switched capacitor ladder filters require low pass or bandpass filters.

Table 9.7-5

Illustration of the general approach to designing ladder switched capacitor filters.



Anti-Aliasing Filters

A very important application of continuous time filters is in anti-aliasing. All discrete-time filters use clocks and sampling. A characterisitic of sampling is that the signal passbands occur at each harmonic of the clock frequency. For example, if a signal with the frequency spectrum of Fig. 9.7-1 is sampled at a clock frequency of f_c, the frequency spectrum will result as that shown in Fig. 9.7-28. The frequency from 0 to ω_{PB} is called the *baseband.* In each passband centered at ω_c and its harmonics, signals and noise in that passband will be passed and aliased into the baseband. Aliasing occurs

when a desired or undesired (noise) signal is within $\pm\omega_{PB}$ of ω_c or any of its harmonics. Aliasing results in unwanted signals in the baseband.

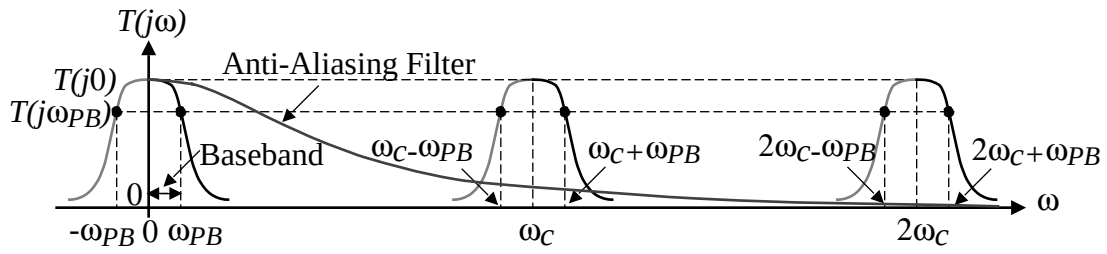


Figure 9.7-28 - Spectrum of a discrete-time filter and a continuous-time anti-aliasing filter.

It is customary to use an anti-aliasing filter to eliminate the aliasing of signals in the higher passband into the baseband. Such a filter is shown in Fig. 9.7-28. The purpose of the anti-aliasing filter is to attenuate the passbands centered at ω_c and its harmonics so that they do not appear in the baseband. Normally, the anti-aliasing filter is a continuous time filter because it does not require the accuracy in time constants that is required of the switched capacitor filter. All the anti-aliasing filter needs to do is to avoid attenuating the baseband and attenuate all of the passbands above the baseband as much as possible.

Some of the popular filters for anti-aliasing are presented in the following. The first filter is called the Sallen-Key filter [26] and is shown in Fig. 9.7-29a. It is a second-order filter that uses positive feedback to achieve complex conjugate poles. The voltage amplifier has a voltage gain of $K = 1$ and is assumed to have an infinite input resistance and a zero output resistance. This voltage amplifier can be realized by the noninverting voltage amplifier shown in Fig. 9.7-7b.

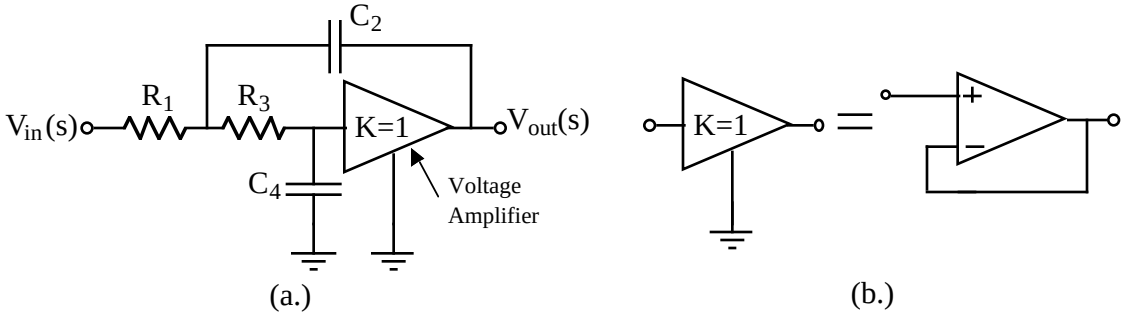


Figure 9.7-29 - (a.) A second-order, low pass active filter using positive feedback. (b.) The realization of the voltage amplifier K by the noninverting op amp configuration.

The closed-loop, voltage transfer function of Fig. 9.7-29a can be found (see Prob. PA1-2) as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\dfrac{K}{R_1R_3C_2C_4}}{s^2 + s\left(\dfrac{1}{R_3C_4} + \dfrac{1}{R_1C_2} + \dfrac{1}{R_3C_2} - \dfrac{K}{R_3C_4}\right) + \dfrac{1}{R_1R_3C_2C_4}} \quad . \tag{81}$$

In order to use this result, we must be able to express the component values of Fig. 9.7-29a (R_1, R_3, C_2, C_4, and K) in terms of the parameters of the standard, second-order, low-

pass transfer function ($T_{LP}(0)$, Q, and ω_o). These relationships are called *design equations* and are the key to designing a given active filter. When equating the coefficients of Eq. (14) to the standard second-order low pass transfer function, three independent equations result. Unfortunately, there are 5 unknowns and therefore a unique solution does not exist. This circumstance happens often in active filter design. To solve this problem, the designer chooses as many additional constraints as necessary to obtain a unique set of design equations.

In order to achieve a unique set of design equations for Fig. 9.7-297a, we need two more independent relationships. Let us choose these relationships as

$$R_3 = nR_1 = nR \tag{82}$$

and

$$C_4 = mC_2 = mC\ . \tag{83}$$

Substituting these relationships into Eq. (81) gives

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1/mn(RC)^2}{s^2 + (1/\mathrm{RC})[(n+1)/n]s + 1/mn(RC)^2}\ . \tag{84}$$

Now, if we equate Eq. (84) to the standard second-order low pass transfer function, we get two design equations which are

$$\omega_o = \frac{1}{\sqrt{mn}RC} \tag{85}$$

$$\frac{1}{Q} = (n+1)\sqrt{\frac{m}{n}} \tag{86}$$

The approach to designing the components of Fig. 9.7-29a is to select a value of m compatible with standard capacitor values such that

$$m \leq \frac{1}{4Q^2}\ . \tag{87}$$

Then, n, can be calculated from

$$n = \left(\frac{1}{2mQ^2} - 1\right) \pm \frac{1}{2mQ^2}\sqrt{1-4mQ^2}\ . \tag{88}$$

Eq. (88) provides two values of n for any given Q and m. It can be shown that these values are reciprocal. Thus, the use of either one produces the same element spread.

Example 9.7-9

Application of the Sallen-Key Antialiasing FIlter

Use the above design approach to design a second-order, low-pass filter using Fig. 9.7-7a if $Q = 0.707$ and $f_o = 1$ kHz

Solution

Eq. (87) implies that m should be less than 0.5. Let us choose $m = 0.5$. Eq. (88) gives $n = 1$. These choices guarantee a Q of 0.707. Now, use Eq. (85) to find the RC product. From Eq. (85) we find that $RC = 0.225 \times 10^{-3}$. At this point, one has to try different values to see what is best for the given situation (typically area required). Let us choose $C = C_2$ 500pF. This gives $R = R_1 = 450k\Omega$. Thus, $C_4 =$ 250pF and $R_3 = 450k\Omega$. It is readily apparent that the anti-aliasing filter will require considerable area to implement.

Because Fig. 9.7-29a is used as an anti-aliasing filter, the RC products do not have to be accurate. Note that the gain of the anti-aliasing filter at low frequencies is well defined by the unity-gain configuration of the op amp. Therefore, the anti-aliasing filter and can be implemented in standard CMOS technology along with the switched capacitor filter.

Another continuous-time filter suitable for anti-aliasing filtering is shown in Fig. 9.7-30. This filter uses frequency-dependent negative feedback to achieve complex conjugate poles. One possible set of design equations is shown on Fig. 9.7-30 [23]. $T_{LP}(0)$, ω_o, and Q are the dc gain, pole-frequency, and pole Q, respectively of the standard second-order, low pass transfer function.

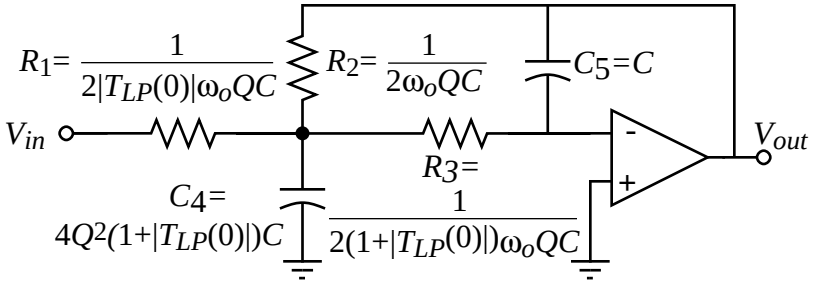


Figure 9.7-30 - A negative feedback realization of a second-order, low pass filter.

Example 9.7-10

Design of A Negative Feedback, Second-Order, Low-Pass Active Filter

Use the negative feedback, second-order, low-pass active filter of Fig. 9.7-30 to design a low-pass filter having a dc gain of -1, $Q = 1/\sqrt{2}$, and $f_o = 10$kHz.

Solution

Let us use the design equations given on Fig. 9.7-30. Assume that $C_5 = C =$ 100pF. Therefore, we get $C_4 = (8)(0.5)C = 400$pF. The resistors are

$$R_1 = \frac{\sqrt{2}}{(2)(1)(6.2832)(10^{-6})} = 112.54\ k\Omega\ .$$

$$R_2 = \frac{\sqrt{2}}{(2)(6.2832)(10^{-6})} = 112.54\ k\Omega\ .$$

and

$$R_3 = \frac{\sqrt{2}}{(2)(6.2832)(2)(10^{-6})} = 56.27\ \text{k}\Omega\ .$$

Unfortunately we see that because of the passive element sizes that anti-aliasing filters will occupy a large portion of the chip.

Noise in Switched Capacitor Filters

In all switched capacitor circuits, a noise aliasing occurs from the passbands that occur at the clock frequency and each harmonic of the clock frequency. This is illustrated by Fig. 9.7-31. It can be shown that the aliasing enhances the baseband noise voltage spectral density by a factor of $2f_{sw}/f_c$. Therefore, the baseband noise voltage spectral density is

$$\overline{e_{BN}^2} = \left(\frac{kT/C}{f_{sw}}\right)\times\left(\frac{2f_{sw}}{f_c}\right) = \frac{2kT}{f_cC}\ \text{volts}^2/\text{Hz} \qquad (89)$$

Multiplying Eq. (89) by $2f_B$ gives the baseband noise voltage in volts(rms)^2. Therefore, the baseband noise voltage is

$$v_{BN}^2 = \left(\frac{2kT}{f_cC}\right)(2f_B) = \frac{2kT}{C}\left(\frac{2f_B}{f_c}\right) = \frac{2kT/C}{OSR}\ \text{volts(rms)}^2 \qquad (90)$$

where *OSR* is the oversampling ratio.

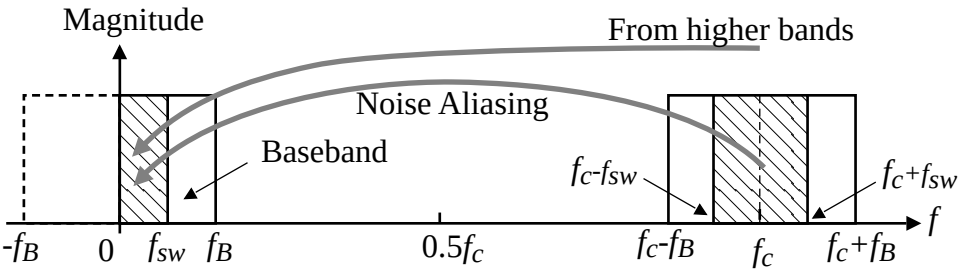


Figure 9.7-31 - Illustration of noise aliasing in switched capacitor circuits.

The noise of switched capacitor filters can be simulated using the above concepts. First, the switched capacitor filter is converted to a continuous time equivalent filter by replacing each switched capacitor with a resistor whose value is $1/(f_cC)$. If the noise of this resistance can be multiplied by $2f_B/f_c$, then the resulting noise will approximate that of the switched capacitor filter. Unfortunately, simulators like SPICE do not permit the multiplication of the thermal noise. Another approach is to assume that the resistors are noise-free and build a noise generator that represents the effect of the noise of Eq. (90). This is done by putting a zero dc current through a resistor identical to the one being modeled. A voltage source that is dependent on the voltage across this resistor can be placed at the input of an op amp to implement Eq. (90). The other resistors of the continuous time realization can be modeled in the same manner. The resulting noise source model along with the normal noise sources of the op amp will serve as a reasonable approximation to the noise in a switched capacitor filter.

9.8 - Summary

The application of switched capacitor circuits compatible with CMOS technology has been presented in this chapter. The key advantage of switched capacitor circuits is that the precision of signal processing becomes proportional to the capacitor ratios which is probably the most accurate aspect of CMOS technology. We have seen that in most cases, it necessary for the clock frequency to be much greater than the signal bandwidth. If this is the case, then the equivalence between the sampled data domain and time domain is straightforward.

All the switched capacitor circuits discussed in this chapter are two-phase. While this simplifies the considerations, there are many applications that divide the clock period into more than two segments. It is necessary that the clocks be nonoverlapping regardless of the number of phases. A disadvantage of switched capacitor circuits is the clock feedthrough that occurs via the overlap capacitance of the switches. While the feedthrough can be minimized, it represents the ultimate accuracy of the switched capacitor circuit.

Applications of switched capacitor circuits from amplifiers, integrators, and filters have been considered. Switched capacitor filters represent an application that has reached maturity and is widely used. Unfortunately, the signal bandwidth must be less than the clock frequency in most switched capacitor filters which prevents the filter from being able to accomplish signal filtering near the bandwidths of the op amps. Switched capacitor circuits are a viable way of accomplishing precision analog signal processing and will be used extensively in the next chapter to implement digital-analog and analog-digital conversion.

Homework Problems

Sec. 9.1

9.1-1 Develop the equivalent resistance expression in Table 9.1-1 for the series switched capacitor resistor emulation circuit.

9.1-2 Develop the equivalent resistance expression in Table 9.1-1 for the bilinear switched capacitor resistor emulation circuit.

9.1-3 What is the accuracy of a time constant implemented with a resistor and capacitor having a tolerance of 10% and 5%, respectively. What is the accuracy of a time constant implemented by a switched capacitor resistor emulation and a capacitor if the tolerances of the capacitors are 5% and the relative tolerance is 0.5%. Assume that the clock frequency is perfectly accurate.

9.1-4 Repeat Example 9.1-3 using a series switched capacitor reistor emulation.

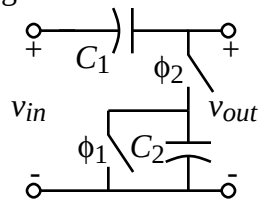


Figure P9.1-5

9.1-5 Find the z-domain transfer function for the circuit shown. Let $\alpha = C_2/C_1$ and find an expression for the discrete time frequency response following the methods of Ex. 9.1-4. Design (find α) a first-order, highpass circuit having a -3dB frequency of 1kHz following the methods of Ex. 9.1-5. Assume that the clock frequency is 100kHz. Plot the frequency response for the resulting discrete time circuit and compare with a first-order, highpass, continuous time circuit.

Sec. 9.2

9.2-1 Fig. P9.2-1 shows two inverting summing amplifiers. Compare the closed-loop frequency response of these two summing amplifiers if the op amp is modeled by $A_{vd}(0) = 10{,}000$ and $GB = 1$MHz.

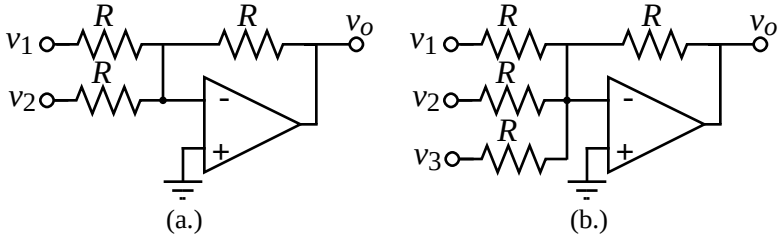


Figure P9.2-1 (a.) 2-input inverting summer. (b.) 3-input inverting summer.

9.2-2 Repeat Problem 9.2-1 if the resistors are replaced by equal valued capacitors.

9.2-3 Replace the parallel switched capacitor resistor emulation in Fig. 9.2-4(b.) with the series switched capacitor resistor emulation and find the z-domain transfer function for $H^{ee}(z)$.

9.2-4 Verify the transresistance of Fig. 9.2-6a.

9.2-5 The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{oe}(z)$. (2.) If $C_1 = 10C_2$, plot the magnitude and phase response of the switched capacitor circuit from 0 Hz to the clock frequency (f_c). Assume that the op amp is ideal for this problem. (F91E1P2)

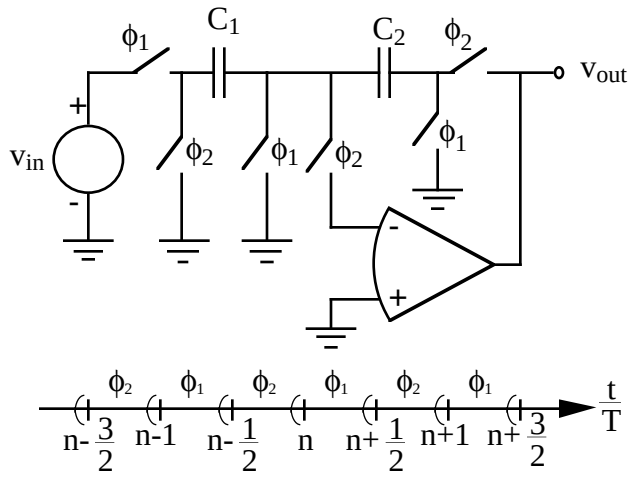


Figure P9.2-5

9.2-6 Find $H^{oe}(z)$ ($=V_2^e(z)/V_1^o(z)$) of the switched capacitor circuit shown. Replace z by $e^{j\omega t}$ and identify the magnitude and phase response of this circuit. Assume $C_1 = C_2$. Sketch the magnitude and phase response on a linear-linear plot from f=0 to f=f_c. What is the magnitude and phase at f = $0.5f_c$? (F95FEP7)

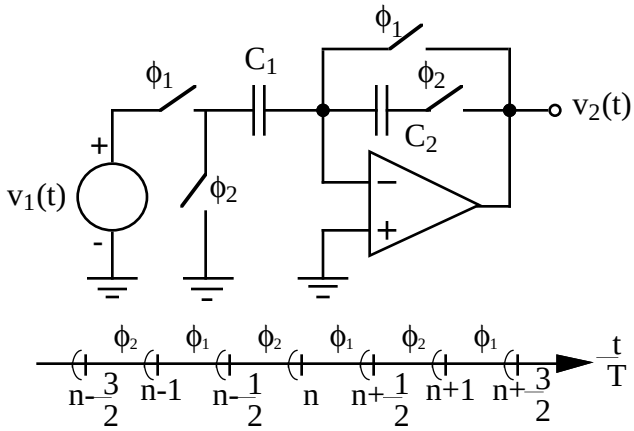


Figure P9.2-6

9.2-7 (a.) Find $H^{oo}(z)$ for the switched capacitor circuit shown. Ignore the fact that the op amp is open loop during the ϕ_1 phase and assume that the output is sampled during ϕ_2 and held during ϕ_1. Note that some switches are shared between the two switched capacitors.

(b.) Sketch the magnitude and phase of the sampled data frequency response from 0 to the clock frequency in Hertz. (F97E2P5)

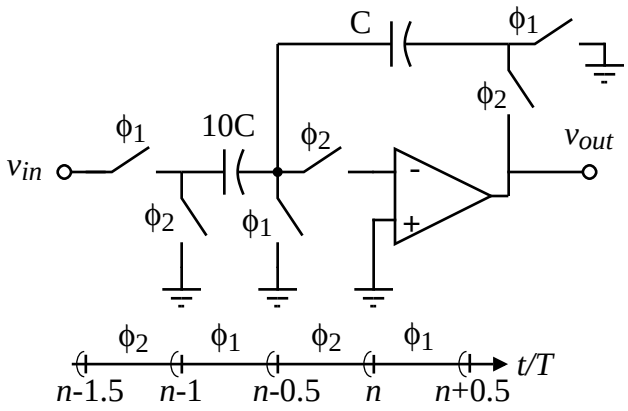


Figure P9.2-7

9.2-8 Find the exact form of Eq. (42) by including the C_{OL} from *all* switches connected to the node.

9.2-9 Rederive Eqs. (42) and (43) including the influence of a bulk-drain, C_{BD}, and a bulk-source, C_{BS}, capacitance. (This problem cited text.)

9.2-10 Repeat the derivation following Fig. 9.2-9 resulting in Eq. (50) if the clock phases of the leftmost two switches are interchanged (in otherwords, the circuit is an inverting amplifier).

9.2-11 In the circuit shown, the capacitor C_1 has been charged to a voltage of V_{in} ($v_{in}>0$). Assuming that C_2 is uncharged, find an expression for the output voltage, V_{out}, after the ϕ_1 clock is applied. Assume that rise and fall times of the ϕ_1 clock are slow enough so that the channel of the NMOS transistor switch tracks the gate voltage. The on and off voltages of ϕ_1 are 10V and 0V, respectively. Evaluate the dc offset at the output if the various parameters for this problem are V_T = 1V, $C_{gs} = C_{gd}$ = 100fF, C_1 = 5pF, and C_2 = 1pF. (W91E2P3)

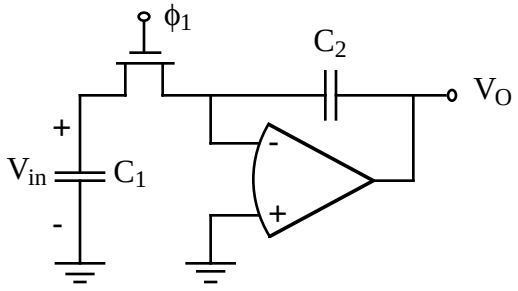


Figure P9.2-11

9.2-12 A switched-capacitor amplifier is shown. What is the minimum clock frequency that would permit the ideal output voltage to be reached to within 1% if the op amp has a dc gain of 10,000 and a single dominant pole at -100 rads/sec.? Assume ideal switches. (F95FEP8)

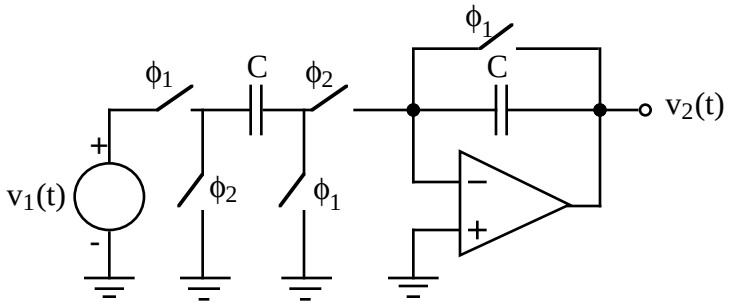


Figure P9.2-12

9.2-13 The following switched capacitor circuit is an amplifier that avoids shorting the output of the op amp to ground during the ϕ_1 phase period. Use the clock scheme shown along with the timing and find the z-domain transfer function, $H^{oo}(z)$. Sketch the magnitude and phase shift of this amplifier from zero frequency to the clock frequency, f_c. (F96E2P5)

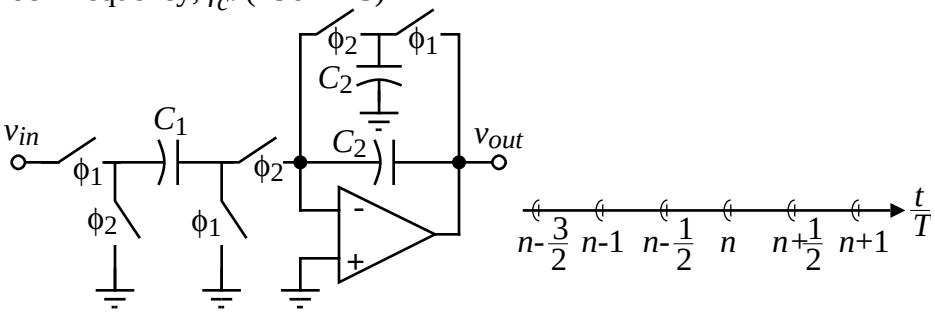


Fig. P9.2-13

9.2-14 (a.) Give a schematic drawing of a switched capacitor realization of a voltage amplifier having a gain of H^{oo} = +10V/V using a two-phase nonoverlapping clock. Assume that the input is sampled on the ϕ_1 and held during ϕ_2. Use op amps, capacitors, and switches with ϕ_1 or ϕ_2 indicating the phase the switch is closed.

(b.) Give a schematic of the circuit in (a.) that reduces the number of switches to a minimum number with the circuit working correctly. Assume the op amp is ideal.

(c.) Convert the circuit of (a.) to a differential implementation using the differential-in, differential-out op amp shown. (F97E2P4)

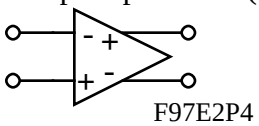


Figure 9.2-14

Sec. 9.3

9.3-1 Over what frequency range will the integrator of Ex. 9.3-1 have a ±1° phase error?

9.3-2 Show Eq. (12) is developed from Fig. 9.3-4(b.).

9.3-3 Find the $H^{eo}(j\omega T)$ transfer function for the inverting integrator of Fig. 9.3-4b and compare with the $H^{ee}(j\omega T)$ transfer function.

9.3-4 An inverting, switched-capacitor integrator is shown. If the gain of the op amp is A_o, find the z-domain transfer function of this integrator. Identify the ideal part of the transfer function and the part due to the finite op amp gain, A_o. Find an expression for the excess phase due to A_o. (W91E2P4)

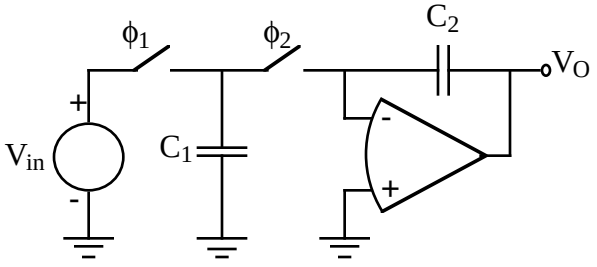


Figure P9.3-4

9.3-5 For the switched-capacitor circuit shown find $V^{o}_{OUT}(z)$ as a function of $V^{o}_{1}(z)$, $V^{o}_{2}(z)$, and $V^{o}_{3}(z)$ assuming the clock is a two-phase, nonoverlapping clock. Assume that the clock frequency is much greater than the signal bandwidth and find an approximate expression for $V_{out}(s)$ in terms of $V_1(s)$, $V_2(s)$, and $V_3(s)$. (F91FEP4)

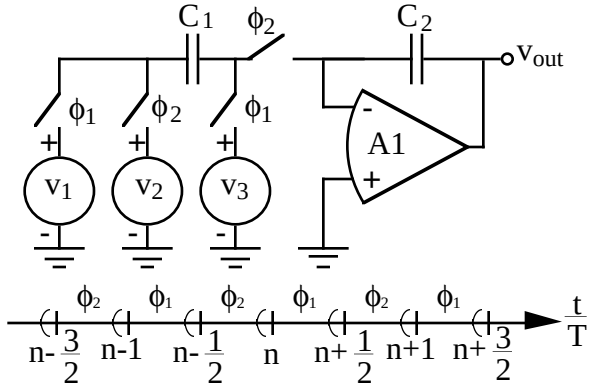


Figure P9.3-5

9.3-6 The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{oo}(z)$. (2.) Replace z by $e^{j\omega T}$ and plot the magnitude and phase of this switched capacitor circuit from 0 Hz to the clock frequency, f_c, if $C_1 = C_3$ and $C_2 = C_4$. Assume that the op amps are ideal for this problem. (3.) What is the multiplicative magnitude error and additive phase error at $f_c/2$? (F91E1P3)

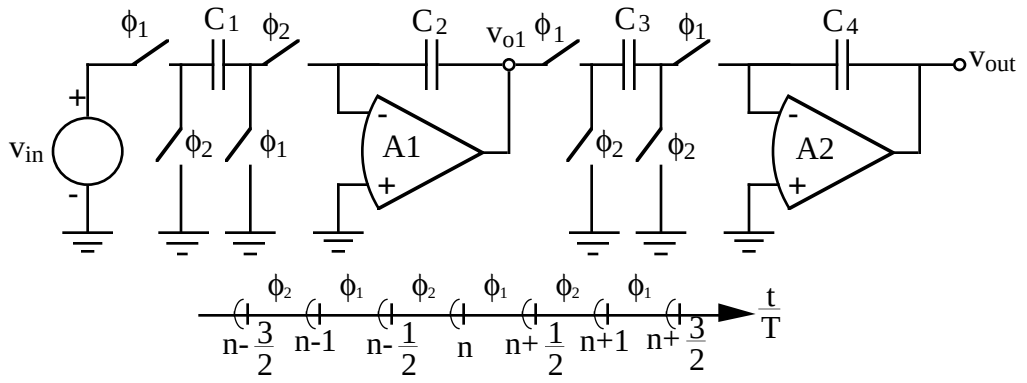


Figure P9.3-6

9.3-7 Find $H^{oo}(z)$ ($=V^{o}_{out}(z)/V^{o}_{in}(z)$) of the switched capacitor circuit shown. Replace z by $e^{j\omega t}$ and identify the magnitude and phase response of this circuit. Assume $C_1/C_2 = \pi/25$. Sketch the exact magnitude and phase response on a linear-linear plot from f=0 to f=f_c. What is the magnitude and phase at f = $0.5f_c$? Assume that the op amp is ideal. (F95FEP1)

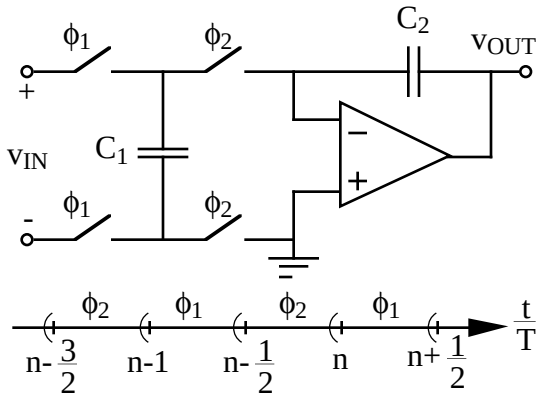


Figure P9.3-7

9.3-8 The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{ee}(z)$. (2.) If $C_2 = 0.2\pi C_1$, plot the magnitude and phase response of the switched capacitor circuit from 0 rps to the clock frequency (ω_c). Assume that the op amp is ideal for this problem. It may be useful to remember that Eulers formula is $e^{\pm jx} = \cos(x) \pm j\sin(x)$. (F92E1P4)

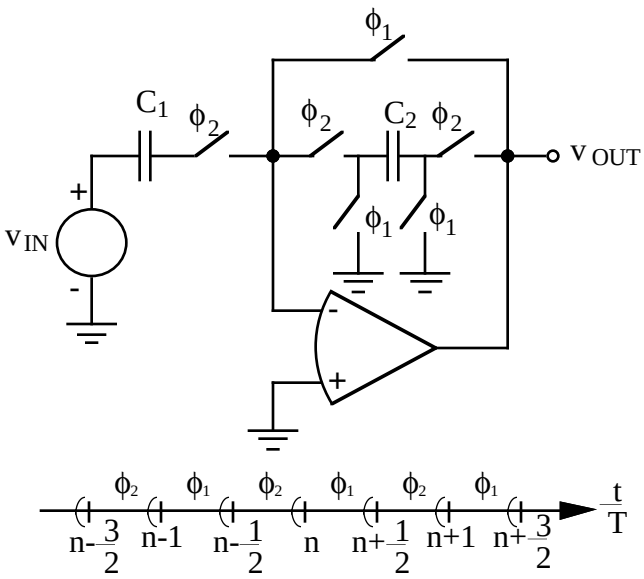


Figure P9.3-8

9.3-9 Find the z-domain transfer function, $H^{oo}(z)$, for the circuit shown. Assume that $C_2 = C_3 = C_4 = C_5$. Also, assume that the input is sampled during ϕ_1 and held through ϕ_2. Next, let the clock frequency be much greater than the signal frequency and find an expression for $H^{oo}(j\omega)$. What kind of circuit is this? (F97FEP2)

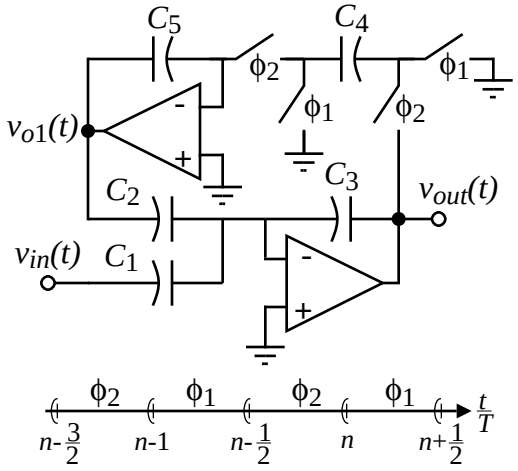


Figure P9.3-9

Sec. 9.4

9.4-1 Repeat Ex. 9.4-1 for the positive switched capacitor transresistance circuit of Fig. 9.4-3.

9.4-2 Use the z-domain models to verify Eqs. (19) and (23) of Sec. 9.2 for Fig. 9.2-4(b.).

9.4-3 Repeat Ex. 9.4-5 assuming that the op amp is ideal (gain = ∞). Compare with the results of Ex. 9.4-5 (Hint: use Fig. 9.4-8b).

9.4-4 Repeat Ex. 9.4-5 assuming the op amp gain is 100V/V. Compare with the results of Ex. 9.4-5.

9.4-5 Repeat Ex. 9.4-5 for the inverting switched capacitor integrator in Fig. 9.3-4(b.).

Sec. 9.5

9.5-1 Develop Eq. (6) for the inverting low pass circuit obtained from Fig. 9.1-5(a.) by reversing the phases of the leftmost two switches. Verify Eq. (7). (This prob. cited in text)

9.5-2 Use SPICE to simulate the results of Ex. 9.5-1.

9.5-3 Repeat Ex. 9.5-1 for a first-order, lowpass circuit with a low frequency gain of +1 and a -3*dB* frequency of 5kHz.

9.5-4 Design a switched capacitor realization for a first-order , lowpass circuit with a low frequency gain of -10 and a -3*dB* frequency of 1kHz using a clock of 100kHz.

9.5-5 Design a switched capacitor realization for a first-order , highpass circuit with a low frequency gain of -10 and a -3*dB* frequency of 1kHz using a clock of 100kHz.

9.5-6 Repeat Ex. 9.5-2 for a treble boost circuit having 0*dB* gain from dc to 1kHz and a increase of gain at +20*dB*/dec. from 1kHz to 10kHz with a gain of +20*dB* from 10kHz and above (the mirror of the response of Fig. 9.5-7 around 1kHz).

9.5-7 The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{oo}(z)$. (2.) Plot the magnitude and phase response of the switched capacitor circuit from 0 rps to the clock frequency (ω_c). Assume that the op amp is ideal for this problem. It may be useful to remember that Eulers formula is $e^{\pm jx} = \cos(x) \pm j\sin(x)$. (F93E2P4)

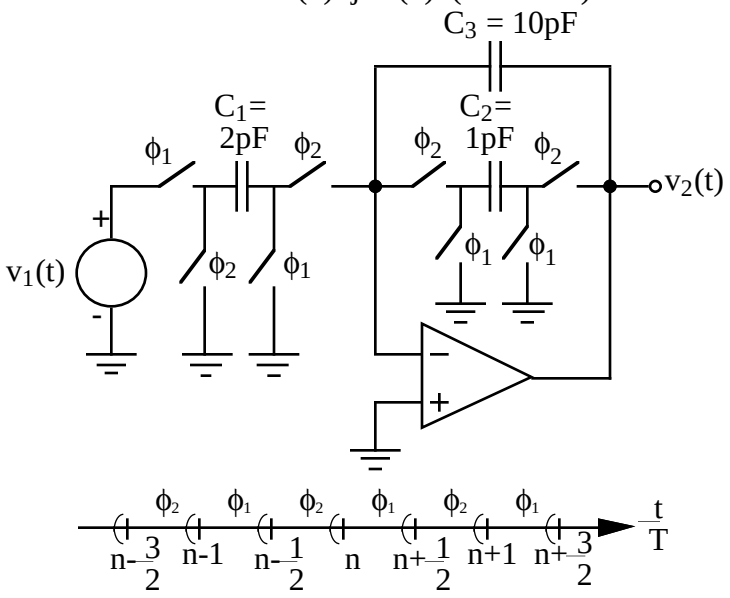


Figure P9.5-7

9.5-8 The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (a.) Find the *z*-domain expression for $H^{oo}(z)$. (b.) Use your expression for $H^{oo}(z)$ to design the values of C_1 and C_2 to achieve a realization to

$$H(s) = \frac{10{,}000}{s+1000}$$

if the clock frequency is 100kHz and C_3 = 10pF. Assume that the op amp is ideal. (F96FEP1)

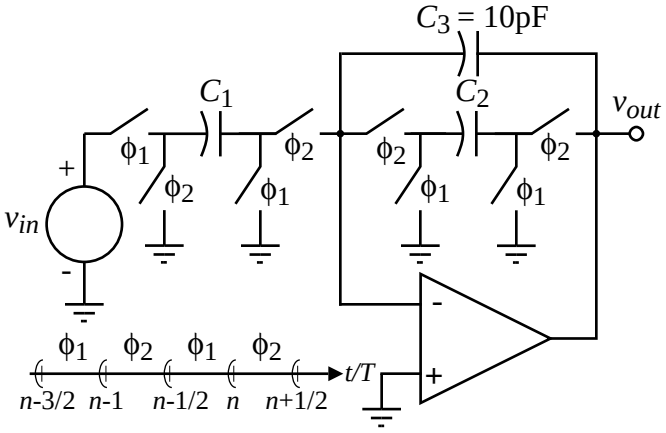


Figure P9.5-8

9.5-9 Find $H^{oo}(z)$ of the switched capacitor circuit shown. Replace z by $e^{j\omega T}$ and identify the magnitude and phase response of this circuit. (F93FEP8)

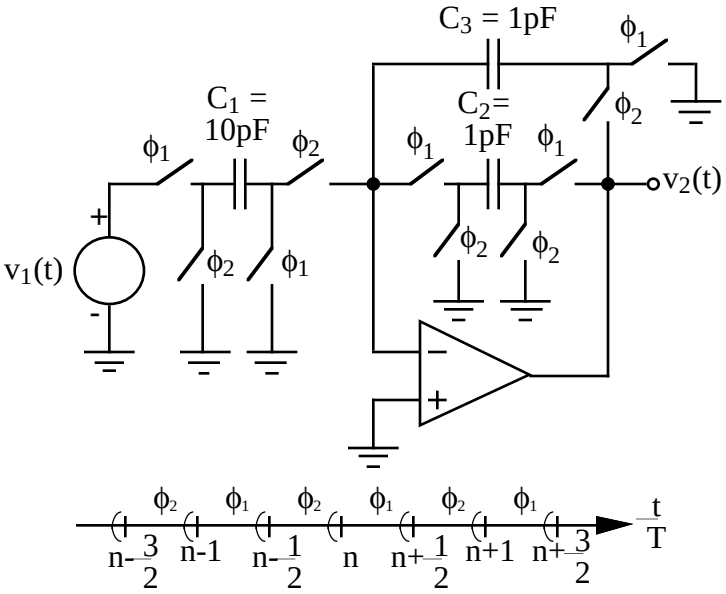


Figure P9.5-9

9.5-10 The switched capacitor circuit shown is used to realize an audio bass-boost circuit. Find

$$H(e^{j\omega T}) = \frac{V_{out}(e^{j\omega T})}{V_{in}(e^{j\omega T})}$$

assuming that $f_c >> f_{signal}$. If $C_2 = C_4$ = 1000pF and f_c = 10kHz, find the value of C_1 and C_3 to implement the following transfer function. (F95FEP2)

$$\frac{V_{out}(s)}{V_{in}(s)} = -10\left(\frac{\frac{s}{100}+1}{\frac{s}{10}+1}\right)$$

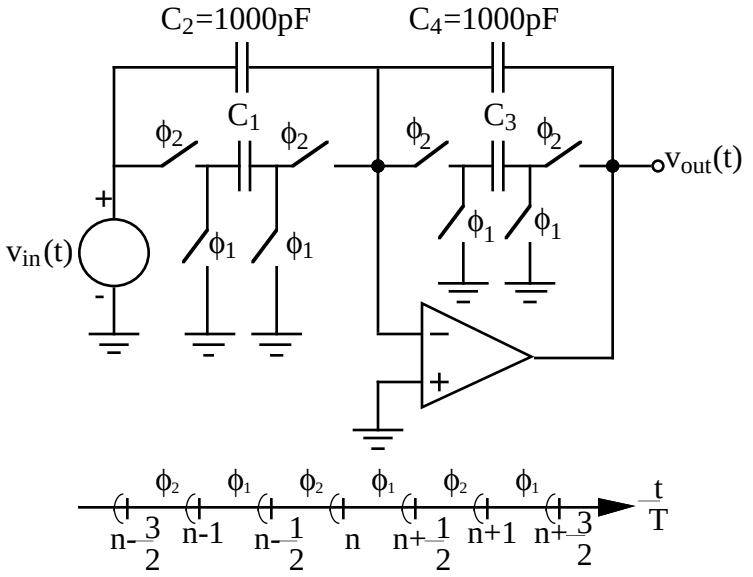


Figure P9.5-10

Sec. 9.6

9.6-1 Combine Figs. 9.6-2a and 9.6-2b to form a continuous time biquad circuit. Replace the negative resistor with an inverting op amp and find the s-domain frequency response. Compare your answer with Eq. (1).

9.6-2 (a.) Use the low-Q switched capacitor biquad circuit shown to design the capacitor ratios of a lowpass second-order filter with a pole frequency of 1kHz, Q = 5 and a gain at dc of -10 if the clock frequency is 100kHz. What is the total capacitance in terms of an arbitrary unit of capacitance, C_u?

(b.) Find the clock frequency, f_c, that keeps all capacitor ratios less than 10:1. What is the total capacitance in terms of C_u for this case? (F97FEP1)

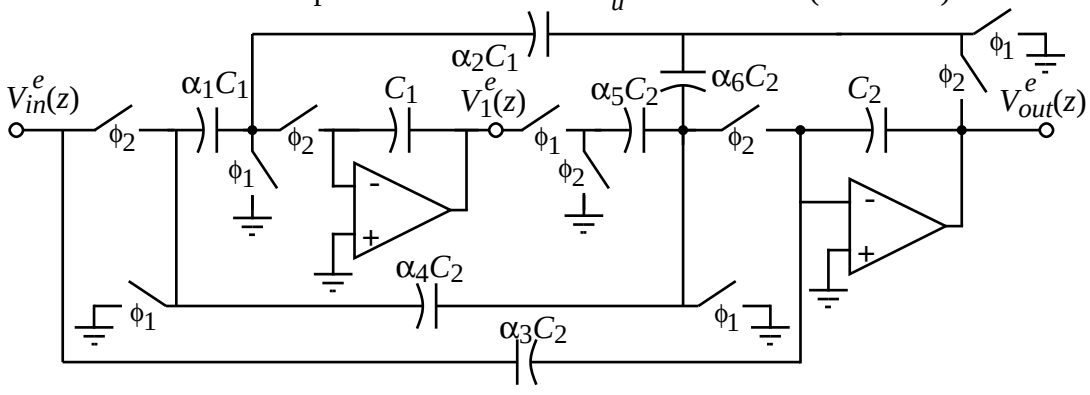


Figure P9.6-2

9.6-3 A Tow-Thomas continuous time filter is shown. Give a discrete-time realization of this filter using strays-insensitive integrators. If the clock frequency is much

greater than the filter frequencies, find the coefficients, a_i and b_i, of the following z-domain transfer function in terms of the capacitors of the discrete-time realization. (W91E2P2)

$$H(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{b_0 + b_1 z^{-1} + b_2 z^{-2}}$$

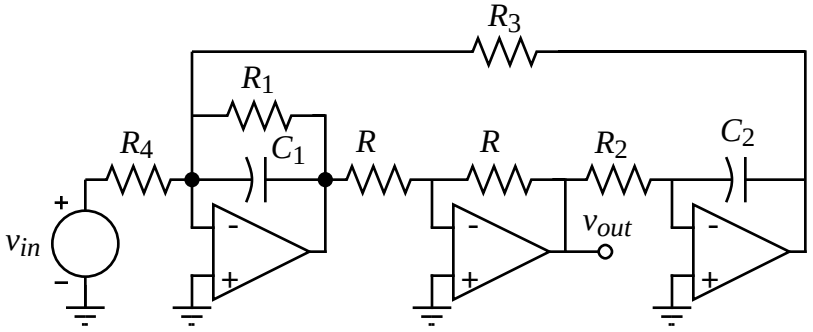


Figure P9.6-3

9.6-4 Find the z-domain transfer function $H(z) = V_{out}(z)/V_{in}(z)$ in the form of

$$H(z) = \frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + b_0}$$

for the switched capacitor circuit shown below. Evaluate the a_i's and b_i's in terms of the capacitors. Next, assume that $\omega T << 1$ and find H(s). What type of second-order circuit is this? (W95E2P3)

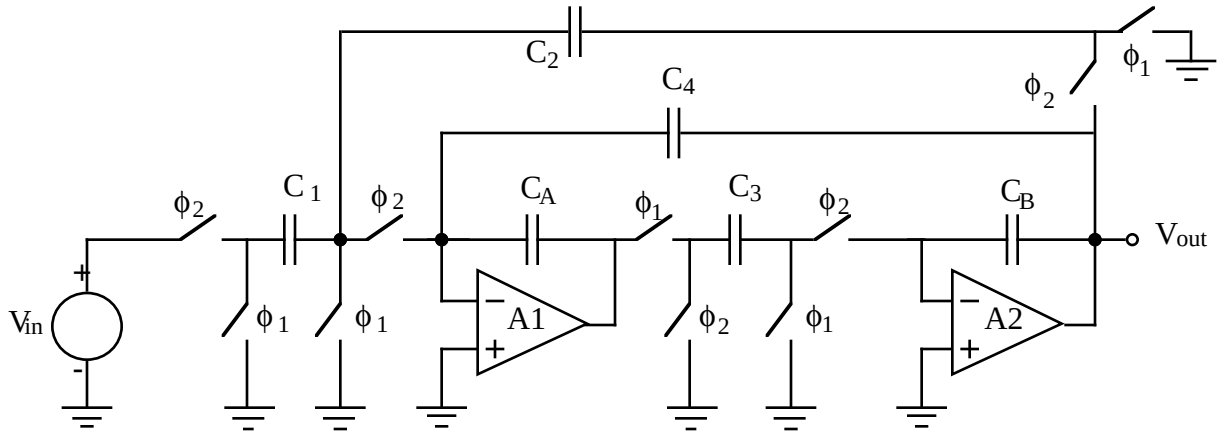


Figure P9.6-4

9.6-5 Find the z-domain transfer function $H(z) = V_{out}(z)/V_{in}(z)$ in the form of

$$H(z) = -\left[\frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}\right]$$

for the switched capacitor circuit shown below. Evaluate the a_i's and b_i's in terms of the capacitors. Next, assume that $\omega T << 1$ and find H(s). What type of circuit is this? (W96FEP4)

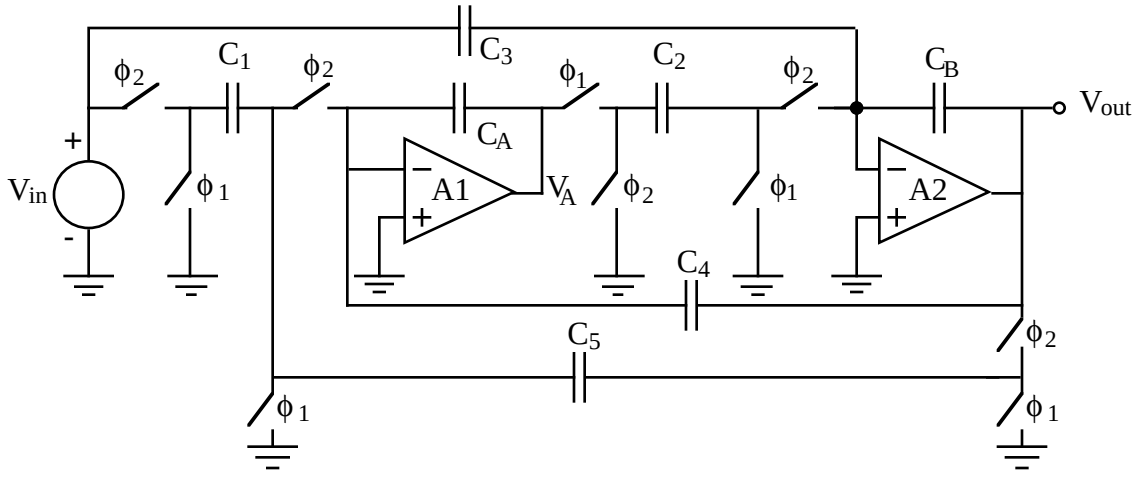


Figure P9.6-5

9.6-6 Find the z-domain transfer function $H(z) = V_{out}(z)/V_{in}(z)$ in the form of

$$H(z) = -\left[\frac{a_2z^2 + a_1z + a_0}{z^2 + b_1z + b_0}\right]$$

for the switched capacitor circuit shown below. Evaluate the a_i's and b_i's in terms of the capacitors. Next, assume that $\omega T << 1$ and find H(s). What type of second- order circuit is this? What is the pole frequency, ω_o, and pole Q? (W97E2NewP4)

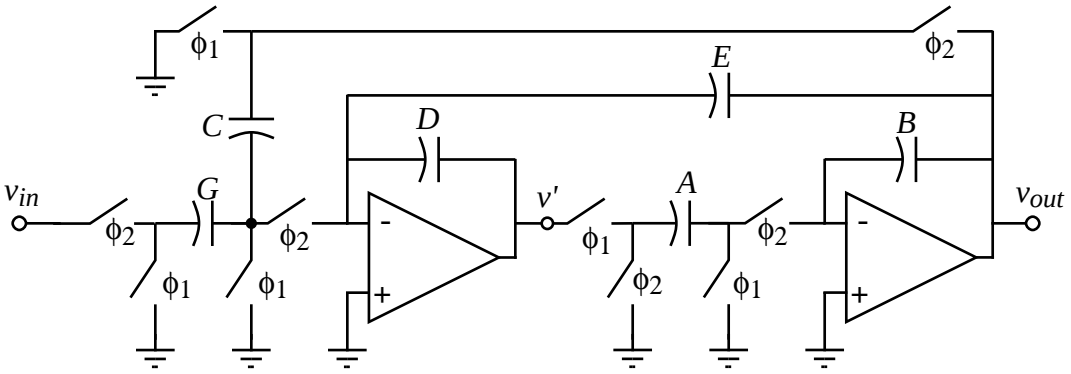


Figure P9.6-6

9.6-7 The switched capacitor circuit shown below realizes the following z-domain transfer function

$$H(z) = -\left(\frac{a_2z^2 + a_1z + a_0}{b_2z^2 + b_1z + 1}\right)$$

where $C_6 = a_2/b_2$, $C_5 = (a_2\text{-}a_0)/b_2C_3$, $C_1 = \frac{a_0+a_1+a_2}{b_2C_3}$, $C_4 = \frac{1-(b_0/b_2)}{C_3}$ and $C_2C_3 = \frac{1+b_1+b_2}{b_2}$. Design a switched capacitor realization for the function

$$H(s) = \frac{-10^6}{s^2 + 100s + 10^6}$$

where the clock frequency is 10 kHz. Use the bilinear transformation, $s = (2/T)[(z-1)/(z+1)]$, to map H(s) to H(z). Choose $C_2 = C_3$ and assume that $C_A = C_B = 1$. (W94E2P4)

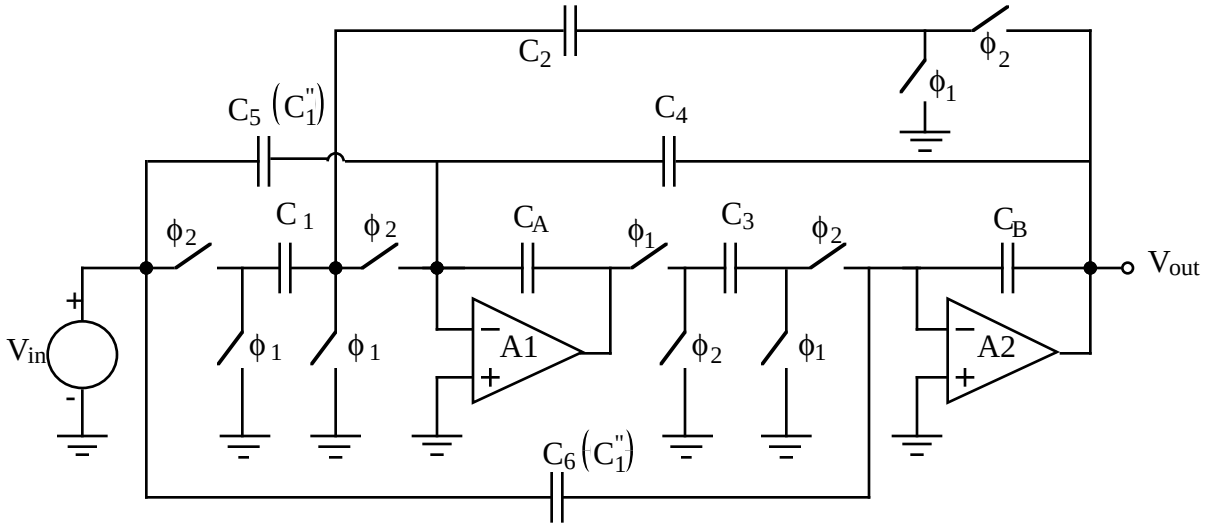


Figure P9.6-7

Sec. 9.7

9.7-1 Find the minimum order of a Butterworth and Cheybshev filter approximation to a filter with the specifications of $T_{PB} = -3dB$, $T_{SB} = -40dB$, and $\Omega_n = 2.0$.

9.7-2 Find the transfer function of a fifth-order, Butterworth filter approximation expressed as products of first- and second-order terms. Find the pole frequency, ω_p and the Q for each second-order term.

9.7-3 Redesign the 3rd stage of Ex. 9.7-5 using the high-Q biquad and find the total capacitance required for this stage. Compare with the example

9.7-4 Design a cascaded, switched capacitor, 5th-order, lowpass filter using the cascaded approach based on the following lowpass, normalized prototype transfer function.

$$H_{lpn}(s_n) = \frac{1}{(s_n+1)(s_n^2+0.61804s_n+1)(s_n^2+1.61804s_n+1)}$$

The passband of the filter is to 1000Hz. Use a clock frequency of 100kHz and design each stage giving the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio, and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

9.7-5 Repeat Problem 9.7-3 for a 5th-order, highpass filter having the same passband frequency. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

9.7-6 Repeat Problem 9.7-3 for a 5th-order, bandpass filter having center frequency of 1000Hz and a -3dB bandwidth of 500Hz. Use SPICE to plot the frequency

response (magnitude and phase) of your design and the ideal continuous time filter.

9.7-7 Design a switched capacitor 6th-order, bandpass filter using the cascaded approach and based on the following lowpass, normalized prototype transfer function.

$$H_{lpn}(s_n) = \frac{2}{(s_n+1)(s_n^2+2s_n+2)}$$

The center frequency of the bandpass filter is to be 1000Hz with a bandwidth of 100Hz. Use a clock frequency of 100kHz. Design each stage given the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

9.7-8 Design a switched capacitor, third-order, highpass filter based on the lowpass normalized prototype transfer function of Problem 9.7-7. The cutoff frequency (f_{PB}), is to be 1000Hz. Design each stage given the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

9.7-9 Design a switched capacitor, third-order, highpass filter based on the following lowpass, normalized prototype transfer function.

$$H_{lpn}(s_n) = \frac{0.5(s_n^2+4)}{(s_n+1)(s_n^2+2s_n+2)}$$

The cutoff frequency (f_{PB}), is to be 1000Hz. Design each stage given the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

9.7-10 Write the minimum set of state equations for each of the circuits shown below. Use voltage analogs of current (R=1Ω). The state equations should be in the form of the state variable equal to other state variables, including itself. (W95FEP1)

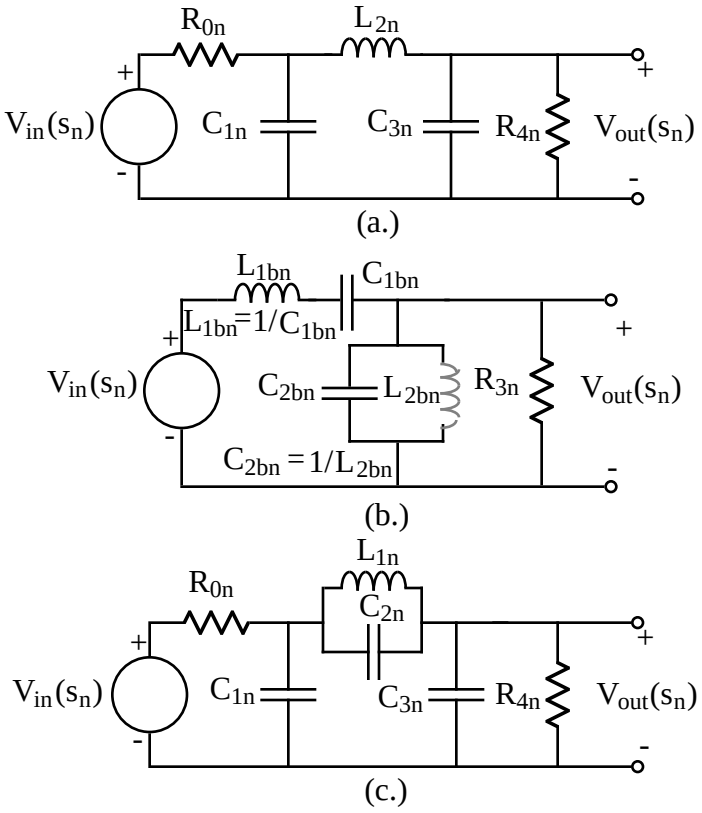


Figure P9.7-10

9.7-11 Give a continuous time and switched capacitor implementation of the following state equations. Use minimum number of components and show the values of the capacitors and the phasing of each switch (ϕ_1 and ϕ_2). Give capacitor values in terms of the parameters of the state equations and Ω_n and f_c for the switched capacitor implementations. (W95FEP2)

1.) $V_1 = \frac{1}{sK}[-\alpha_1 V_1 + \alpha_2 V_2 - \alpha_3 V_3]$

2.) $V_1 = \frac{s}{s^2+1}[-\alpha_1 V_1 + \alpha_2 V_2 - \alpha_3 V_3]$

3.) $V_1 = \frac{1}{sK}[-\alpha_1 V_1 + \alpha_2 V_2] + \alpha_3 V_3$

9.7-12 Find a switched capacitor, realization of the low-pass normalized RLC ladder filter shown. The cutoff frequency of the low-pass filter is 1000Hz and the clock frequency is 100kHz. Give the value of all capacitors in terms of the integrating capacitor of each stage and show the correct phasing of switches. What is the C_{max}/C_{min} and the total units of capacitance for this filter? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter. (W91E1P5)

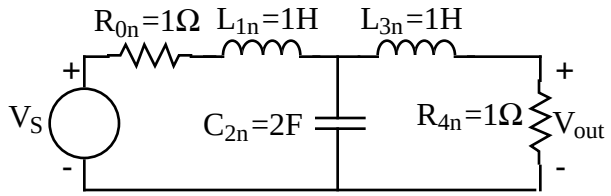


Figure P9.7-12

9.7-13 Design a switched capacitor realization of the low-pass prototype filter shown assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C. Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is C_{max}/C_{min}? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter. (W93E2NewP4)

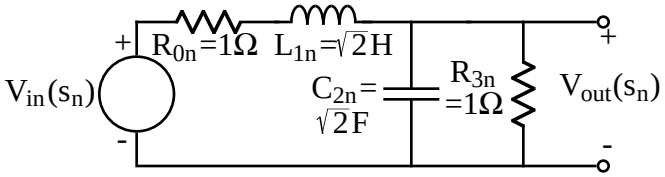


Figure P9.7-13

9.7-14 Design a switched capacitor realization of the low-pass prototype filter shown assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C. Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is C_{max}/C_{min}? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter. (W94E2P3)

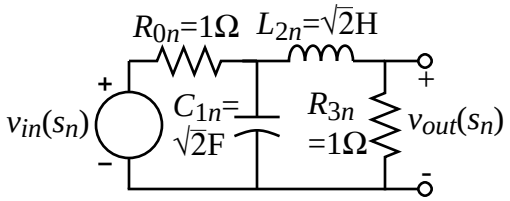


Figure P9.7-14

9.7-15 Design a switched capacitor realization of the low-pass prototype filter shown below assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C. Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is largest C_{max}/C_{min}? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter. (W95E2P2)

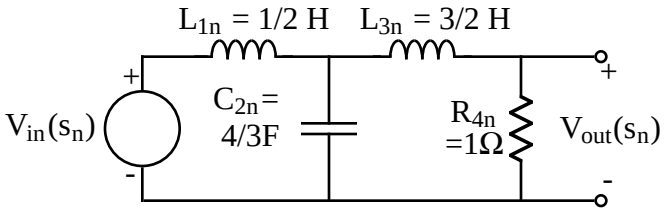


Figure P9.7-15

9.7-16 Design a switched capacitor realization of the low-pass prototype filter shown below assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C (the capacitor connected from op amp output to inverting input). Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is largest C_{max}/C_{min}? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter. (W96FEP3)

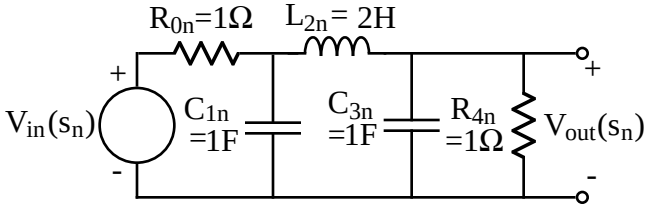


Figure P9.7-16

9.7-17 Design a switched capacitor realization of the low-pass prototype filter shown below assuming a clock frequency of 200 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C (the capacitor connected from op amp output to inverting input). Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is largest C_{max}/C_{min}? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter. (W97E2P3)

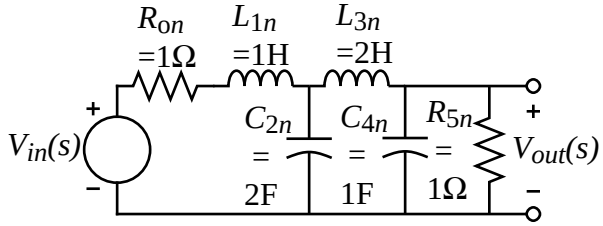


Figure P9.7-17

9.7-18 Use the low-pass, normalized prototype filter of Fig. P9.7-14 to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 500Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter. (W91E2P1)

9.7-19 Use the low-pass, normalized prototype filter of Fig. P9.7-13 to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 500Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

9.7-20 Use the low-pass, normalized prototype filter shown to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 100Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

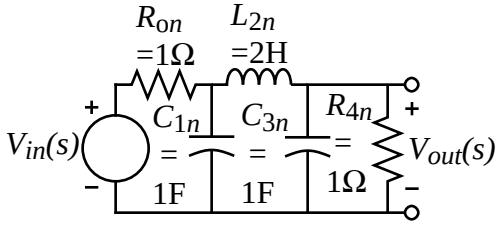


Figure P9.7-20

9.7-21 Use the low-pass, normalized prototype filter shown to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 100Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

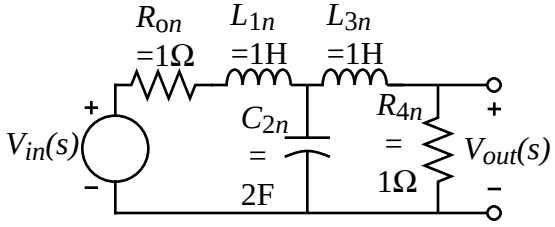


Figure P9.7-21

9.7-22 A second-order, lowpass, Sallen and Key active filter is shown along with the transfer function in terms of the components of the filter.

a.) Define $n = R_3/R_1$ and $m = C_4/C_2$ and let $R_1 = R$ and $C_2 = C$. Develop the design equations for Q and ω_o if K = 1.

b.) Use these equations to design for a second-order, lowpass, Butterworth anti-aliasing filter with a bandpass frequency of 10kHz. Let $R_1 = R = 10k\Omega$ and find the value of C_2, R_3, and C_4. (W96FEP7)

$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{K}{R_1R_3C_2C_4}}{s^2+s\left[\dfrac{1}{R_3C_4}+\dfrac{1}{R_1C_2}+\dfrac{1}{R_3C_2}-\dfrac{K}{R_3C_4}\right]+\dfrac{1}{R_1R_3C_2C_4}}$$

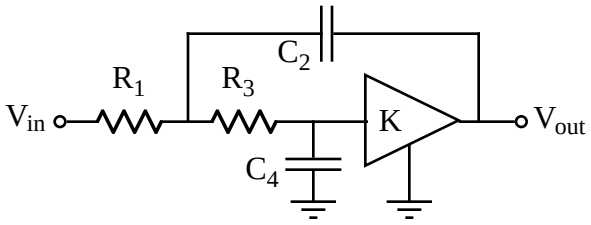


Figure P9.7-22

9.7-23 The circuit shown is to be analyzed to determine its capability to realize a second-order transfer function with complex conjugate poles. Find the transfer function of the circuit and determine and verify the answers to the following questions:

1.) Is the circuit low-pass, bandpass, high-pass, or other?

2.) Find H_o, ω_o, and Q in terms of R_1, C_2, R_3, and C_4.

3.) What elements would you adjust to independently tune Q and ω_o?

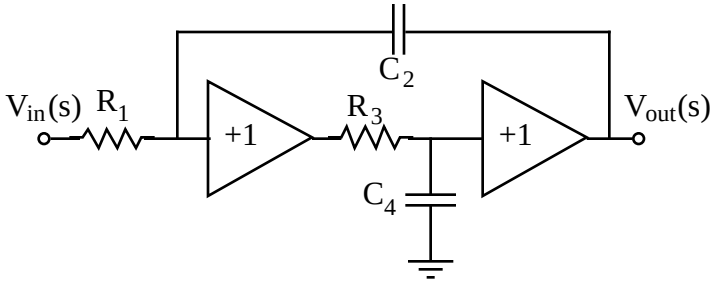


Figure P9.7-23

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